A multi-channel cryogenic low-noise skipper-CCD readout ASIC

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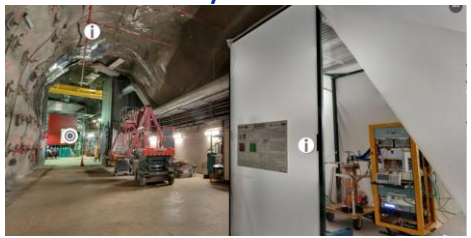
Outline

- Skipper CCDs used for Dark Matter
- Midna ASIC for Skipper CCD Readout
- Midna Architecture and Simulation Results
- Future Development

Skipper-CCD for Dark Matter Search

FNAL / MINOS



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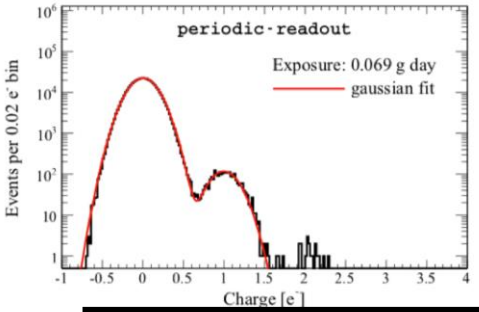
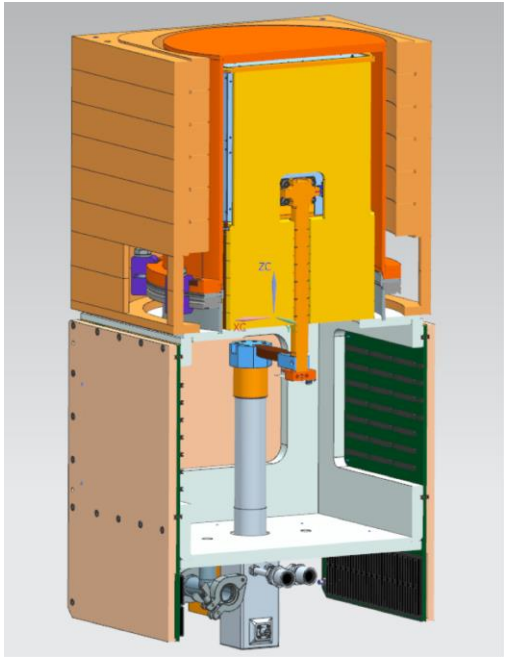


SNOLAB

During December 2019 we installed the first skipper-CCD at SNOLAB. (2.5 g active mass)

SENSEI 100



Design for the 100g experiment is done, and orders for parts have been placed.

Next: 24 Gigapixel digital camera for dark matter!

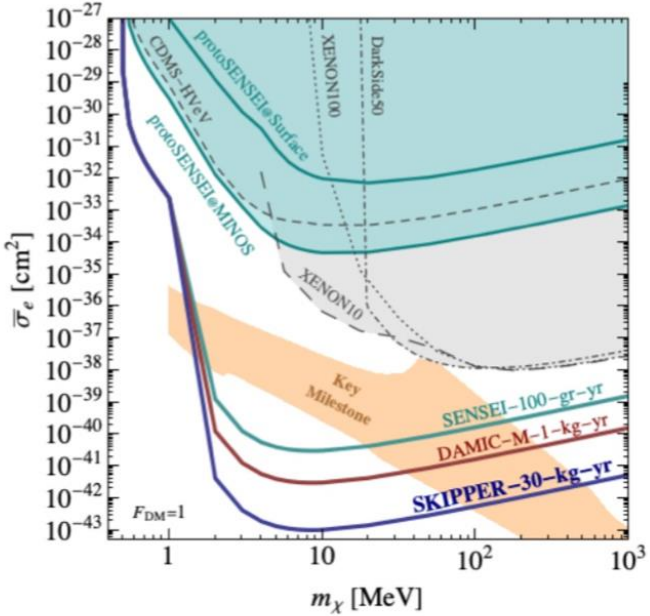
Cooling, readout, packaging and testing of the required **4000 skipper-CCD sensors require engineering solutions that are not available yet for scientific CCDs.**

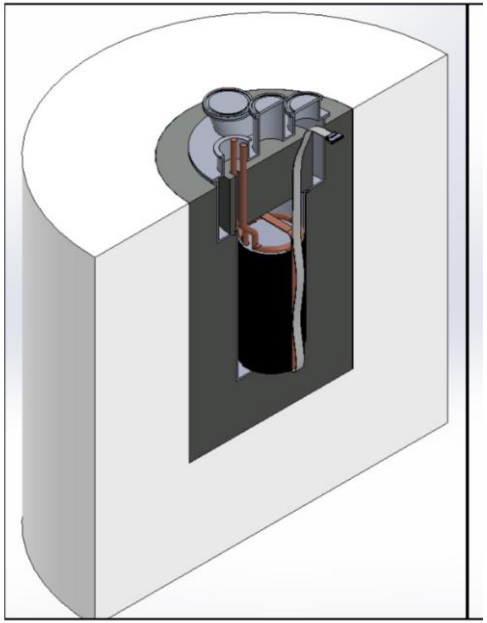
Multi skipper-CCD modules for SENSEI-100 currently being tested with great success.

Oscura 4 year Research and Development Effort

"DOE Dark matter New Initiatives" FNAL, LBNL, PNNL, U. Chicago, U. Washington, Stony Brook University.

Fermilab is leading the effort to develop the a skipper-CCD dark matter detector with active mass of 10 kg of Silicon.



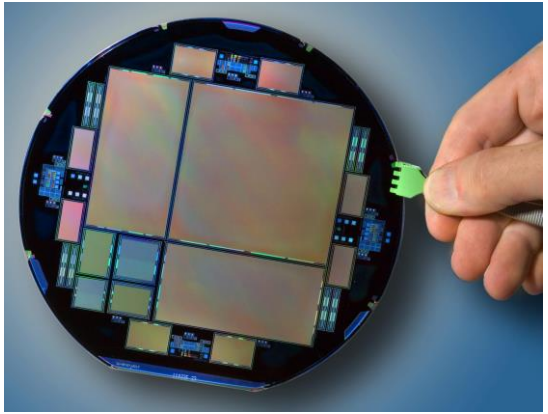


24 Gigapixel digital camera for dark matter!

Cooling, readout, packaging and testing of the required **4000 skipper-CCD sensors require engineering solutions that are not available yet for scientific CCDs.**

Radiation background required is ~10 lower than state of the art experiments.

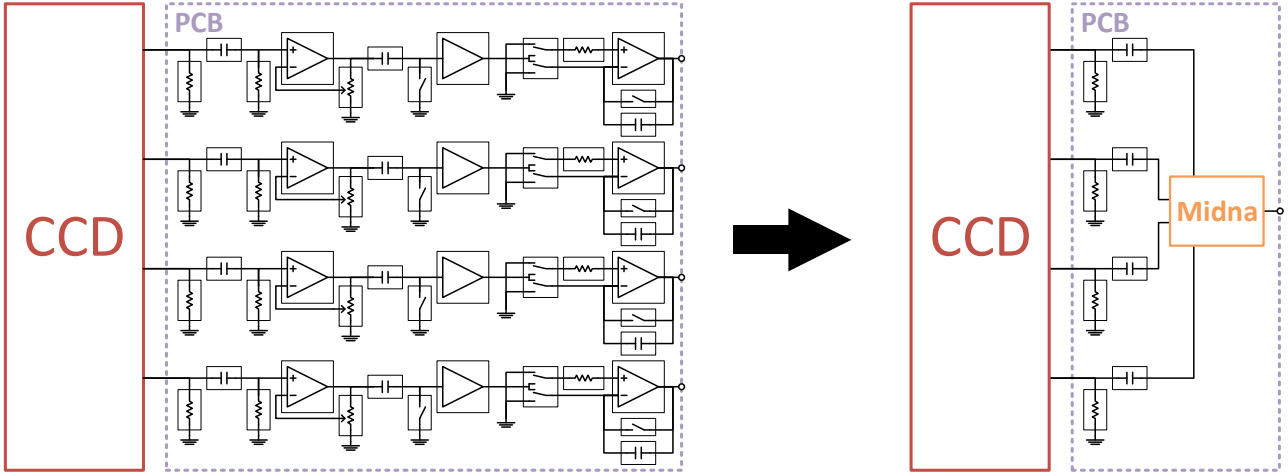
Fabrication of **skipper-CCDs is needs to be adapted to the changes in the semiconductor industry. We have identified new industrial** partners for this, and will be testing them over the next year.



Taking the skipper-CCDs to their full potential as dark matter detectors.

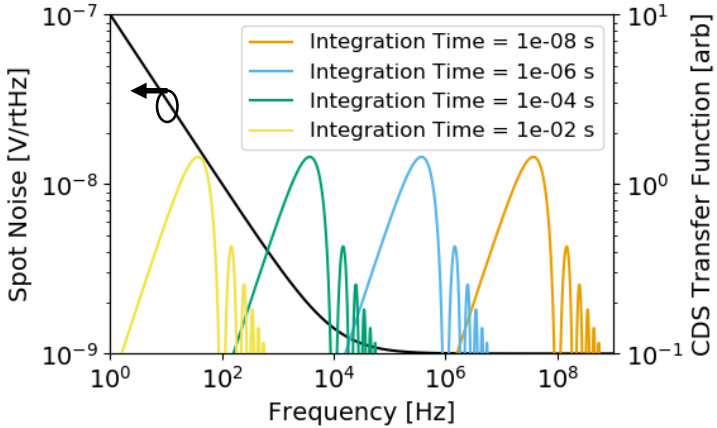
An ASIC to Support Scaling to 28 Gigapixels, MIDNA

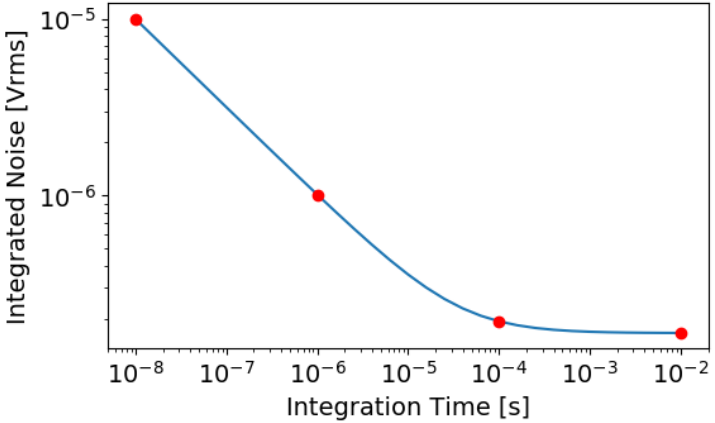
- MIDNA is a prototype cryogenic low-noise skipper-CCD readout ASIC
- It is an enabling technology for the OSCURA dark matter detection project
- Integrates multiple readout channels onto a single chip, replacing numerous costly PCB components and saving valuable physical space
- Operates at 120 Kelvin where COTS devices are not guaranteed to specification



CCDs for Low Noise Imaging

- CCDs have long been the main choice for low noise scientific imaging
- The low noise has been enabled by a combination of integrating the readout for long periods and using correlated double sampling (CDS) [1]
  - Unfortunately, 1/f noise means that there was a limit to the effectiveness of this approach
  - Long integration moved the content of interest to lower and lower frequencies
  - The spreading out of the CDS sampling points reduced the filtering of flicker noise





[1] White et al., "Characterization of Surface Channel CCD Image Arrays at Low Light Levels."

Skipper CCDs for Exceptional Low Noise for Dark Matter Search

- Skipper CCDs and similar technologies enabled the non-destructive readout of the same pixel many times [2]
  - The noise can be lowered by averaging many shorter reads rather than one long read
  - It continues the decreasing noise trend with longer measurement times
- There are still limits to this approach
  - Leakage in the charge transport in the CCD (low)
  - Speed of the various readout stages and clocking
- A skipper CCD has demonstrated the lowest ever, 0.068 e^-_{rms}, noise floor in CCDs [3]
  - Required 4000 read averages at 10 µs/read

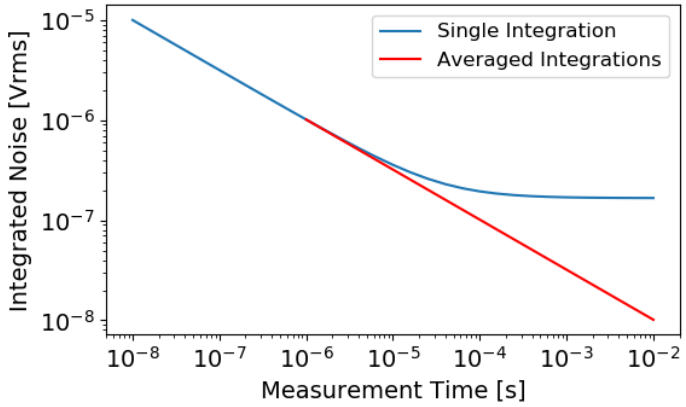
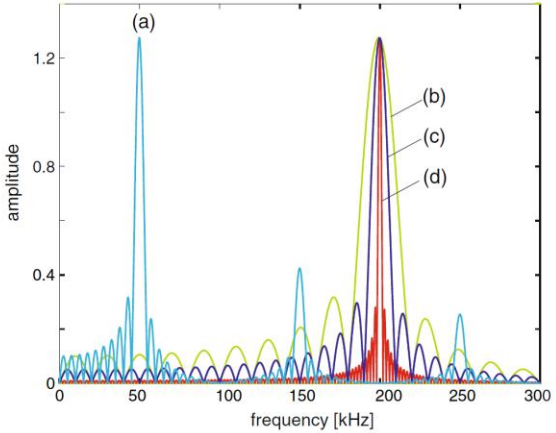


Fig. 8 Frequency response of the Skipper readout system for $T_S = 10\ \mu s$ and $N = 10$ (**a**) and for $T_S = 2.5\ \mu s$ and $N = 10$ (**b**), $N = 20$ (**c**) and $N = 100$ (**d**)

From [3]



[2] Janesick, J.R., et al. "New advancements in charge-coupled device technology: sub-electron noise and 4096×4096 pixel CCDs."
[3] Fernández Moroni et al., "Sub-Electron Readout Noise in a Skipper CCD Fabricated on High Resistivity Silicon."

Midna Prototype Specifications

- Both the CCD and the ASIC will be operated at 120 Kelvin
- Fermilab possesses models for 84 Kelvin for LP CMOS 65 nm transistors
  - The ASIC will be fully verified at 84 Kelvin expecting only minor differences at 120 Kelvin
  - Only verifying for basic functionality at room temperature
- Uses 2.5 V transistors for voltage room
- *The ASIC input referred noise must be less than one third of the CCD output noise*
  - Most difficult and constraining requirement
- 4 channels on prototype
- 3000 e^- dynamic range
- 1 µs min. integration time
- < 6 nV/√Hz input referred noise at 10 kHz

Skipper CCD

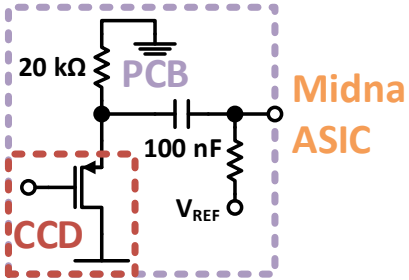
Variable	Value	Unit
Gain	3	µV/e^-
Dynamic range	3000	e^-
White Noise	18e-9	V/√Hz
1/f Noise at 1 Hz	3.95e-6	V/√Hz
1/f Noise exponent	1.3	Arb.

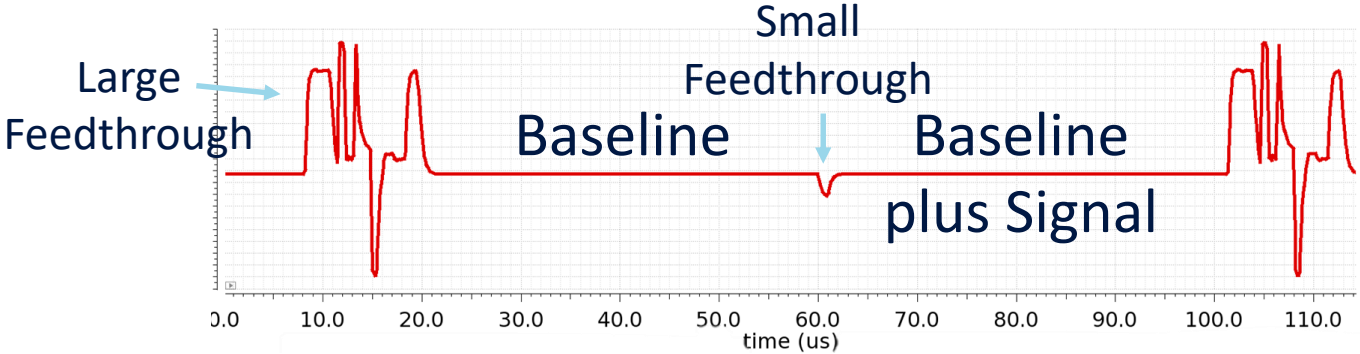
Midna ASIC Specifications

Variable	Min	Target	Max	Unit
Input Amplitude	1		3000	e^-
Input Amplitude	3		9000	µV
Integration Time	1	10		µs
Temperature	84	84	120	K
Input Referred Noise		1/3		CCD
Out. Hold Time		50		µs
Settling Time		50		ns
DC Input	-20		-15	V

Skipper CCD Output Characteristics

- The output of the Skipper CCD is a buried-channel source-follower pFET driving voltage levels
- The transconductance is approximately 200 µS, 4 kΩ output impedance
- The load resistance of 20 kΩ provides the best speed vs. noise trade-off
- The output transient consists of a repeating pattern of large clock feedthrough, the baseline level, small feedthrough, and the baseline plus signal level
- The transient resides on a DC level near -20 V, so it will be AC coupled

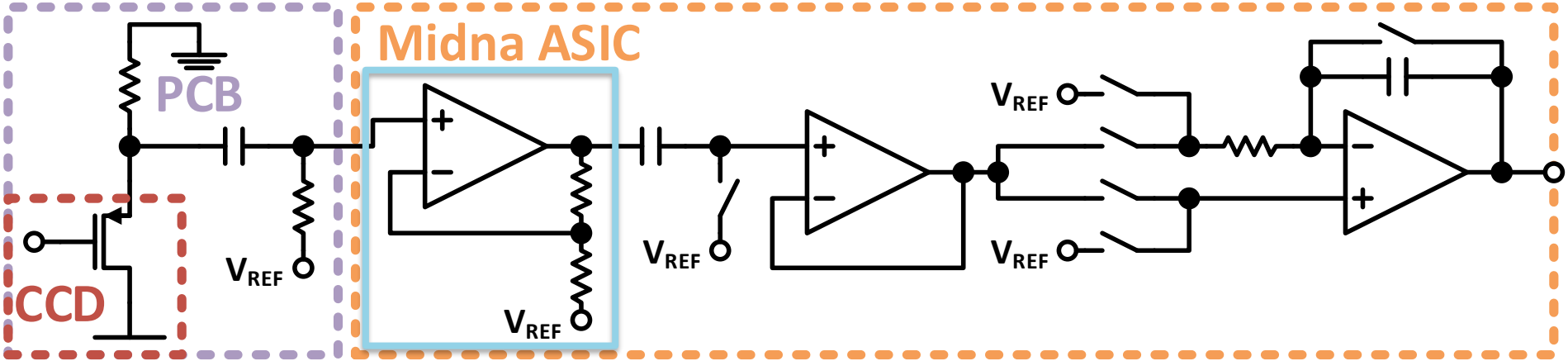




Preamplifier

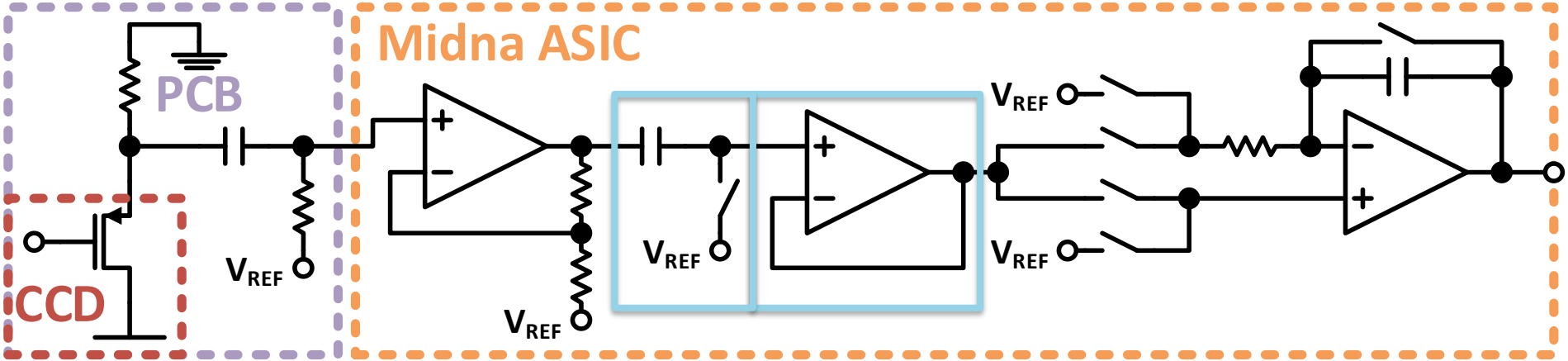
- Largely responsible for noise performance
- Requires large devices and large currents
- It must drive the 100 pF DC restore capacitor and settle within 50 ns
- Uses class AB push-pull output
- Selectable gain of 10 V/V or 20 V/V

Simulated Noise Characteristics:
470 nV/rHz @ 1 Hz
2.04 nV/rHz @ 1 MHz



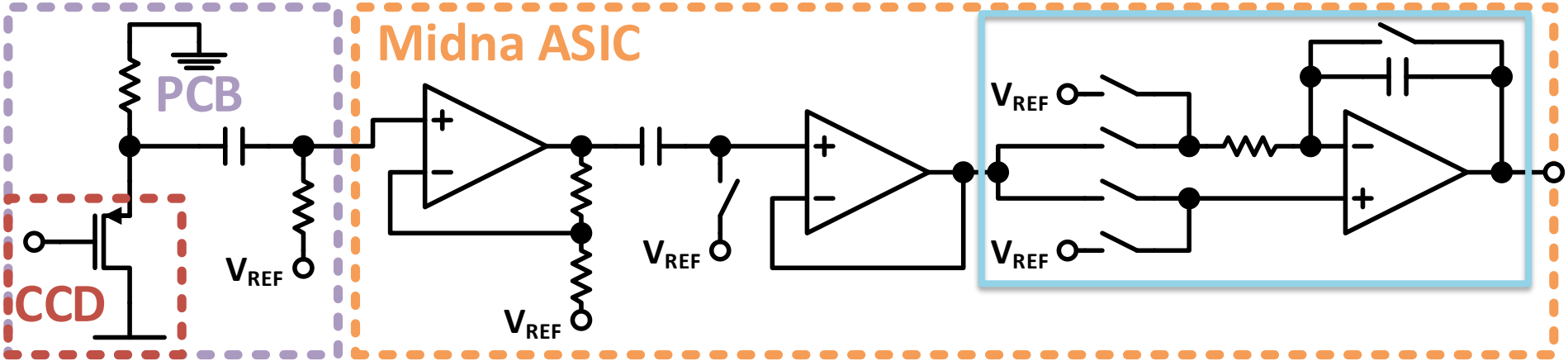
DC Restore and Buffer

- DC Restore ensures the baseline does not saturate the integrator
- Buffer provides the drive necessary for the integrator
  - DC Restore cannot provide DC current



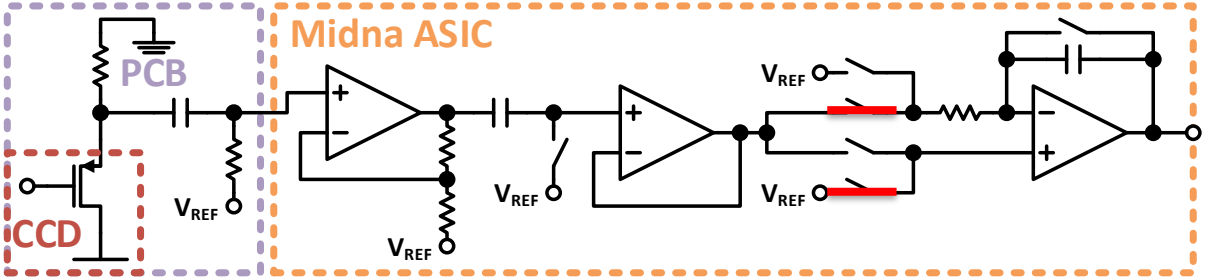
Integrator

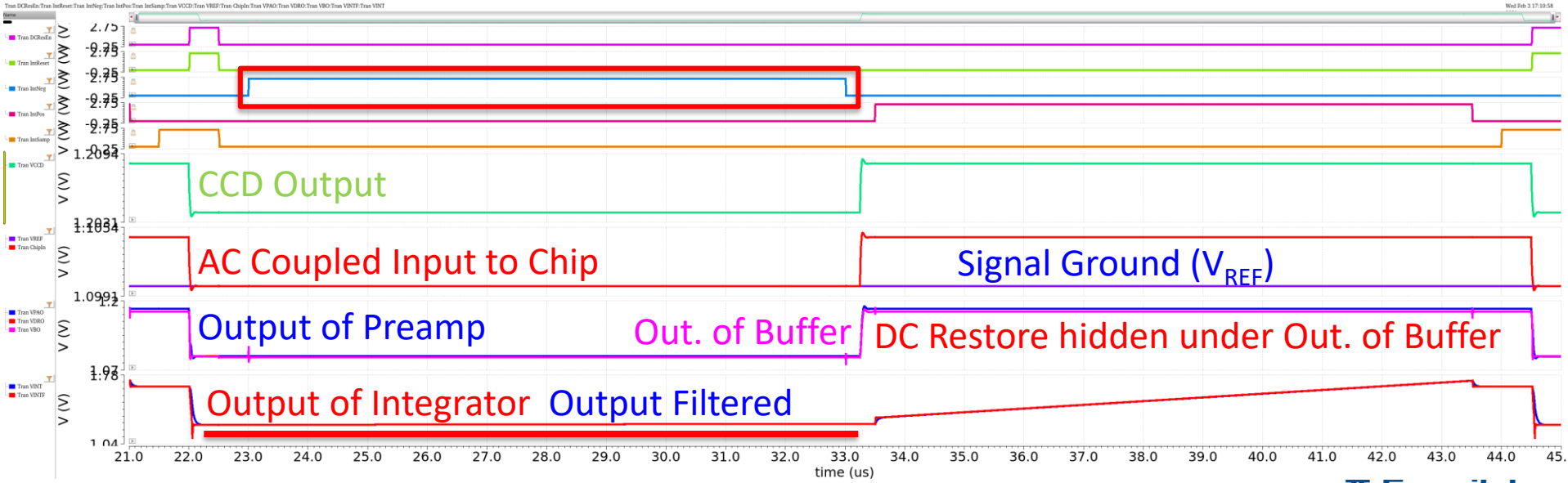
- A switching multi-slope integrator is used to implement CDS and filtering
- It has two gain settings using a switchable resistor
- Four phases: reset, inverting integration, non-inverting integration, and sample



Channel Transient Functionality Simulation

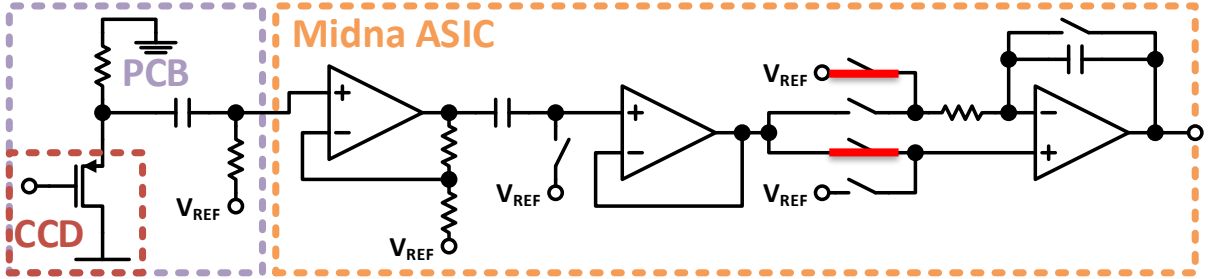
- At 23 µs, Negative Integration of the baseline starts and lasts for 10 µs
- Because the DC Restore shifted the output of the Buffer to V_{REF} there is only a small integration value equivalent to the offsets of the DC Restore, Buffer, and Integrator

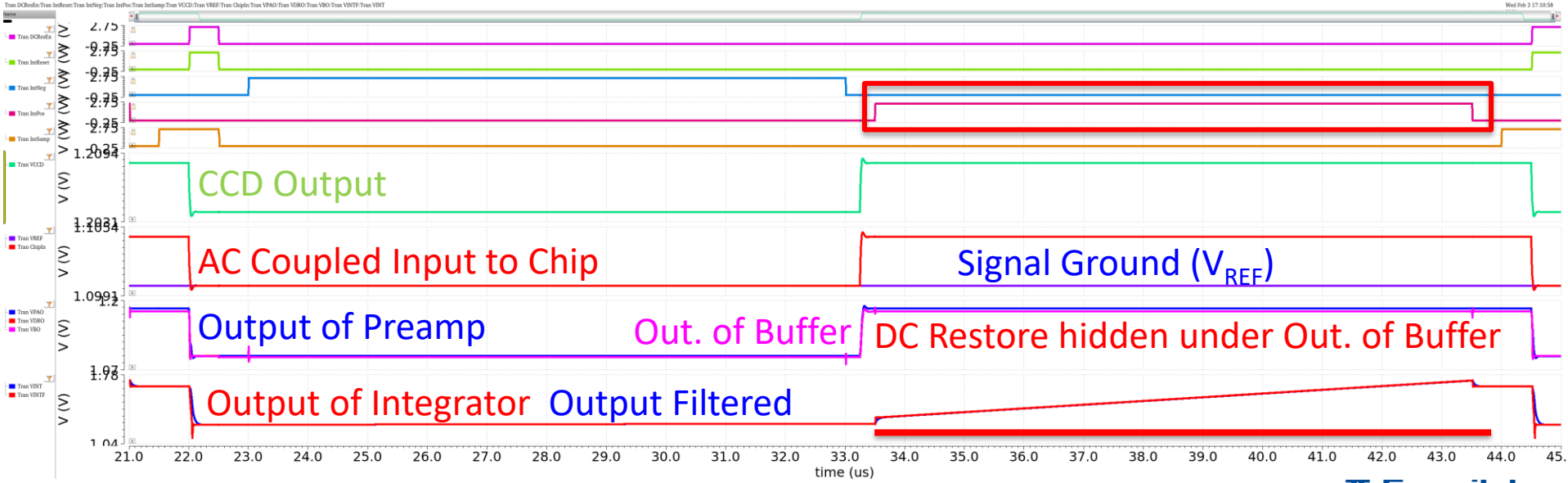




Channel Transient Functionality Simulation

- At 33.5 µs, Positive Integration starts
- The most voltage space is used by the integrator in this phase

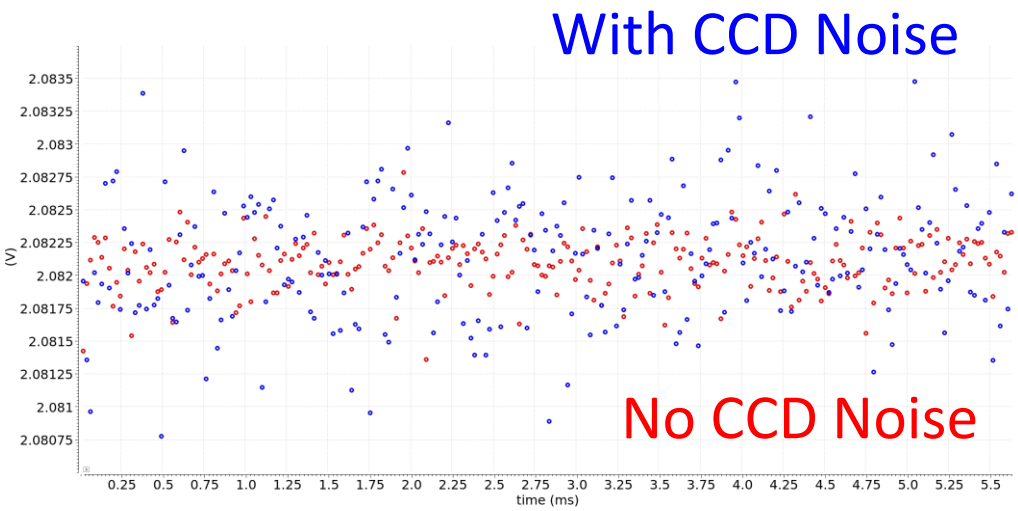




Full Channel Parasitic Extracted Transient Noise Simulation

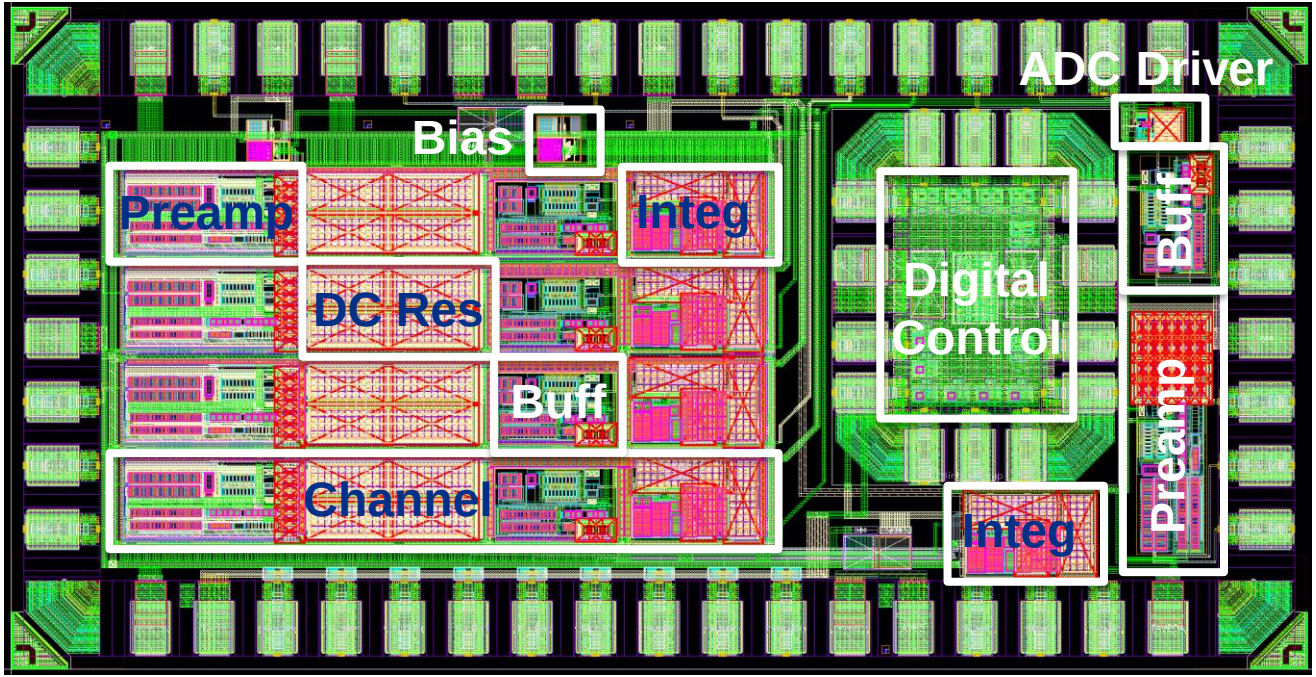
- 256 successive reads in transient noise analysis
  - Noise generated up to 100 MHz
- Output mathematically sampled during third phase of the integrator
- Standard deviation of results gives the integrated output noise
- The noise is referred back using the average output voltage value minus the reference divided by the input height and the CCD sensitivity, 3 µV/e-
- With similar measurement time, this would cut the record noise result in half

Noise	Output [μV_{rms}]	Input Referred [$e\text{-}_{rms}$]
No CCD	198.8	0.61
With CCD	466.5	1.43



Chip Screenshot and Tape Out Structures

- Each channel is about 150 µm x 1 mm
- Chip is 2 mm x 1 mm
- Taped out on March 12
- Four analog channels
- Standalone preamp
- Standalone buffer
- Standalone integrator
- Standalone ADC driver
- Bias mirroring
- Digital control



Midna Performance Summary

- Sub-e^- read noise from channel at 10 µs integration times
- < 6 nV/√Hz input referred noise at 10 kHz
- 3000 e^- dynamic range
- High linearity, R^2-1 = -8.5e-7
- Cryogenic operation down to 84 Kelvin
- Selectable gain:
  - 54.4, 81.6, **108.8**, 163.2
  - Output voltage swing divided by voltage step height
- 4.2 mW per channel

Future Development for Midna

- Supporting 4000 CCDs will require even more on-chip features
- Grow to many more channels to follow the CCD, up to 64
  - Currently limited by cost of readout
- Integrated analog-to-digital converter (ADC)
  - 12 bit, 500 kS/s
- Digital processing of data
  - The ADC combined with on-chip memory enables many averaged reads on chip
  - Improves noise, power, and complexity compared to analog solutions

Thanks!