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A scalable low-noise skipper-CCD readout ASIC in 65 nm LP CMOS

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The MIDNA application specific integrated circuit (ASIC) is a prototype cryogenic skipper-CCD readout chip fabricated in a 65 nm LP CMOS process and intended for the OSCURA dark matter detection project. The MIDNA ASIC integrates four front-end channels designed to interface with the 4000 skipper-CCDs for a 28 gigapixel camera for dark matter detection. Each channel is only 0.156 mm² and achieves an equivalent noise charge of 1 e⁻_{rms} at 20 µs integration time in simulation. With the non-destructive readout capability of skipper CCDs, MIDNA and the skipper CCDs will be capable of sub-e⁻_{rms} noise by averaging samples of each pixel and at the scale required by OSCURA. Each readout channel contains a pre-amplifier, a DC restorer, and a triple-phase integrator. The channel has four gain settings to maximize dynamic range for a variety of CCD charge gains. The minimum integration time is 1 µs. The power consumption is 4.2 mW per channel. The linear dynamic range is 3000 e⁻ in nominal gain. The temperature range is 84-120 Kelvin as required by the skipper CCD, and the input referred noise is less than 6 nV/√Hz at 10 kHz.

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