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Testing Virtual ASICs with Real Data: an Example from CMS timing upgrade

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During the development of new detectors for future experiments or the Upgraded Collider detectors, the ASIC and sensor development often follow parallel paths. This implies that, for the last stages of ASIC development there often exists a significant body of data obtained with high quality waveform sampling that capture the subtleties of real response of the sensors to various particle beams.

Whereas the final validation of the ASIC, before production can begin, requires real "battle testing" of the sensor and ASIC in a test beam setup, the production cycle could be accelerated by an intermediate step where the ASIC simulation models developed as part of the design process are used to analyze quality waveforms captured in pre-existing test beam samples. These waveforms are then treated as input signals to which transfer functions are applied to exhibit the response at various nodes in the ASIC.

In contrast to an input signal model for the simulation, a library of test beam waveforms is more likely to expose subtleties arising from, for example, Landau fluctuations, high rate effects leading to signal pileup, etc.

Although the full blown simulation tools (eg CADENCE in the present example) could be used to analyze a large sample of digitized test beam waveforms, the cost of licenses and the relatively large CPU usage have discouraged this in the past. As an alternative to using lighter weight variants of the commercial packages we illustrate an approach wherein, starting from limited information about the key components in the ASIC, we developed a strategy to probe the transfer functions of a chip (in this case, the TOFHIR2 chip development for the CMS barrel timing layer).
We show that an adequate description can be obtained using a network of Resistors and Capacitors to replicate the transfer functions, resulting in a very efficient code for analyzing real test beam input data to the ASIC.

The events of 2020 shut down operation of laboratories providing crucial test beam facilities and exposed the vulnerabilities of the electronics development cycle in terms of training young engineers and overall impact on large experiments with interconnected subsystem schedules. Going forward, the current approach may also be beneficial in reducing vulnerabilities.

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