R&Ds of ASICs and Optical Modules for Detector Data Communication

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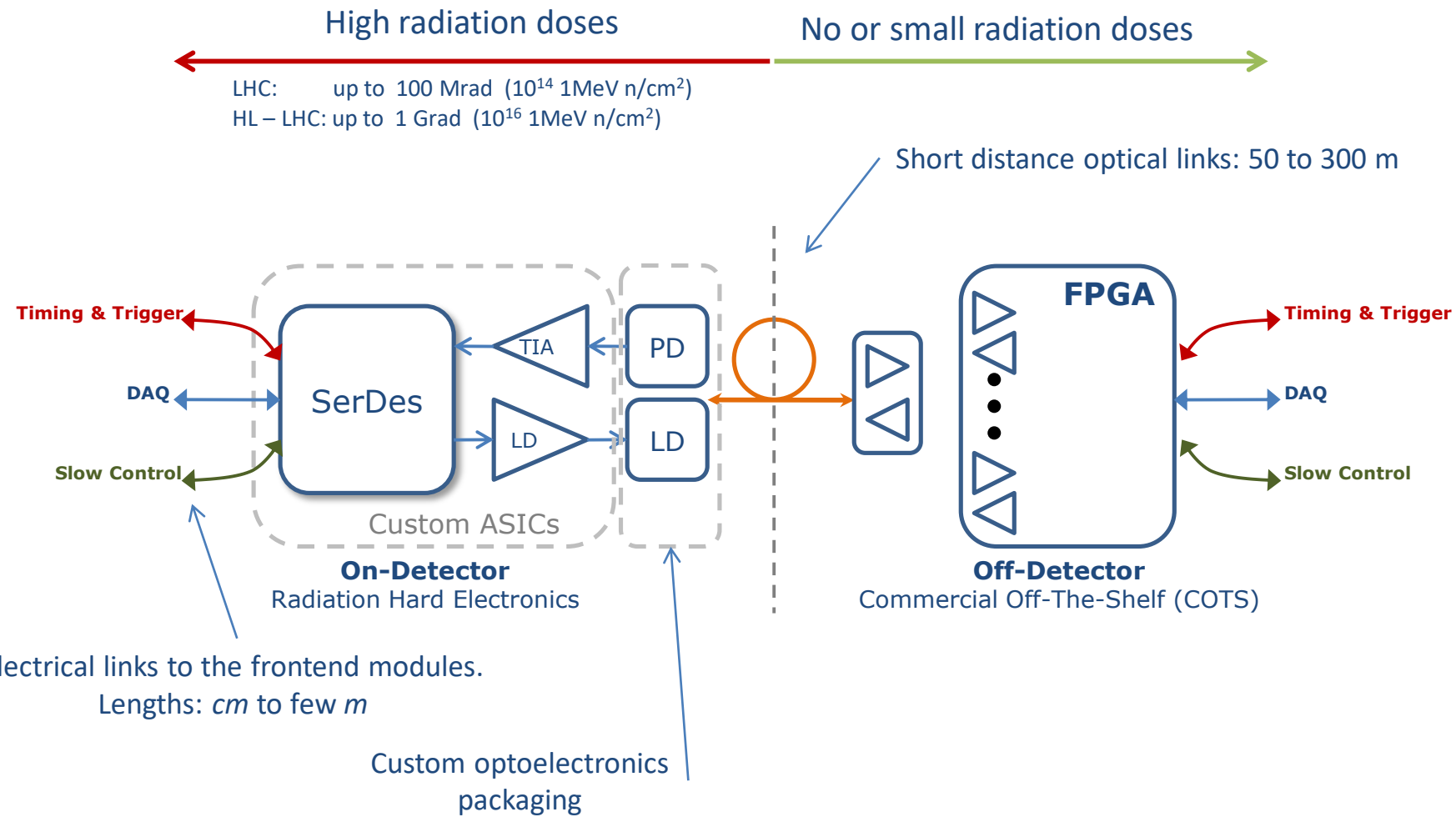
Content

- A very brief overview of ASICs and optical modules we develop/use in the past two decades.
- Going forward what's on the horizon (my understand of it).
- Some R&D at SMU (in collaboration with many others, especially IPAS):
  - GBS20 to push to 20 Gbps per fiber.
  - cpVLAD to cope with extreme use conditions.
  - QTIA to explore ideas that may mitigate the p-i-n diode degradation in radiation.
- Summary.

Today's typical HEP Link Architecture

Challenges:

- Radiation, in both pp and ee machines
- Reliability, especially the link to the detector, and the radiation induced degradation in photo diode.
- High channel/data density and throughput from detector
- Low power, low mass and small formfactor (of the module)



Slide from Paulo Moreira, CERN EP workshop on R&D, 2019/10/24

Looking back two decades*

	Generation/Speeds	(AS)ICs	OMs (Optical Modules)
Current LHC detectors	1**, 1.6 Gbps	G-Link (the only COTS, bipolar) GOL (0.25 um CMOS)	OTx, ORx (COTS based custom modules) SC or ST type of COTS transceiver
Phase-I upgrades	2, 4.8 Gbps	GBTx, GBLD, GBTIA, LOCx2-130 (130 nm CMOS)	VTRx (CERN common project)
	5.12 Gbps	LOCx2, LOCld (0.25 um SOS)	MTx, MTRx (specially for LAr, 6 mm height)
Phase-II upgrades	3, 5.12 /10.24 Gbps	lpGBT, LDQ DLAS10, cpVLAD (65 nm CMOS)	VTRx+ (4 Tx + 1 Rx array) MTx+, MRx+, MTRx+

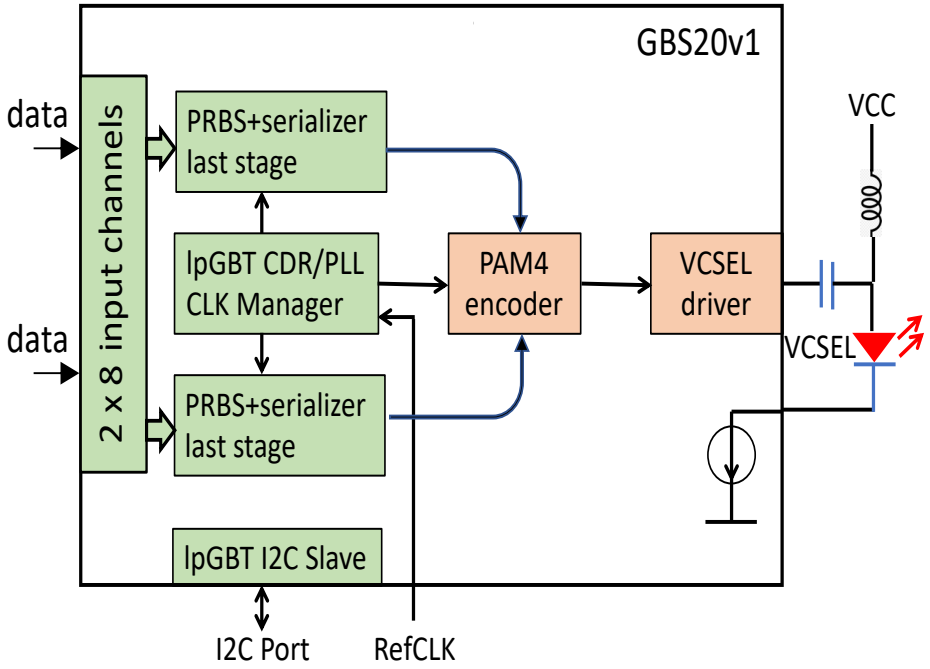
*, the list is not complete. For example, it does not include link through electric cable.
**, there are custom modules in tens of Mbps developed for inner trackers.

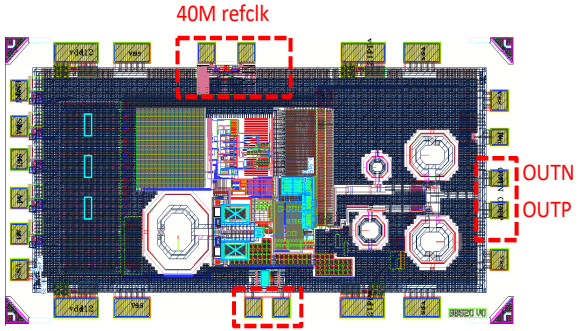
Look forward

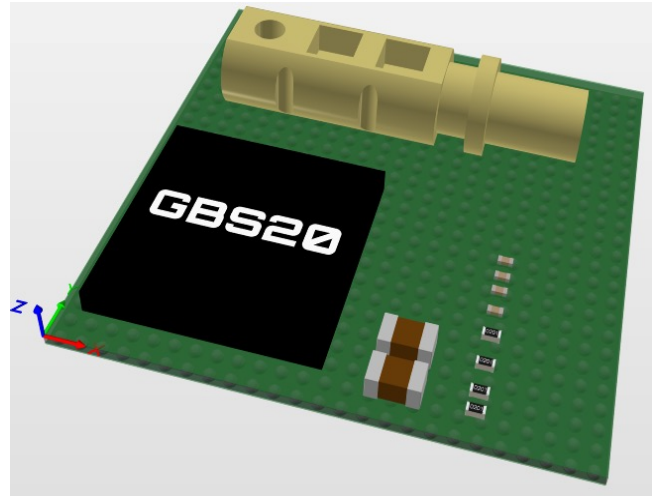
- Not trying to do any advertisement for CERN, but I would like to point out the following developments that I know:
  - CERN EP R&D program and the WG6 on Fast Links: ASICs on high data rates, optoelectronics drivers and low-mass electrical cable transmission; FPGA-based system testing and emulation; Silicon photonics (chip, packaging and system, and next-generation VCSEL-based optical modules). On ASIC, one goal is 28 nm CMOS based 28 Gbps NRZ and 56 Gbps PAM4 transmitters.
  - Task Force 7 reports (March 25, 2021) in the the ECFA Detector R&D Roadmap Symposia will cover ASICs and Links for detector front-end electronics, including data links.
- Some R&Ds on links at SMU.

GBS20

- GBS20 is an ASIC that uses many design blocks from lpGBT (65 nm CMOS), plus a PAM4 encoder + driver, for a data rate at 20.48 Gbps.



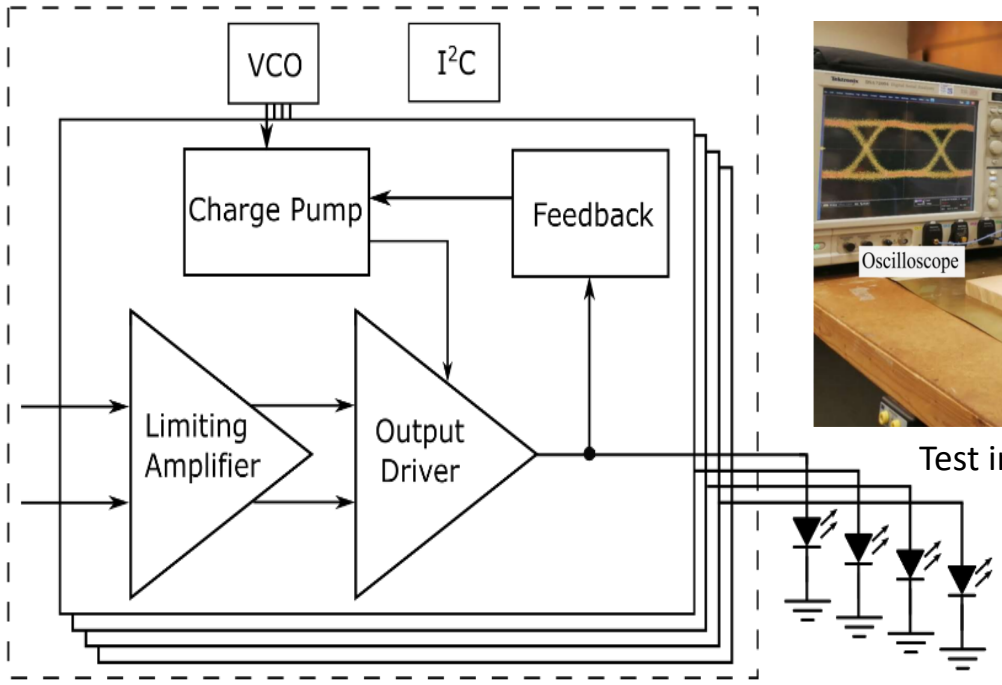


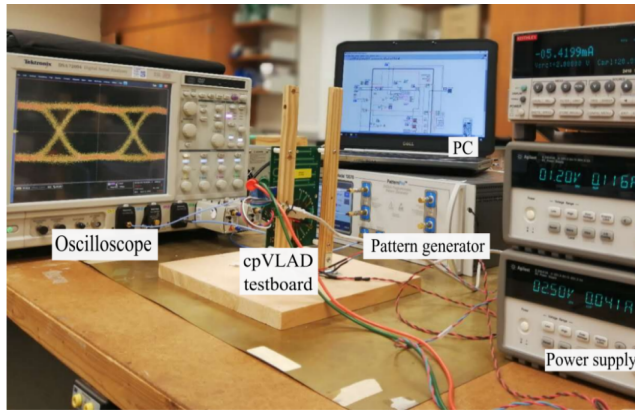


- Test results of the first version reported at RT2020, Tests of the second prototype chips will start in April. Tests provide experience in PAM4 + VCSEL.
- The final goal is to implement the full lpGBT transmitter (and link protocol), and to develop the optical transmitter as a mezzanine, to fit into the lpGBT ecosystem, and to spare system developers the trouble of dealing with fast (10G) PCB layout.

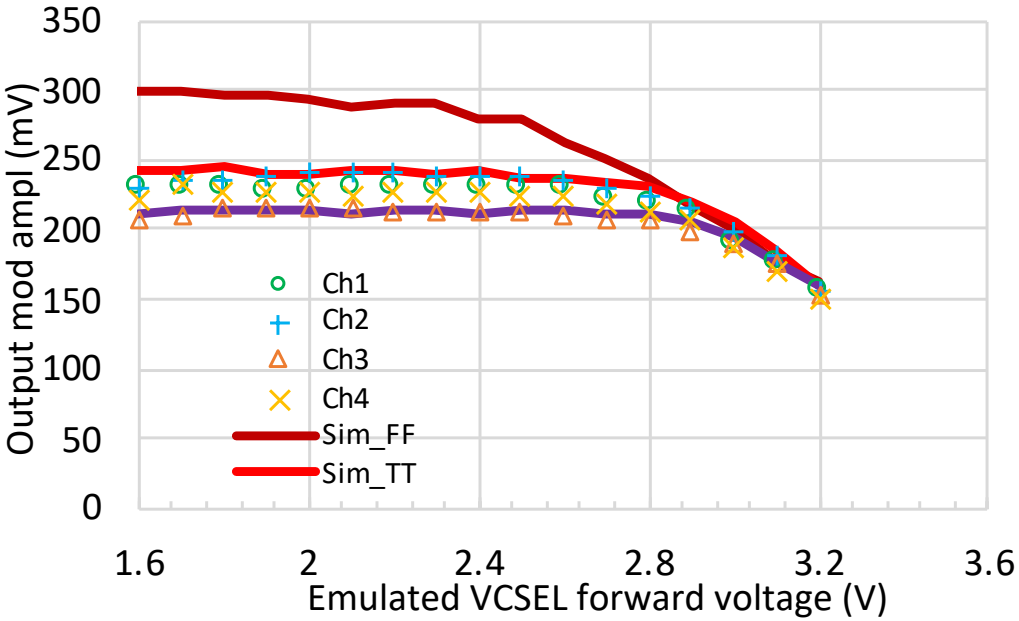
cpVLAD

- cpVLAD is a 4 lane, 10 Gbps each, VCSEL array driver developed to address the issue that VCSEL forward voltage increases under ultra high radiation and low temperature. This increase will cause problem of array optical transmitters in the current 1.2 and 2.5 V powering scheme.





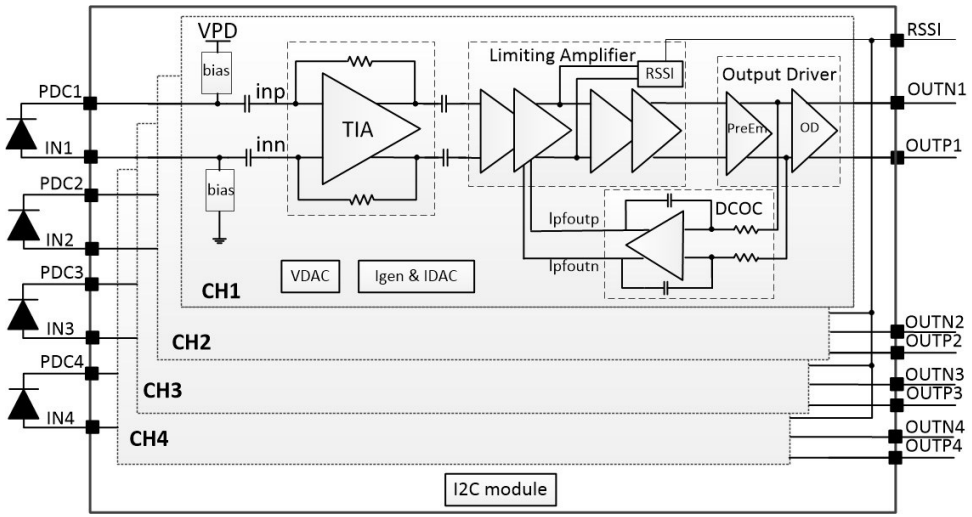
Test in collaboration with CERN



- This design has been fully tested and reported (TWEPP and JINST). It can be used in future development of array optical transmitters for applications in extreme conditions.

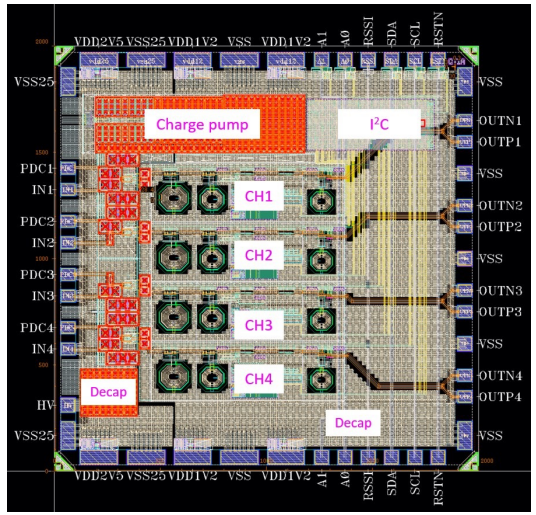
QTIA

- QTIA is a 4 lane array p-i-n diode (GeAs or InGeAs) TIA + LA. The speed is selectable to be 2.56 and 10 Gbps. Different diode biasing schemes, with one that has a charge pump to raise the bias voltage, are designed in the 4 channels to search for mitigation to radiation induced performance degradation of the diodes.



Other than testing the TIA + LA, we will test different biasing condition to the diode to mitigate responsivity loss due to radiation.

- ❑ CH1: charge pump + PD bias UP & Down
- ❑ CH2: (VDD25) + PD bias UP
- ❑ CH3: (VDD25) + PD bias Down
- ❑ CH4: HV (external) + PD bias UP & Down



- Tests of the prototype chips will start in April. Results will be reported to the community in due time.

Summary

- We progressed from 1 Gbps (15 – 20 yrs ago) to 5 Gbps (now) and are reaching 10 Gbps (to be installed in detectors in a few years) for detector data transmission.
- Many ASICs and Optical Modules have been developed, and the community is adapting to the lpGBT ecosystem.
- There are plans of R&Ds to reach 28 Gbps NRZ and 56 Gbps PAM4, through 28 nm CMOS.
- In collaborations with IPAS, SMU is carrying out R&Ds on a few ASICs and optical modules (not reported in this talk) to address issues in detector data transmission, and to try to reach 20 Gbps using PAM4 using the 65 nm CMOS.