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R&Ds of ASICs and Optical Modules for Detector Data Communication

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In HEP experiments, detector data communication is one of the key R&D areas. This is especially important when the operating environments inside the detectors preclude the use of COTS in these link systems. ASICs and optical modules are being developed to meet the challenges of detector upgrades in the LHC. This effort has been led by the CERN common projects GBT/lpGBT and Versatile Link/VL+. The GBT ASICs and the VTRx optical module are key components for optical links at 5 Gbps per fiber. The lpGBT ASIC and the VTRx+ optical module reach 10 Gbps per fiber for detector data transmission (the so-called up-link). The bandwidth of the data communication (clock, configure and control) to the detector (the down-link) is reduced to 2.56 Gbps (compared with GBT) to save power. What are also studied in these common projects are link protocols, correction schemes for transmission errors, optical power budgets, passive components such as fibers and connectors to meet the special operating environments inside HEP detectors. Moving forward, CERN has held workshops on future R&D programs for data rates as high as 56 Gbps with 28 nm ASIC technology and PAM4. While these common projects and collaboration among many institutions are efficient and effective, ideas and R&D from individual university groups should also be encouraged and supported. We will report on two R&D efforts: GBS20, the ASIC that builds on many design blocks from lpGBT (hence 65 nm technology) plus a PAM4 encoder and driver, to reach 20 Gbps per fiber. Prototypes of GBS20 will be available for test in the near future; cpVLAD, the array VCSEL driver that has an embedded charge pump to automatically raise the driving voltage inside the chip to above 3 V with a 1.2 and 2.5 V external power supply system, for applications in extreme conditions where the VCSEL forward voltage may increase due to accumulated radiation damage. To the best of our knowledge both PAM4 and the charge pump for high-speed circuits are the first attempts in HEP ASICs. GBS20 is in prototype stage and will provide valuable experience to the community when it moves to the more expensive 28 nm technology for 56 Gbps data rate. cpVLAD is fully developed and complete as an R&D program. Looking a few steps further forward, we are exploring the idea of using a charge pump in an array amplifier ASIC for p-i-n diode in the down-link channel to address several issues including radiation induced degradation of signal to noise ratio. After this we would like to address the SEE issue related to a p-i-n diode to recover long consecutive bit errors at hardware level with a special TIA and module design. While we continue our participation in the highly efficient and effective CERN led common projects and R&D programs, it is our hope that centers of excellence in universities and national labs will not be starved out for near term gain in specific projects. Long term investments immune to the success or failure of specific and ad-hoc proposals will establish a healthy foundation for the whole HEP program.

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