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Towards Edge Computing: Co-Design for Machine Learning based ASICs for Scientific Applications

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In a multi-channel detector readout system, waveform sampling, digitization and transmitting bits to the data acquisition system constitutes a conventional processing chain. Quantities, such as time-of-arrival and signal magnitude, i.e deposited energy, are estimated by fitting analytical models over the acquired digital data, hence enabling the extraction of signal starting time, peak amplitude, and more. These tasks could be carried out through machine learning algorithms: their implementation in the front-end ASIC comes with enormous benefits, especially when the analytical response signals are not fully known or the registered waveforms suffer from the imperfection of practical implementations. This approach significantly reduces the bandwidth of data throughput, thereby reducing the overall cable count in experiments.

Initial studies are focused on various neural networks, their implementation and training with test waveforms typical for silicon sensors. The most accurate model is further optimized in terms of layers and neurons while still targeting prediction with acceptable accuracy. The translation of machine learning algorithms to transistor level circuit not only requires new design methodologies but also the introduction of novel devices such as memristors, needed to reduce the overall memory footprint and total power dissipation. In this workshop, we would like to present the status of this new research and development initiative with a final goal towards edge computing in scientific applications.

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