



Low noise, low jitter cryogenic amplifier for superconducting nanowire detectors

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Outline

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 - HBTs cryogenic performances
- Cryo LNA Design
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 - Simulation results
- CMOS test structure
- Measurements
 - Cryogenic probe station
- Superconducting Nanowire Detectors for the EIC
- Conclusions

Superconducting Nanowires Detectors

As PHOTON DETECTORS:

- Highest performing detectors available for time-correlated single photon counting from the deep UV to the mid-infrared
- Demonstrated detection efficiencies as high as 98% at 1550 nm
- Timing jitter below 3 ps
- Effectively zero dark count rates
- Intrinsic photon number resolution
- Maximum count rates exceeding 1 Gcps in arrays

As PARTICLE DETECTORS:

- Can have high segmentation (~10um "pixels")
- Can be truly edgeless detector (important for beam monitoring)
- Operation in high magnetic field (5T)
- Inherently radiation hard



Exploited for photon detection (classical and quantum optics and communication)

Unique capabilities for farforward detectors that operate close to the beam (high T, high radiation, high segmentation)

NECQST: Novel Electronics for Cryogenic Quantum Sensors Technology

- Fermilab: D. Braga (PI), F. Fahim, C. Peña
- Georgia Tech: J. D. Cressler (Co-PI), H. Ying
- JPL: M. Shaw (Co-PI), B. Korzh
- Caltech: M. Spiropulu, S. Xie



Hanbin Ying (Victor), PhD student

Pilot QuantISED grant for the design of a cryogenic (4K) Low-Noise Amplifier (LNA) ASIC:

- optimized for low-jitter readout of SNSPDs
- using state-of-the-art, commercially available SiGe BiCMOS platform: path to high-channel count ASIC with low noise amplifier and signal processing
- Targets high-speed quantum networks (e.g. FQNET, INQNET), as well as classical optical communication.







Jet Propulsion Laboratory California Institute of Technology



LNA and detector setup

- Differential input, DC-coupled to minimize jitter
- Input and output transmission lines (50 Ω)
- 4K stage allows good thermal lift and noise performance





SiGe Heterojunction Bipolar Transistors (HBTs) at cryogenic temperatures

- Unlike conventional bipolar transistors, when cooled SiGe HBTs exhibit **improved frequency response**, current gain, noise, bandwidth, output conductance and other performance metrics.
- **BiCMOS** (SiGe HBT + Si CMOS) platform **ideal mixed-signal technology** that marries high-performance SiGe HBTs for analog, RF, and microwave circuits, with Si CMOS to support highly-integrated system functionality.
- Fabricated on large wafers (300 mm) at **high yield** and **low cost** using conventional silicon processing techniques and silicon economy-of-scale.
- SiGe HBTs cooled to temperatures as low at 70 mK demonstrated operability for a variety of interesting circuit designs (gain of 2000 at 100 mK at only a few μW dissipation).
- At sub-K, the amplification principle becomes fundamentally quantum mechanical in nature, as tunneling becomes the dominant transport mechanism. Constant operation across temperature below ~7K.

H. Ying et al., "Operation of SiGe HBTs Down to 70 mK," in IEEE Electron Device Letters, vol. 38, no. 1, pp. 12-15, Jan. 2017.

Timeline

Relatively long lead time for this process (compared to CMOS)

- LNA V1 & V2 (+ CMOS test structure) taped out in Nov 2019, received in Aug 2020
 - Preliminary probe measurements
 - Not possible to use attenuator for noise measurement
- May 2020 tapeout with LNA V3, received in Nov 2020
 - LNA V3 designed with improved cryo HBT model (including series cap and attenuator for onchip noise measurement)
 - Manufacturing error: all dualMIM shorted on wafer!
 - Foundry no-cost respin: started Dec 2020, chips delivered at the end of Feb 2021
 - Cryogenic setup does not allow differential testing: single ended measurements compared with simulation
 - Populated board shipped to Caltech for cryogenic testing with SNSPD (this week)

HBT Cryogenic Modeling

- HICUM L0 compact model from LHe measurements
- Good DC bias fit for IC = 100uA~10mA
- Good AC fit for VCB > -0.5V
- Minimum noise from one device is around 7 K

HBT cryogenic modeling (4K)

- $f_{\scriptscriptstyle T}$ and transit time match well with data in the desired operating region
- S-parameters match well

• Input DC-coupled

- Differential in and out
- 50 Ohm input and output matching over BW
- BW: 0 6.5 GHz
- Power ~ 10 mW
- Gain >20 dB
- Noise Temperature ~ 10-15 K
- Low jitter

3 versions prototyped:

- V1: BW 0 6.5GHz
- V2: AC coupling between two stages with 0.5GHz low cutoff.
- <u>V3</u>: BW 0 6.5GHz. Improved cryo models wrt V1.

Performance (simulation)	V1	V2	V3
Gain (dB)	24	23	24
Match Bandwidth (GHz)	DC - 6.3	0.5 - 8	DC – 6.5 (S11)
Noise Temperature (K)	12 (at 7 K)	105 (at 233 K)	10K
Power (mW)	12.5	12	8
FoM ₁	47	5.12	85
FoM ₂	296	46	375
DC-coupled	Yes	No	Yes

 $FoM_1 = Gain_{dB}/(NF_{linear}-1)/Power_{mW}$

 $FoM_2 = FoM_1^*BW_{GHz}$

Low Noise Amplifier Performance (simulation)

• Power = 7.7 mW, BW (matched) = 4.5 GHz (S22), 6.5 GHz (S11)

• DC-coupled differential LNA

Simulated Performance

- Simulated at 12 K
- SNSPD current = 10uA (larger --> better)
- Max SNSPD firing frequency: 1GHz (assuming 2nH/2kΩ impedance)

Prototype taped out in Nov 2019

Circuit Description:

- Low Noise Differential HBT Amplifier designed for low jitter and low power consumption (HBT model extracted at 4K)
- CMOS test structure for process characterization
 - Ring oscillators
 - Individual CMOS devices for 4T measurement
 - Four content-addressable matrixes of 200 devices each (n, p dgn, dgp) for 3T measurement and mismatch characterization

Area (mm²): 2 x 2.5

Process: 4th generation SiGe BiCMOS SiGe HBT NPNs: Ft: 300GHz Fmax: 360GHz BVCEO: 1.65V BVCBO: 5.2V Verified for operation at 4K 90nm CMOS: 1.2V core 2.5V/3.3V dual gate N3 isolation 9 levels of Cu BEOL metal

RoomT and cryo testing

5x5 cm Al2O3 substrate (thermally conductive)

- 1. RoomT probing of LNA
- 2. Cryoprobing of LNA
- 3. roomT board test
- 4. Cryoprobing of board

Smoke test (one side terminated)

RoomT setup (one side terminated)

Measured S-Parameters

- Probed at 25 K, one-side terminated on-chip
- VCC=1.5V, IB1 = 1mA, IB2 = 12uA/24uA

Measurements

Simulations

eRD28: Superconducting Nanowire Detectors for the Electron Ion Collider

State-of-the-art applications for superconducting nanowire detectors identified in the **EIC Yellow Report**:

- **Compton Polarimeter:** High segmentation and high rate to extract beam polarization.
- Far-forward Roman pot detectors: 35m or more from the interaction point. Can leverage magnets as extreme forward spectrometers.
- Integrating detectors inside the cold bore of superconducting magnets: provide tracking in regions of high magnetic field. Detector can run on magnet's cooling system.
- Front portion of the Zero-Degree Calorimeter: excellent position and timing resolution, high radiation hardness and proximity to superconducting magnets.
- Measurement of the luminosity: requires a detector for brem photons in the very backward region. Integration within magnets removes main challenge of having sufficient acceptance through the machine to the detector.

ASIC development in coordination with Argonne's Medium Energy Physics group (W. Armstrong). See Tomas Polakovic's talk next week: <u>https://wiki.bnl.gov/conferences/index.php/March_2021</u>

Multichannel ASICs for Superconducting Nanowire Detectors

For both photon and particle superconducting nanowire detectors: multichannel front-end ASIC

- Low noise amplifier
- Comparator/ADC
- Fast time tagging to exploit detector timing performance
- Backend data processing + high speed links

Proposed multichannel ASIC

Concept of a superconducting nanowire Roman Pot detector (FPGAs or data concentrator ASIC depending on rates)