



Contribution ID: 183

Type: not specified

## Low noise, low jitter cryogenic amplifier for superconducting nanowire detectors.

*Thursday, March 18, 2021 2:20 PM (20 minutes)*

We present the development of a cryogenic Low-Noise Amplifier (LNA) for the readout of Superconducting Nanowire Single Photon Detectors (SNSPDs). The integrated circuit operates at 4 K and is based on fourth-generation heterojunction bipolar transistors from a state-of-the-art, commercially available SiGe BiCMOS platform, which allows large scale integration and economy of scale. Target specifications for the fully differential LNA include  $>20$  dB gain,  $\sim 6$  GHz BW,  $\sim 10$  ps jitter, and  $<10$  mW/channel. We discuss cryogenic modeling of the devices, design and test results of the prototypes (AC and DC coupled), the latest received in Feb 2021. The project is a collaboration between Fermilab, Georgia Tech, Caltech and JPL. The target application is low-noise, low-jitter single photon detection for high-speed quantum networks. The scalability of this technology, however, coupled with the availability of small feature size CMOS transistors on the same die, provides a path for the integration of a large number of low-noise, fast front end readout amplifiers, together with low-power digital backend logic for digital signal processing; thus enabling large, multi-Gbps SNSPD arrays for photon and particle detection, with direct application to QIST, HEP and NP programs.

**Primary authors:** BRAGA, Davide; HANBIN, Ying (Georgia Institute of Technology)

**Co-authors:** KORZH, Boris (Jet Propulsion Laboratory); PEÑA, Cristián (Fermilab); FAHIM, Farah (FERMILAB); CRESSLER, John (Georgia Institute of Technology); Prof. SPIROPULU, Maria (California Institute of Technology); SHAW, Matt (Jet Propulsion Laboratory); XIE, Si

**Presenter:** BRAGA, Davide

**Session Classification:** Readout and ASIC

**Track Classification:** Readout & ASICs