Custom Electronics and the Front-End Board of the ATLAS LAr Calorimeter Readout for the HL-LHC

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on behalf of the ATLAS HL-LHC LAr Upgrade group

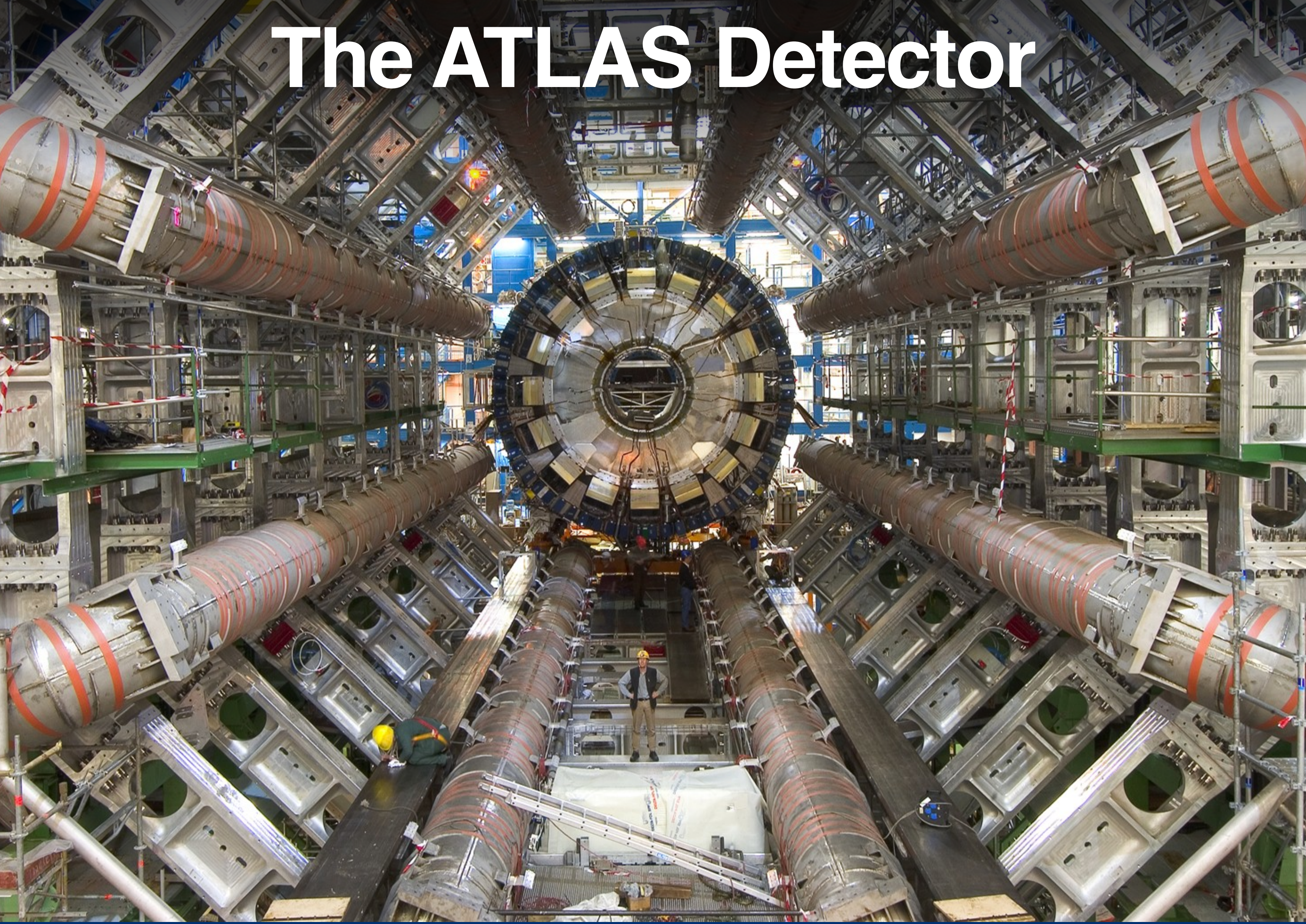
22 March 2021

CPAD Early Career Plenary

Nevis Laboratories
Columbia University

ATLAS EXPERIMENT

The ATLAS Detector



The ATLAS Detector

- Two calorimeters: **electromagnetic (LAr)** + hadronic (**LAr** + scintillating tiles)
- Readout electronics system samples calo cells at LHC frequency of 40 MHz and sends a digitized pulse off the detector

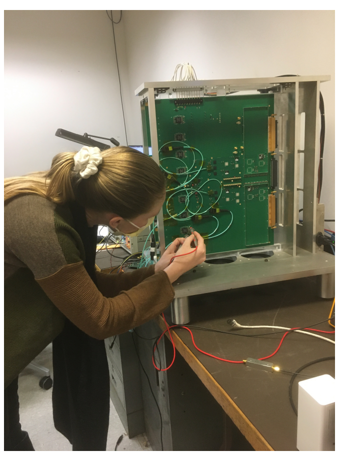
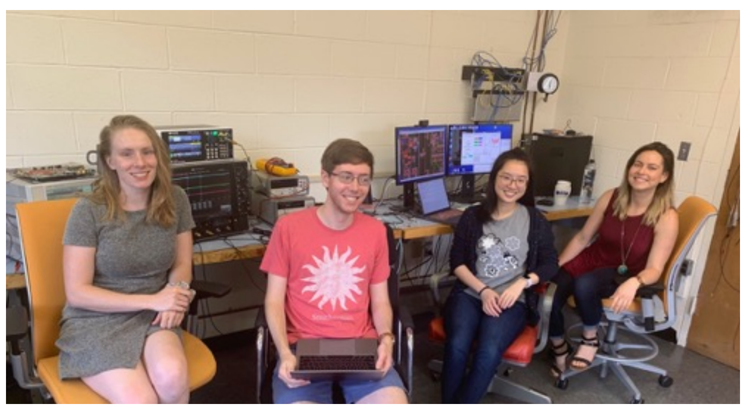
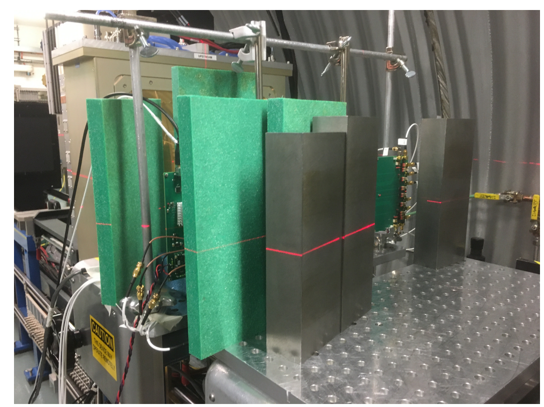
- **High Luminosity LHC (HL-LHC) in ~2025:**
  - Up to 7x design luminosity (~200 simultaneous collisions) to give better handle on very rare new physics processes

- LAr calorimeters themselves are expected to operate reliably throughout HL-LHC
  - However, need to **replace all front-end/off detector electronics** (mainly to provide full calo info for more powerful trigger decisions while handling increased lumi/rates)

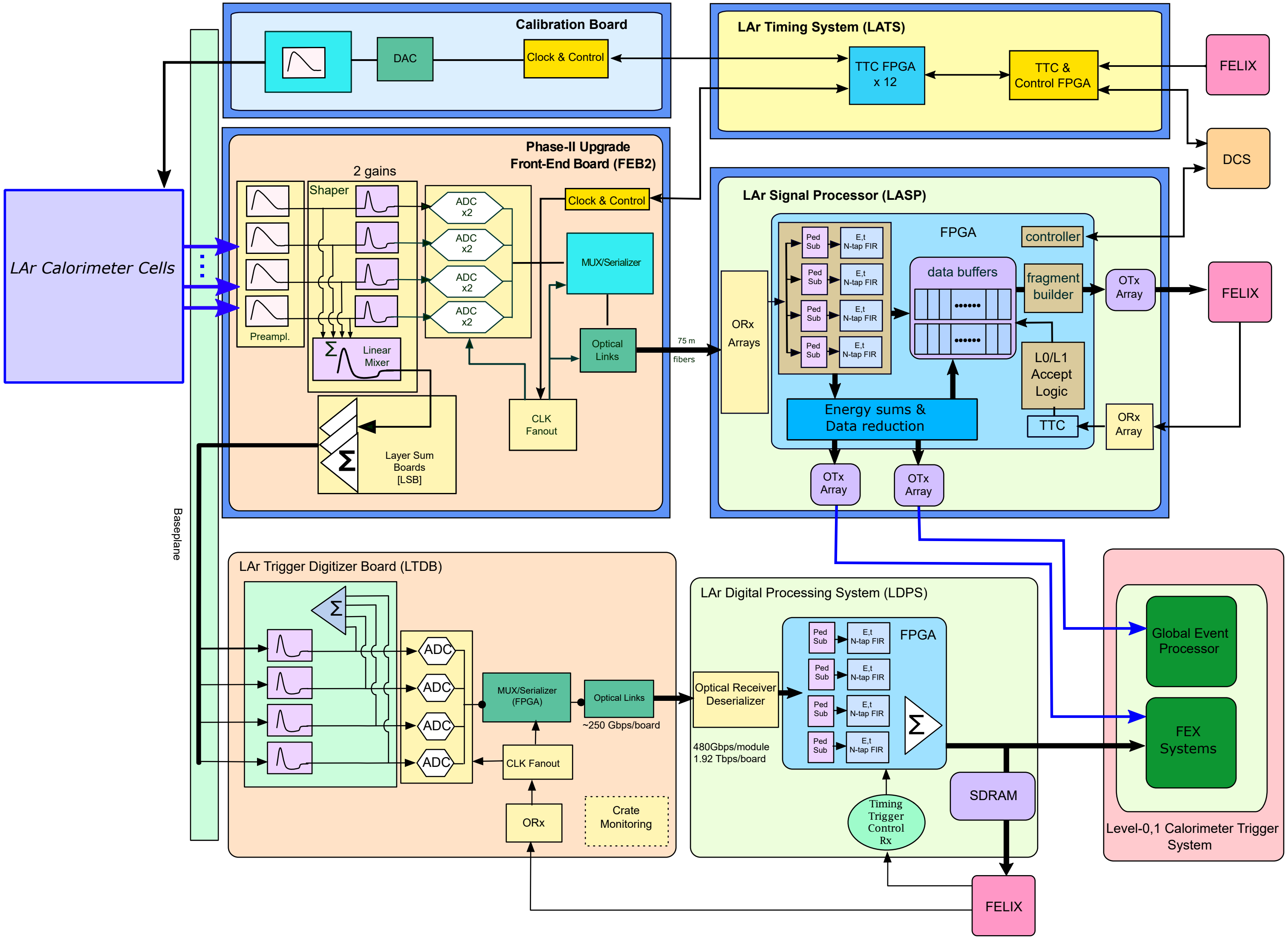
ATLAS LAr Calorimeter Upgrade

- **Requirements:** performant for 10 years of HL-LHC/4000 fb^{-1}
  - Wide dynamic range: 16 bits
  - Quantization noise < intrinsic LAr resolution (10% / $\sqrt{E}$ + 0.7%)
  - Mitigate effects of systematic due to gain intercalibration ($H \rightarrow \gamma\gamma$)
  - Per-mille linearity at EWK scale
  - Radiation tolerance: TID (12.9×10^{2} Gy), NIEL ($4.3 \times 10^{13}\ n_{eq}/cm^{2}$), SEE ($10.5 \times 10^{12}\ h/cm^{2}$)

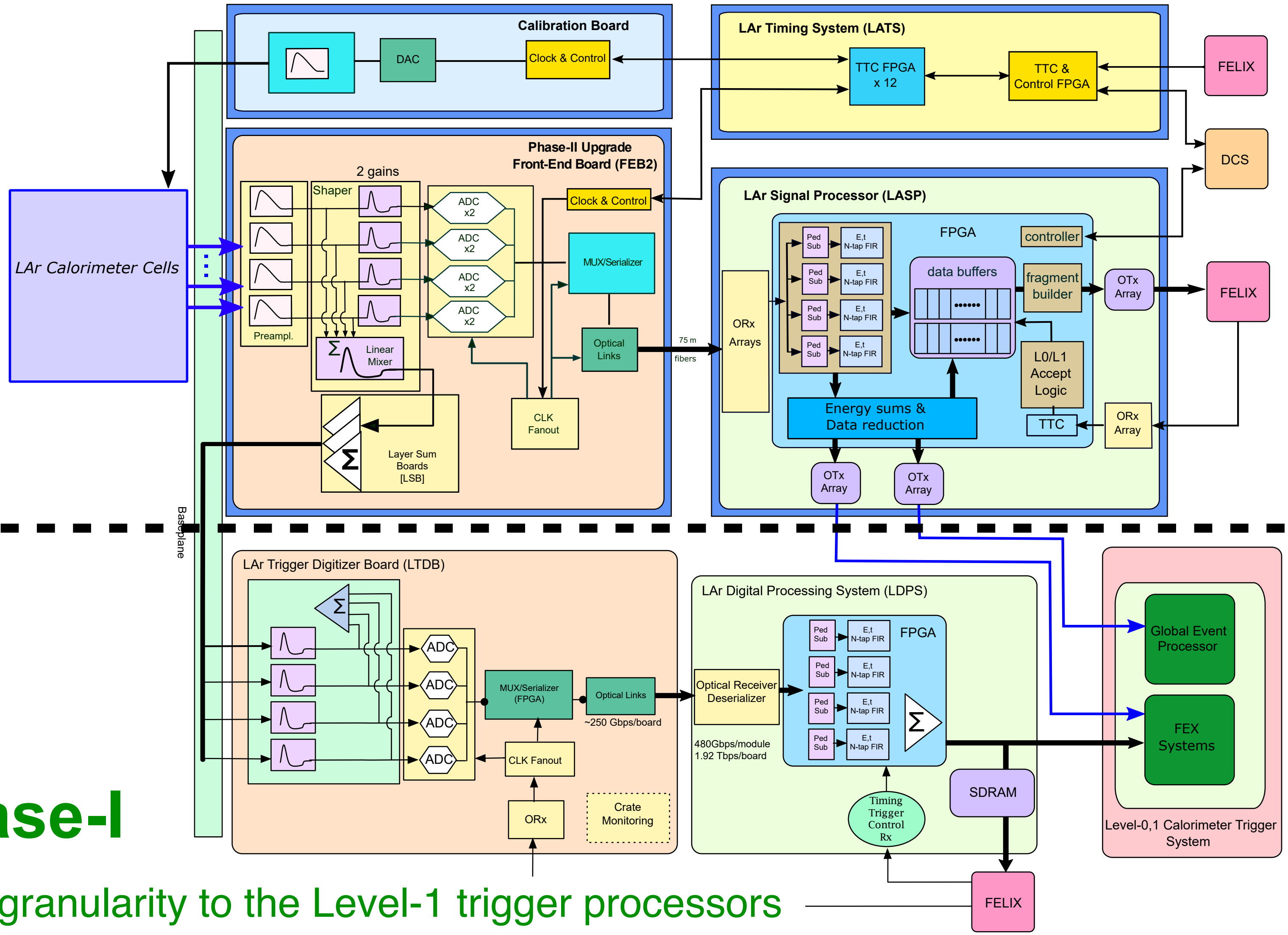
- Read out *entire LAr calorimeter* at 40 MHz LHC bunch crossing frequency: data rate = 40 MHz x 16 bits x 2 gains x **128 chans** x 1524 boards **= 250 Tb/s!**

ATLAS HL-LHC LAr Readout



ATLAS HL-LHC LAr Readout



Installation ongoing ✔

Phase-I

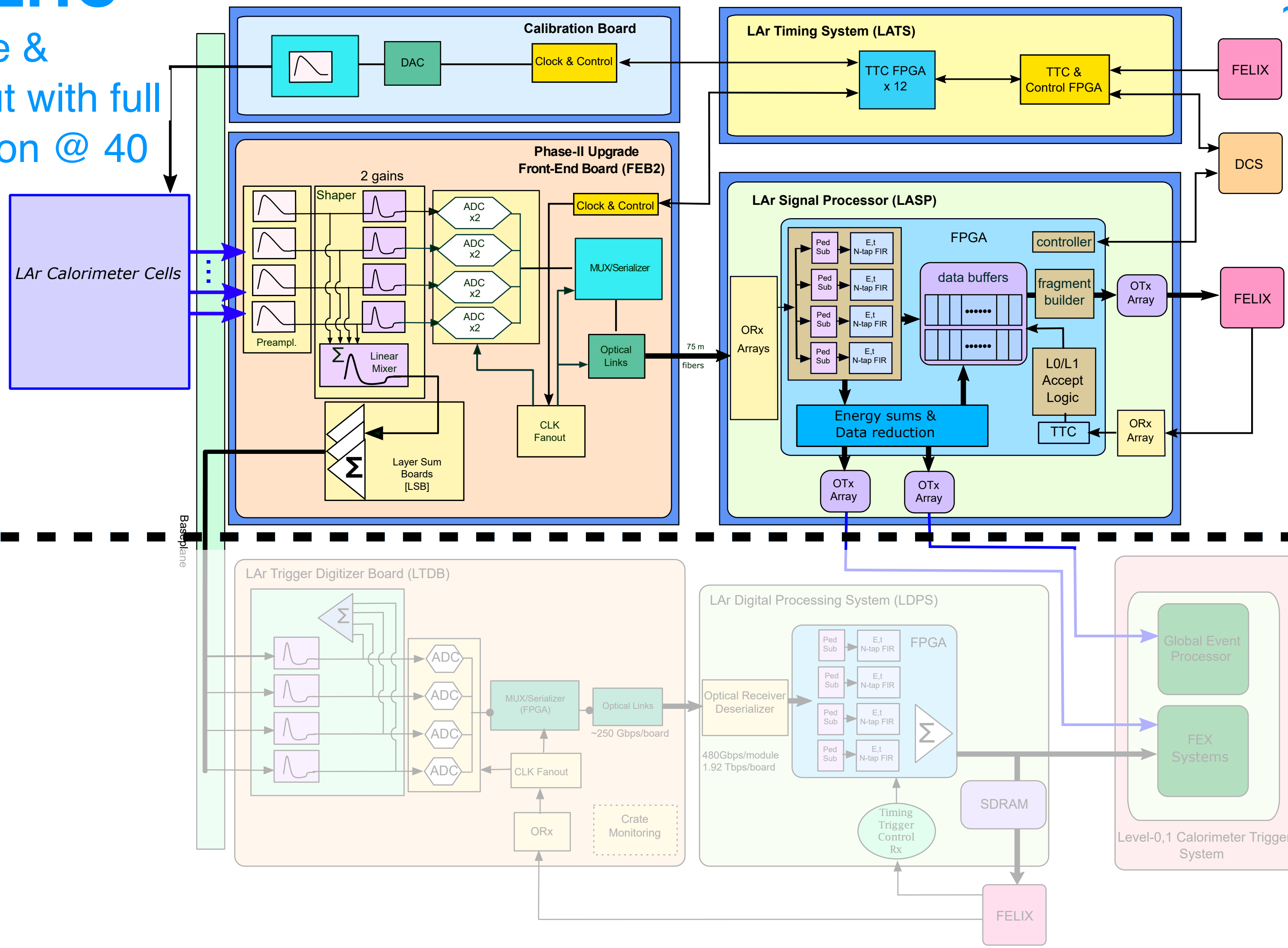
Finer granularity to the Level-1 trigger processors

ATLAS HL-LHC LAr Readout

HL-LHC

Digitize & readout with full precision @ 40 MHz

Installation ~2025



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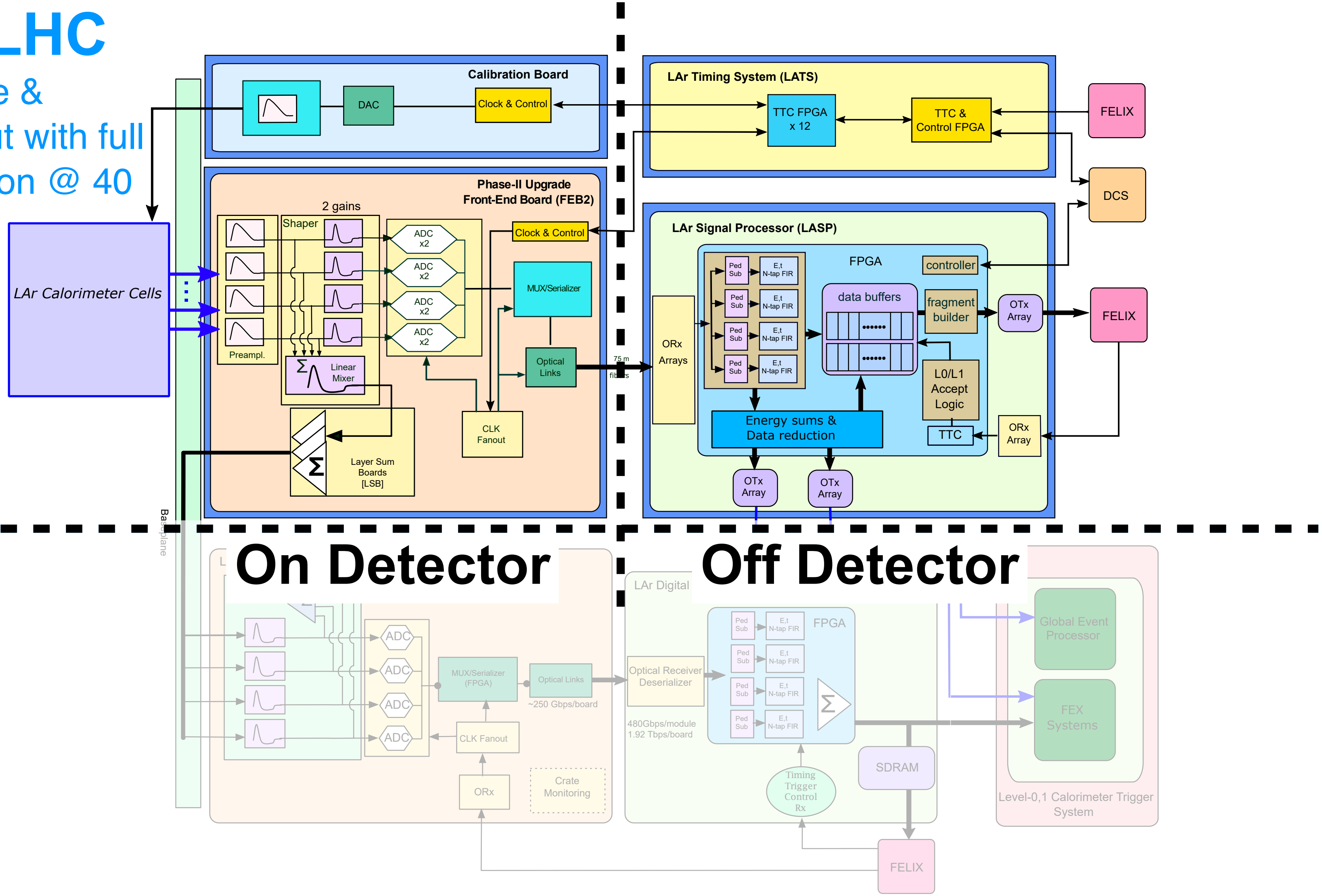
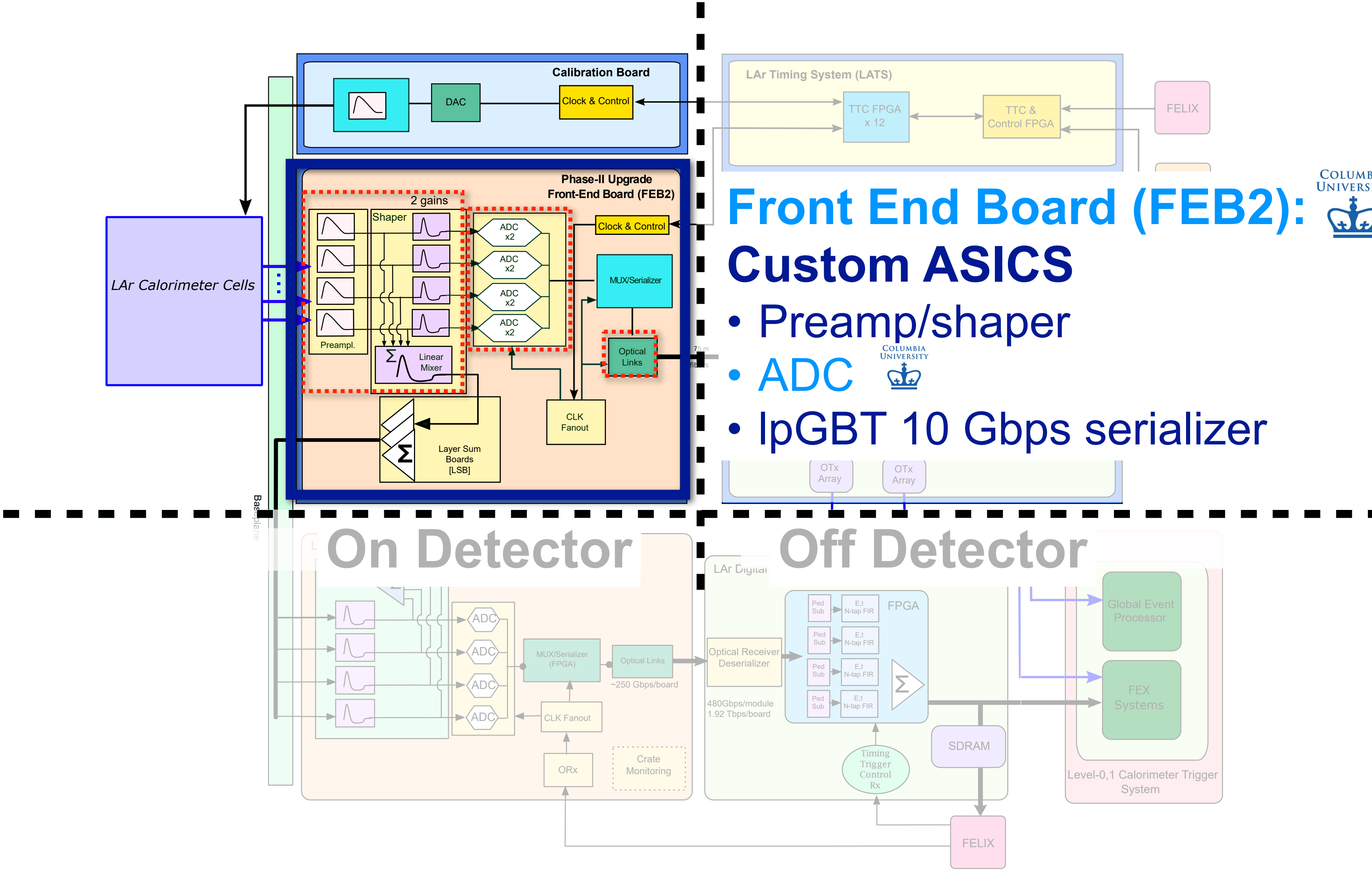


ATLAS HL-LHC LAr Readout

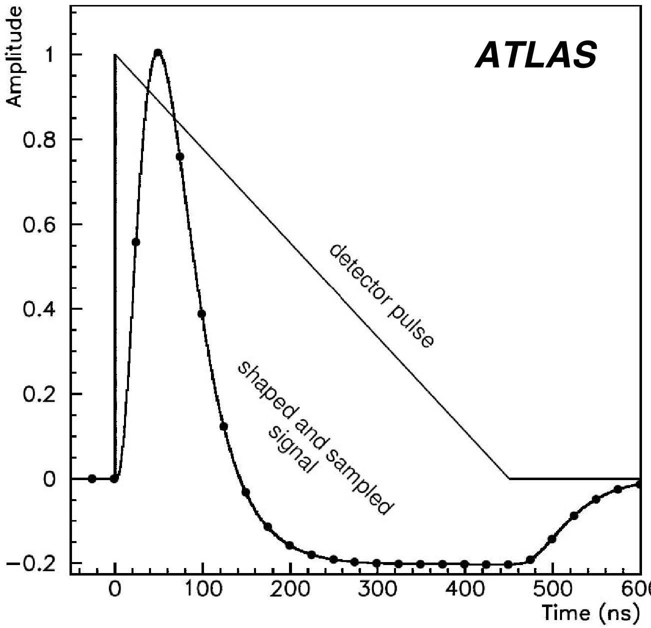


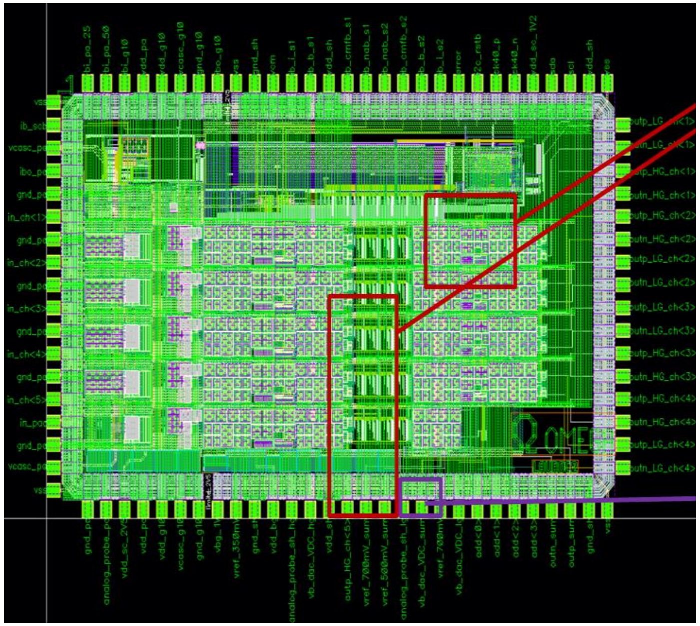
Front End Board (FEB2): Custom ASICS

- Preamp/shaper
- ADC
- lpGBT 10 Gbps serializer

FEB2 Custom ASICs: Preamp/Shaper

- *Analog processing on signals (amplification, splitting into 2 gain scales, CR-(RC)^2 shaping function)*





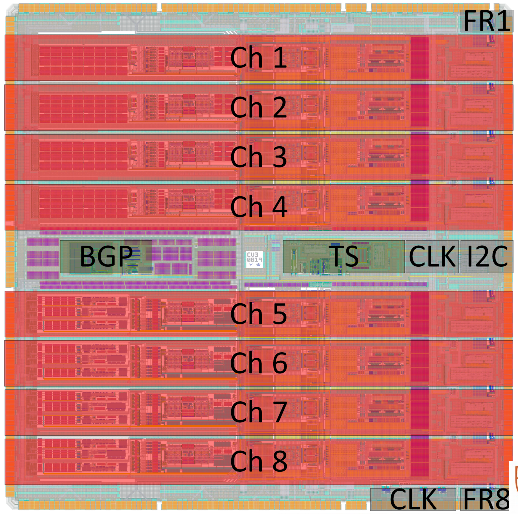
- **Details**: 130 nm CMOS, 16 bit dynamic range, gain ratio 20
- **Specifications**:
  - ENI < 350 nA @ shape time 46 ns (ALFE1 PA/S achieves 147 nA, well within specs)
  - INL < ± 0.3% across full dynamic range

FEB2 Custom ASICs: ADC

- *Digitize PA/S outputs at 40 MHz with 14-bit dynamic range and > 11-bit precision*

- **COLUTA**: full custom 40 Msps in 65nm CMOS
  - >11 bit ENOB over 14 bit DR (3.5 bits from Multiplying DAC followed by 12-bit Successive Approximation Register [SAR])
  - Digitize LAr pulses across almost full dynamic range with resolution within spec

COLUTAv3



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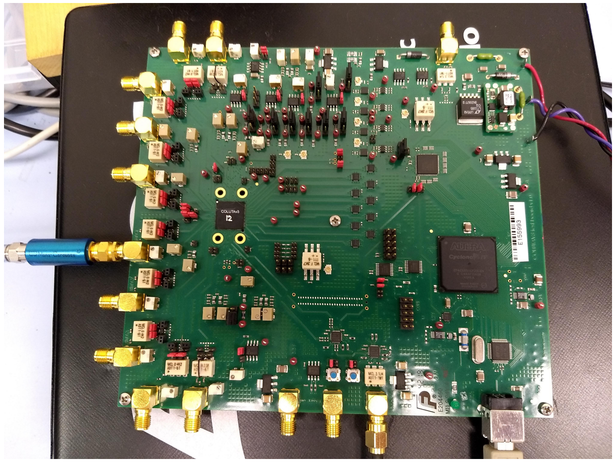
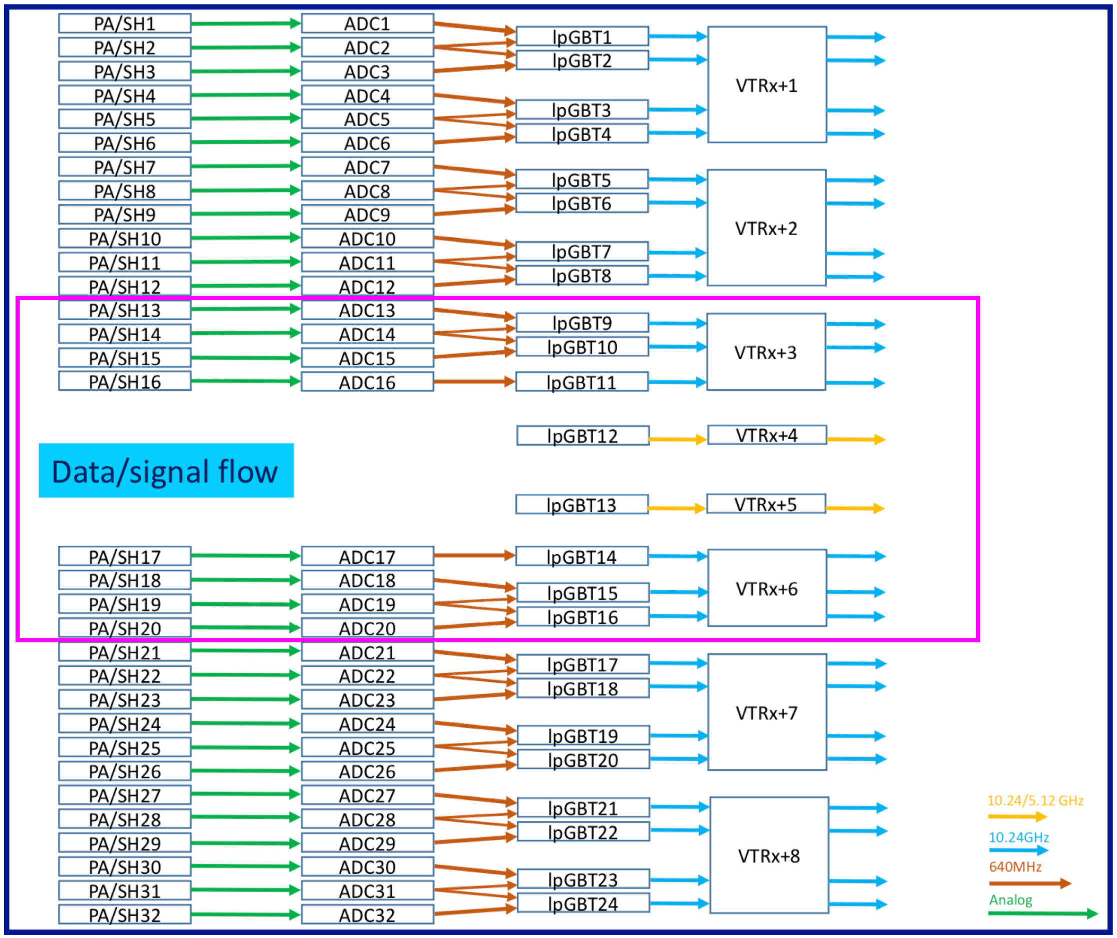


Integration

- Done with a sequence of increasingly complex pre-prototypes with new generations of custom ASIC
- ***2019***: Analog Testboard (2 channels)



2020-21: Slice Testboard

32 channels with 3rd pre-prototypes of PA/S + ADC + v0 prototype of lpGBT

2022: FEB2 prototype

full 128 channels

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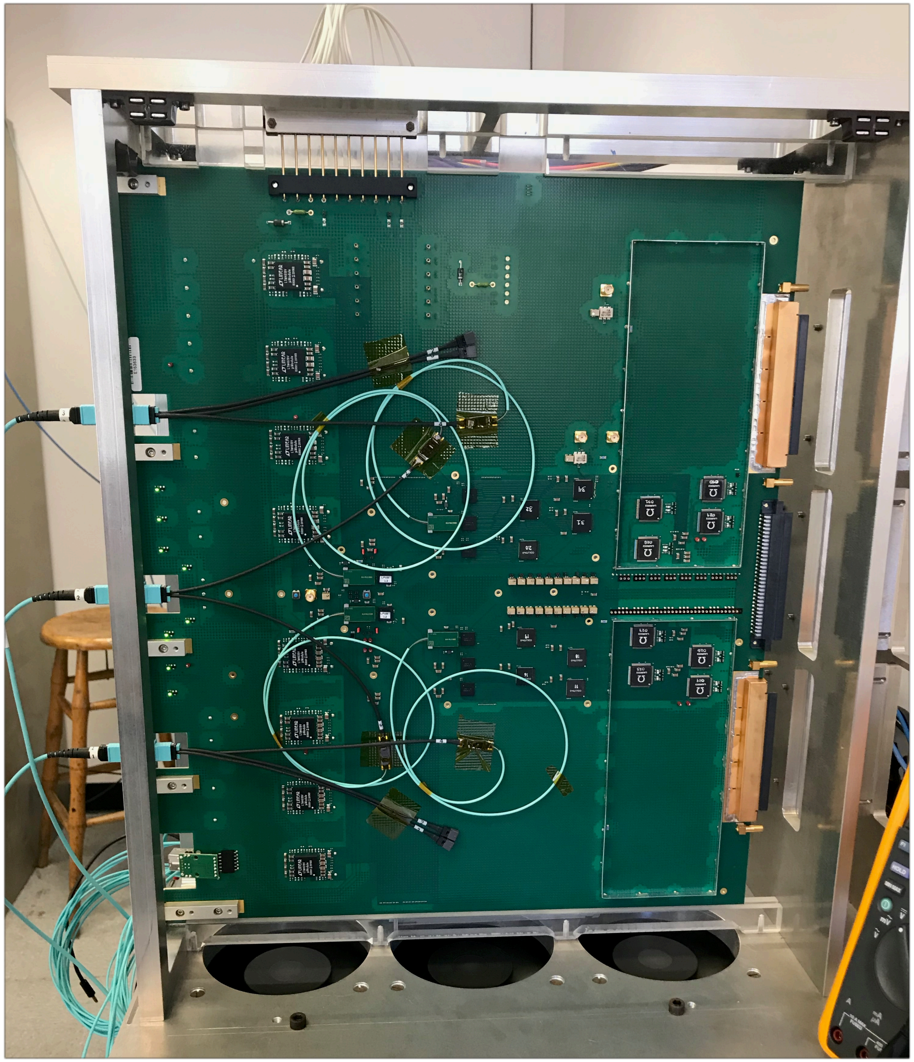
- ***2019***: Analo



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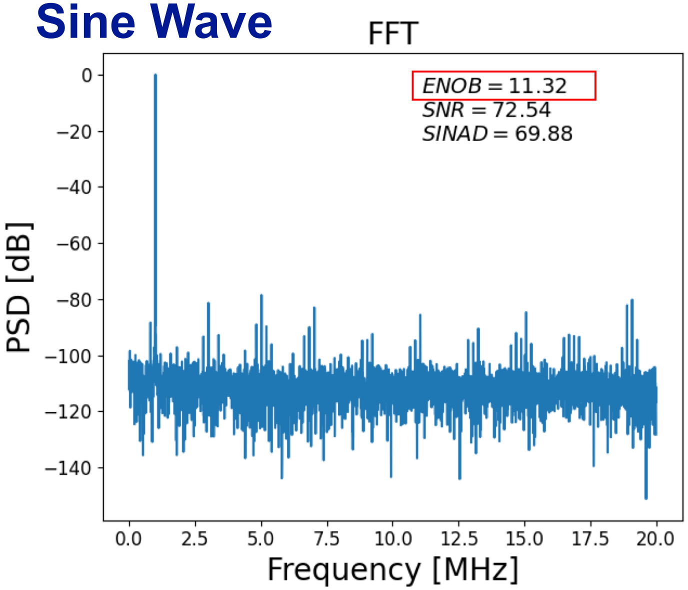
Selected Slice Testboard Results

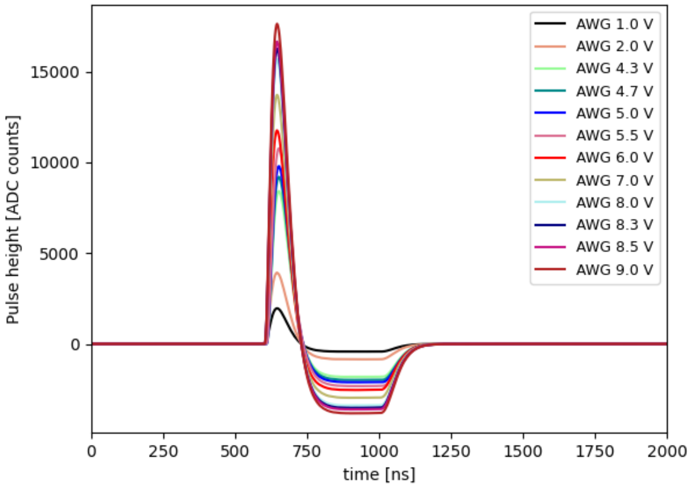
- Characterize performance with pedestal, sine wave, and LAr pulse input

- Design reviews of custom ASICS to verify performance within physics-based specs; ex:
  - Linearity
  - Noise & resolution
  - Cross talk
  - Coherent noise
  - Radiation tolerance

Sine Wave



LAr Pulses



Conclusions

- Many full custom ASICs all working together in full HL-LHC ATLAS LAr calorimeter readout chain (Preamp/shaper → ADC → optical link)
  - Each chip passing stringent design specifications motivated by HL-LHC physics needs

- "Integrate early & integrate often": moving into production of multiple slice testboards and distributing to other institutions for wide integration testing

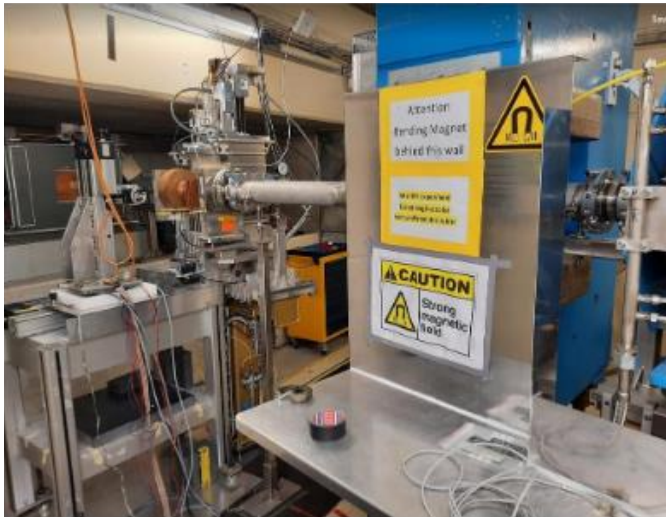
- Next steps:
  - Submission of next iteration (prototype) of ASICs
  - 2022: full 128 channel integrated FEB2 prototype available for testing
  - ~2025: HL-LHC installation begins

Backup

Radiation Testing

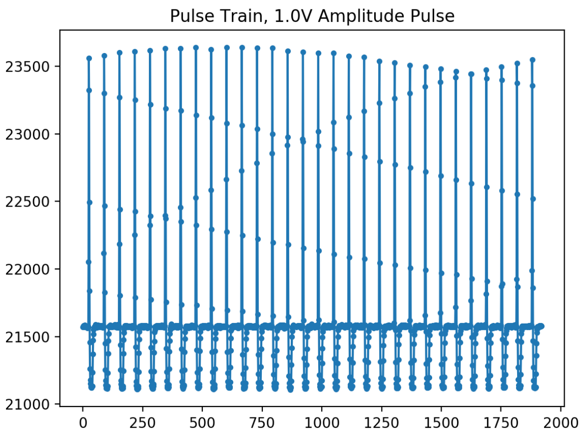
- Facilities:
  - -Paul Scherrer Institute (PSI) Proton Irradiation Facility (Sept 2020)
  - -Space Radiation @ Brookhaven (Nov 2020)
  - -Massachusetts General Hospital proton therapy (Mar 2020)
- Lead + neutron shielding on electronics, expose only chip to be tested
- Ensure custom ASICs survive & measure SEUs, TID, NIEL over entire HL-LHC expected dose

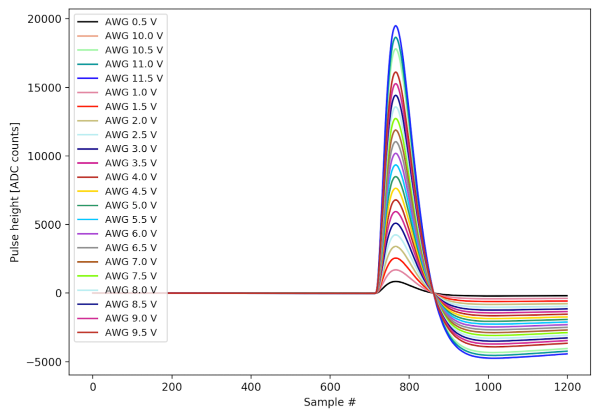
LAUROCv2 PA/S

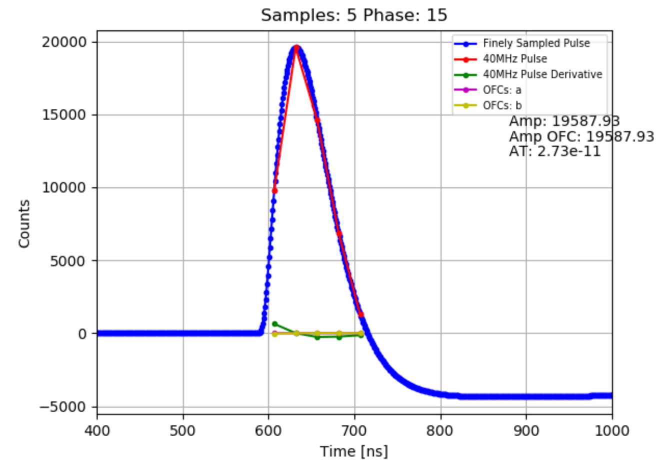


COLUTAv3

LAr Pulse Analysis







AWG sends a pulse train of known amplitude to ADC chip, sampled at different phases

Pulse train is interleaved to reconstruct fine pulse for each amp. Check that maxima and zero point match across amplitudes

Samples from one phase (containing peak) and derivatives are used to calculate OFCs, then used to find energy and timing of each pulse

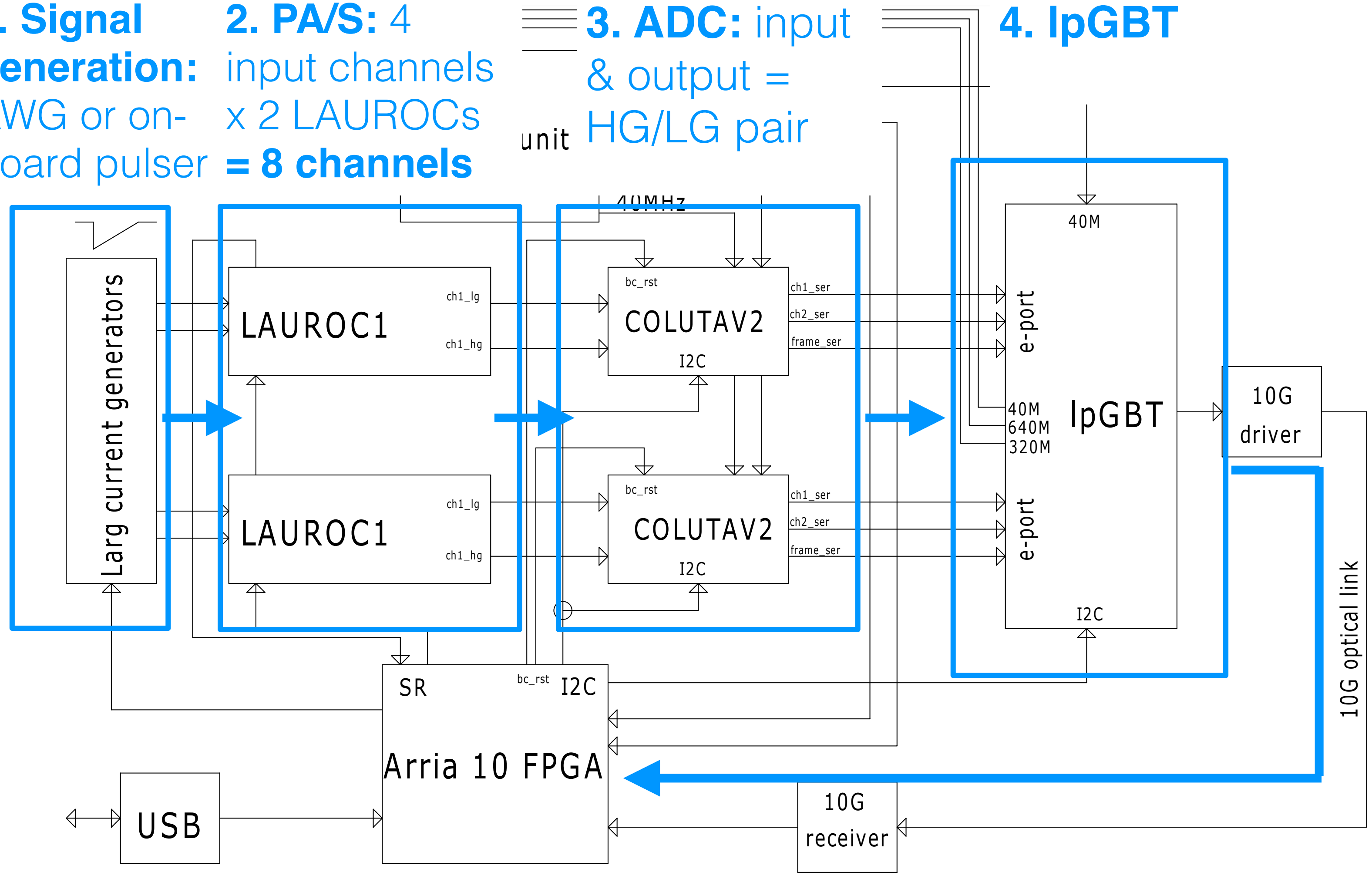
Analog Testboard (2019-2020)

1. Signal generation: AWG or on-board pulser

2. PA/S: 4 input channels x 2 LAUROCs **= 8 channels**

3. ADC: input & output = HG/LG pair

4. lpGBT



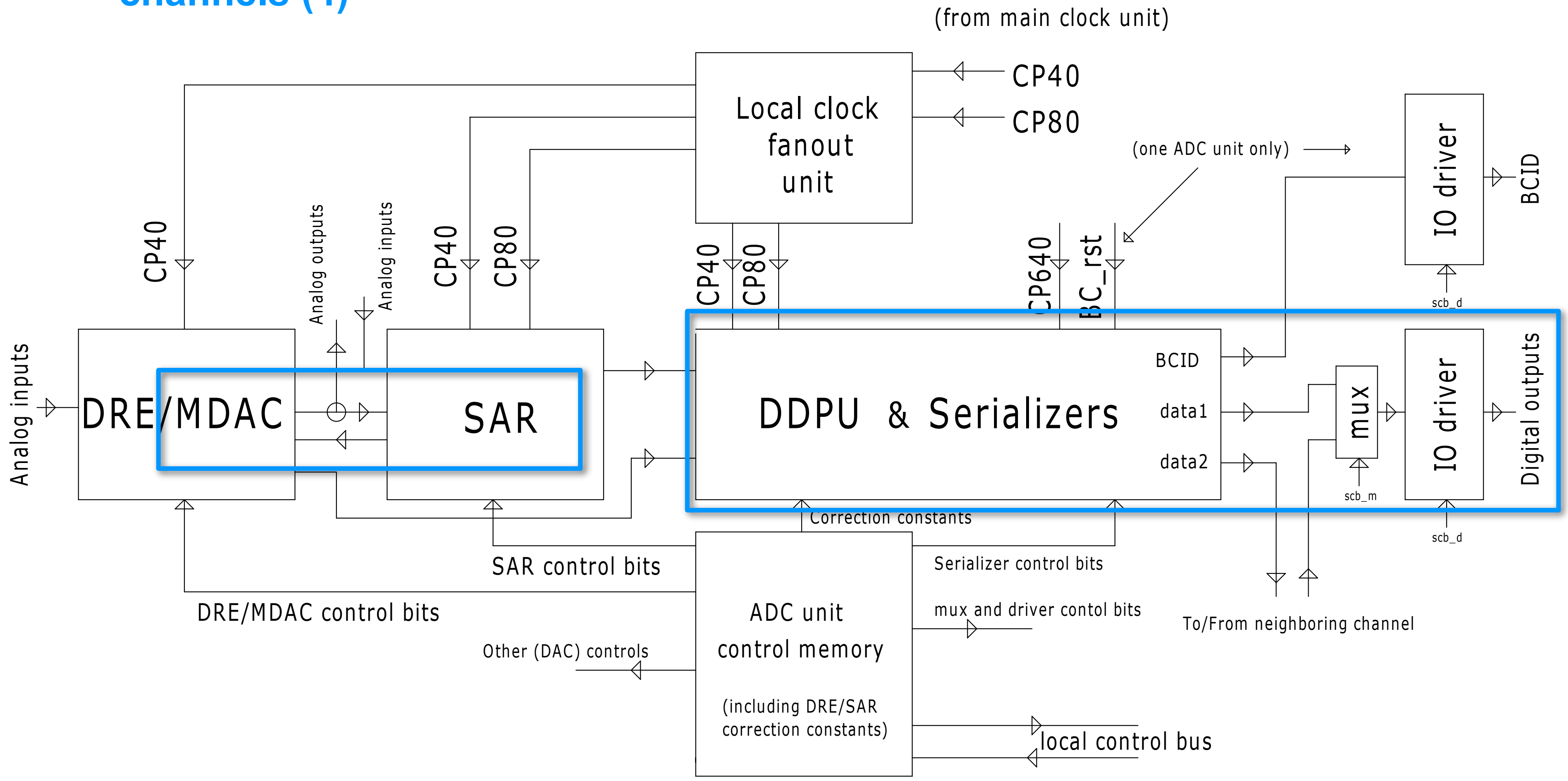
COLUTAv3 PDR Results

- ✓ Sine waves: > 11 ENOB at 1, 5 MHz
- ✓ LAr σ_E/E < 0.25%, time res < 100 ps
- ✓ Coherent noise < 0.2 LSB
- ✓ INL + DNL: no missing codes, < few % at 100% DR
- ✓ Cross talk < 0.1%
- ✓ Precision measurements on 4 channels x 2 soldered boards
- ✓ Stability over several days
- ✓ Temperature stability/range not requiring new calibration
- ✓ Layout-induced and filter-induced errors
- ✓ Operational margins: run at 43, 39 MHz, check power consumption

Cv3 Channel (x8)

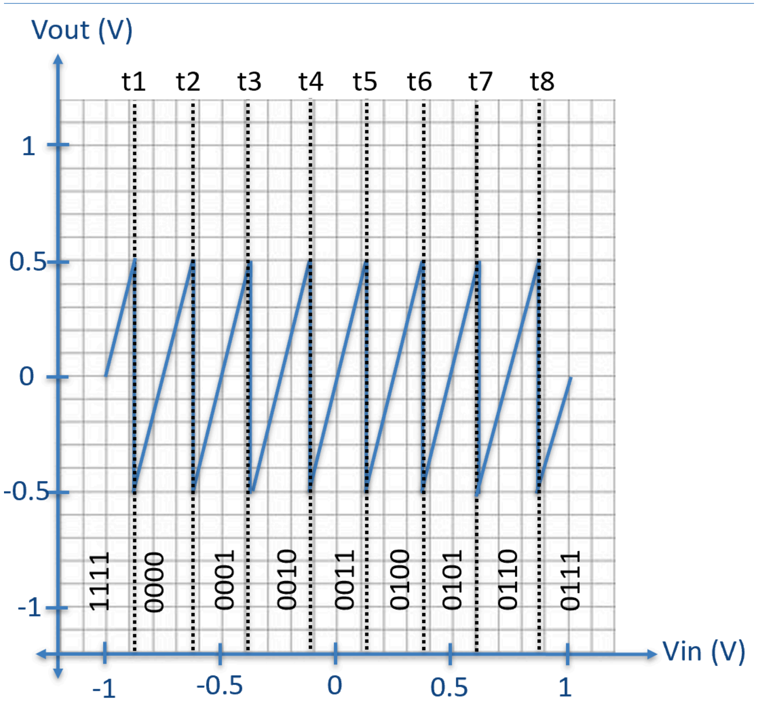
⇨**Use MDAC + SAR channels (4)**

⇨**Digital Data Processing Unit (DDPU): compute ADC codes + output data to lpGBT @ 640 Mbps**



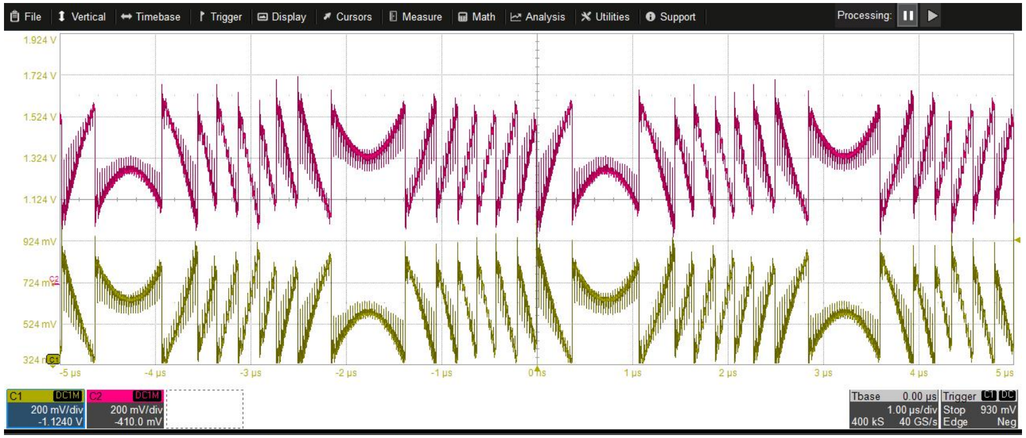
MDAC Characterization

- 9 MDAC subranges, each mapped to cover ~1/2 of SAR full scale



MDAC
Transfer Function

⟹



Scope Image
(input sine)