Argonne NATIONAL LABORATORY

FELIX

The new detector readout system for the ATLAS experiment

Front End LInk eXchange

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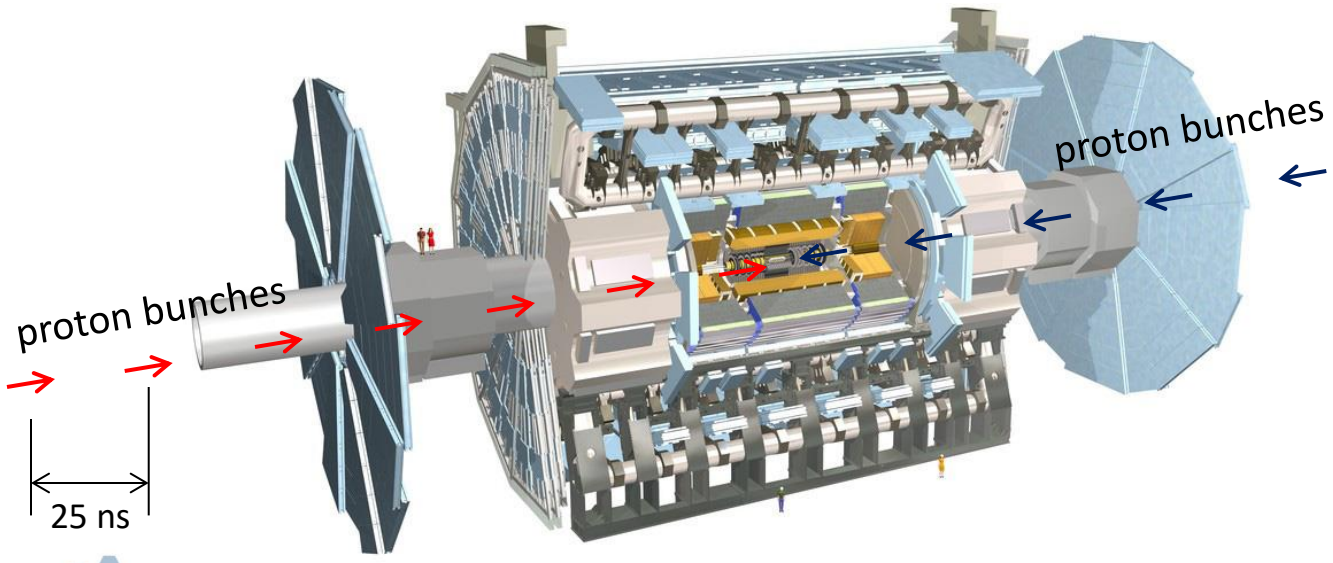
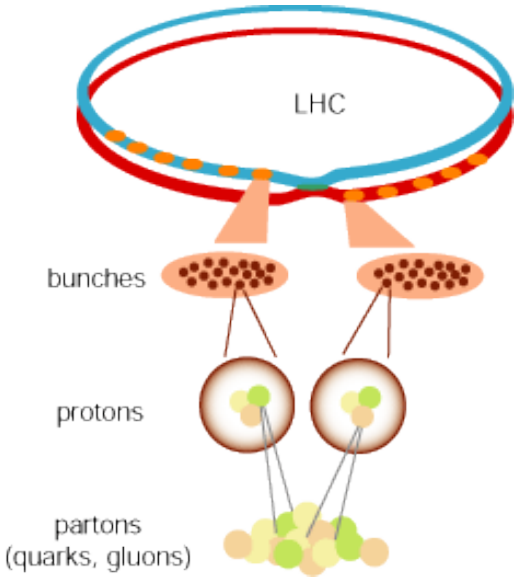
ATLAS EXPERIMENT

U.S. DEPARTMENT OF ENERGY

What is a collider experiment?

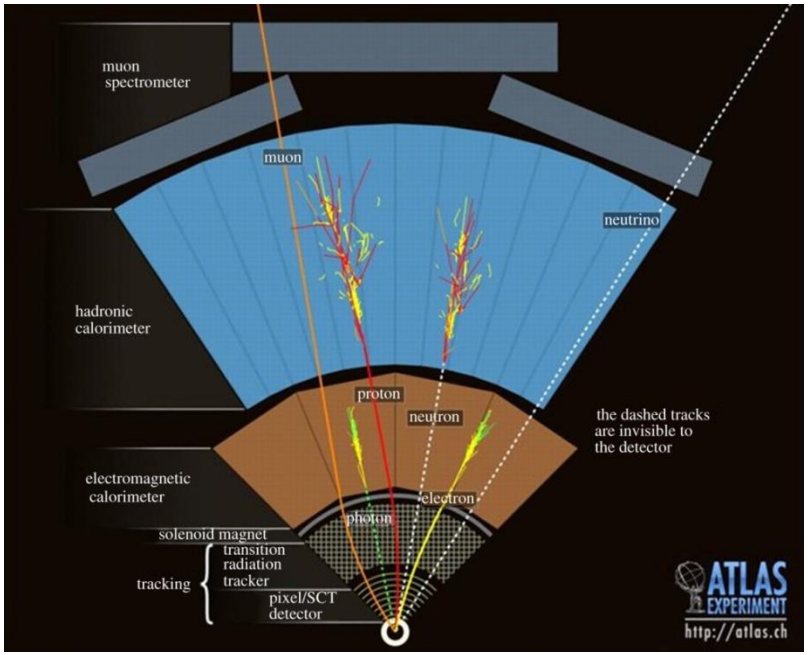
- Contemporary collider experiments study collisions of particles such as protons, electrons, and nuclei to look for new physics.
- The particles are accelerated in bunches so collisions are spaced in time.
- For example, the Large Hadron Collider accelerates protons to about 7 TeV and collides them every 25 ns. The ATLAS experiment at the LHC examines products from these collisions.
- Fixed target experiments (e.g. DUNE) also observe bunches of particles





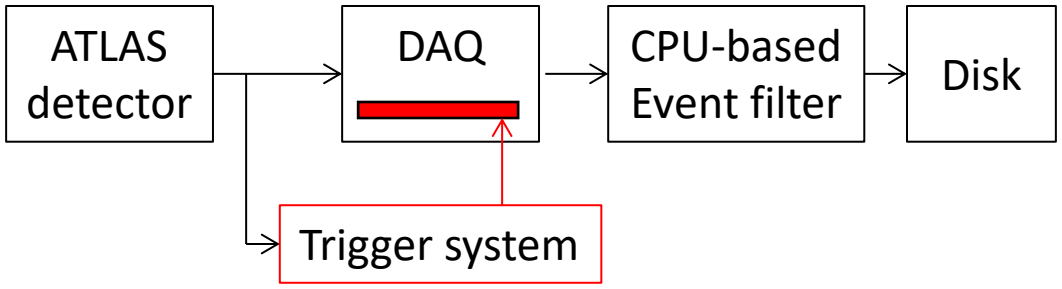
Challenges of the detector readout

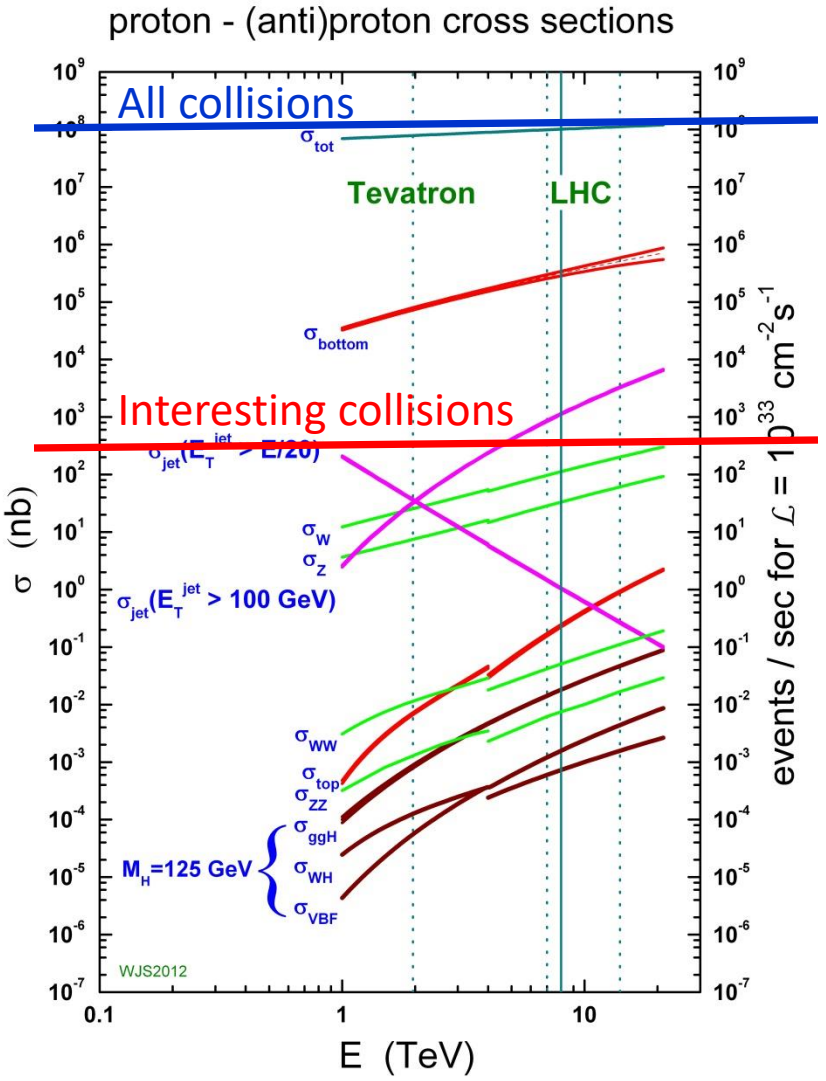
1. Huge number of channels. For example, the ATLAS experiment has
   - calorimeter with 120k channels
   - muon system with 820k fast channels (RPCs and TGCs)
   - inner tracker has 80M pixels and 46k strips
2. Fast sampling rate without dead time
   - 40 Msps for the majority of the ATLAS experiment
3. High level of synchronization for digitization across all the systems (better than 1 ns) for years.
4. High reliability. Beam time is very expensive.
5. Affordable. Limit how much custom electronics is designed.



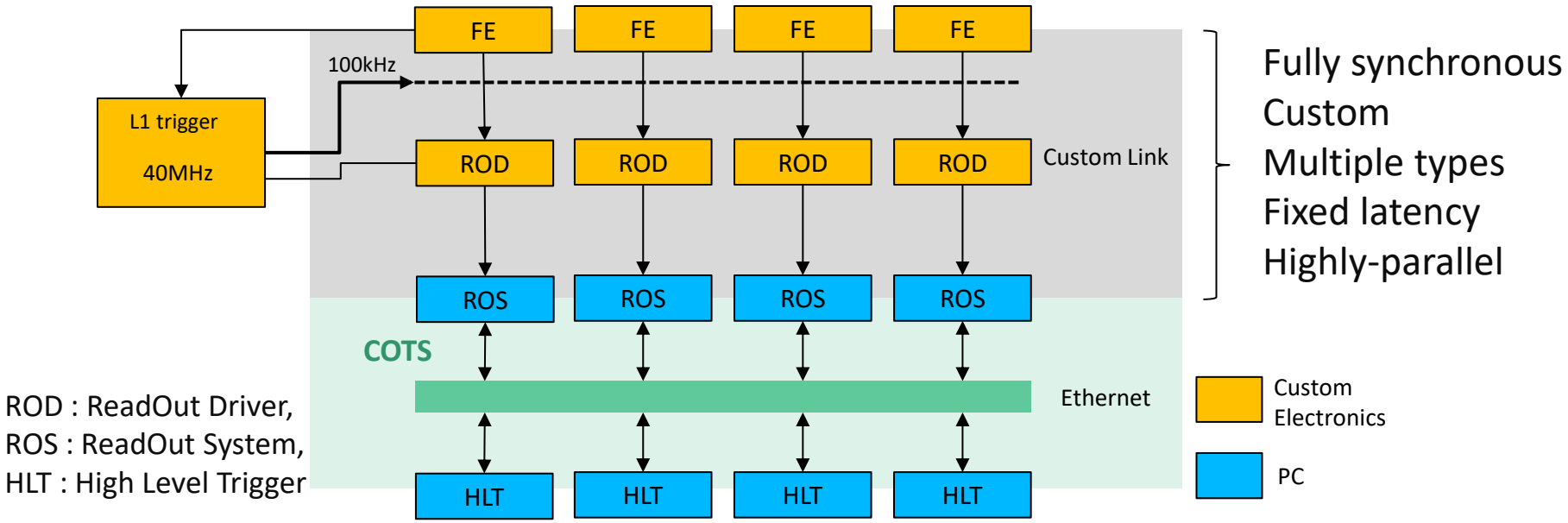
Design of the present Data Acquisition System

- About only 1 out of 40,000 proton collisions (events) is interesting.
- The Trigger/DAQ system filters the entire data volume to keep only data from interesting events.
  - The trigger system performs real time selection is efficient and removes most of uninteresting events.
  - The DAQ system buffers data while the trigger system is analyzing it.



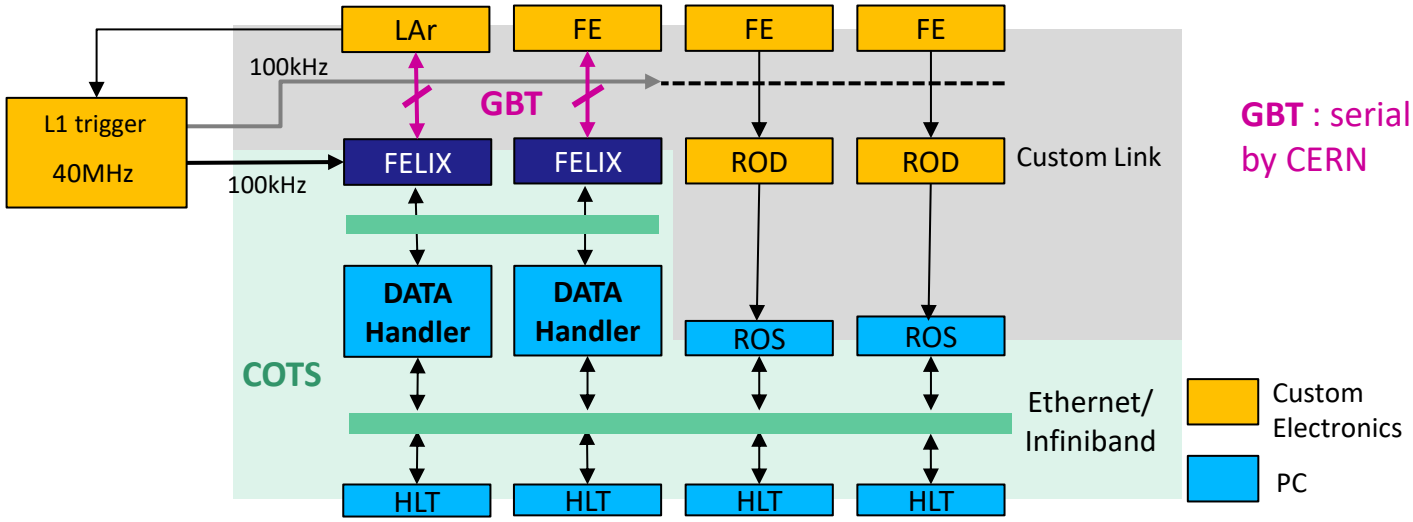


ATLAS DAQ for LHC Run2 (2015-2018)



- Custom hardware and link protocols are used for the frontend readout
  - Commodity systems are easier to support than the custom alternatives
- Most of data is buffered in the on-detector electronics (FE) while the trigger system is analyzing the data
- Trigger signals and LHC clock are sent to both front-end and ReadOut Driver
- This architecture was dictated by capabilities of electronics in ~2005.
- We have designed a faster and simpler readout system

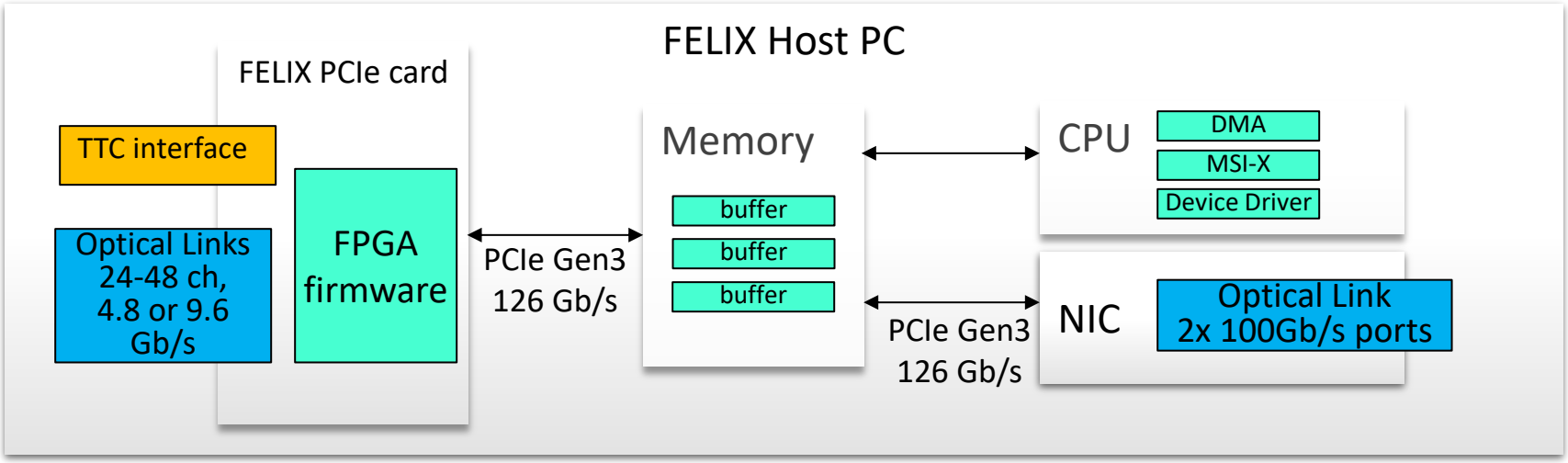
ATLAS DAQ for LHC Run3 (2021-2022)



GBT : serial protocol designed by CERN

- FELIX is a modern detector readout system with fewer custom parts.
  - Much easier to support and upgrade than the older system
- FELIX will readout the new muon detector, LAr calorimeters, and calorimeter trigger electronics
  - Readout and configuration of on-detector electronics
  - Distribution of trigger information and LHC clock to the on-detector (FE) systems

FELIX hardware platform



PCIe card with FPGA chip + Host PC + NIC

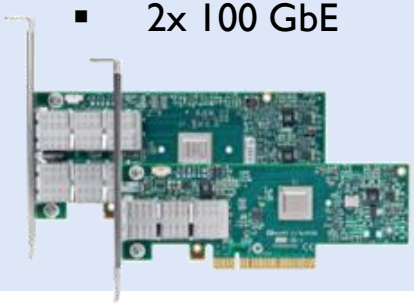
TTC (Time, Trigger and Control) : LHC protocol used to distribute global clock (40.08MHz) and information from the real-time trigger

FELIX hardware components

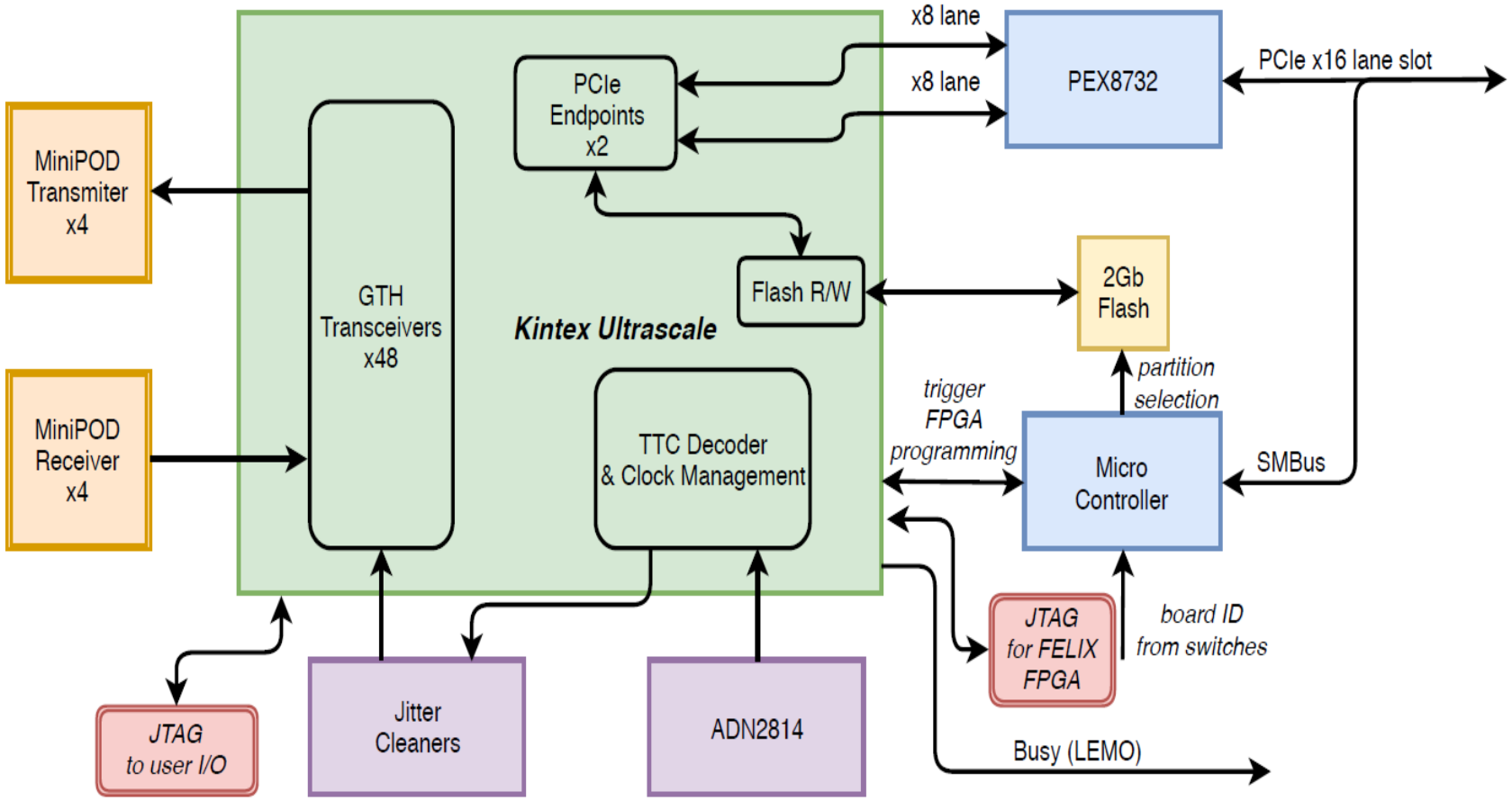
- **FLX712 board**
  - Custom board with Xilinx Kintex Ultrascale XCKU115
  - 48 optical links (MiniPODs) with up to 12 Gb/s per link
  - Input: 24 GBT links (4.8 Gb/s) or 12 8b/10b links (9.6 Gb/s)
  - Output: 24 or 48 GBT links (4.8 Gb/s)
  - The mezzanine board is customizable for a variety of timing and trigger distribution signals (e.g. White Rabbit)
  - The ATLAS TTC signal is sampled with ADN2814 receiver on the mezzanine board
  - SI5345 and LMK03200 clock jitter cleaners
  - PCIe Gen3 x16 (via a 2x8 switch)
  - 100+ boards were produced through CERN

- **Sample Motherboard**
  - SuperMicro X10SRA-F
  - Single fast CPU
  - 4 PCIe Gen3 slots

- **Sample NIC**
  - Mellanox ConnectX-5
  - 2x FDR/QDR Infiniband
  - 2x 100 GbE

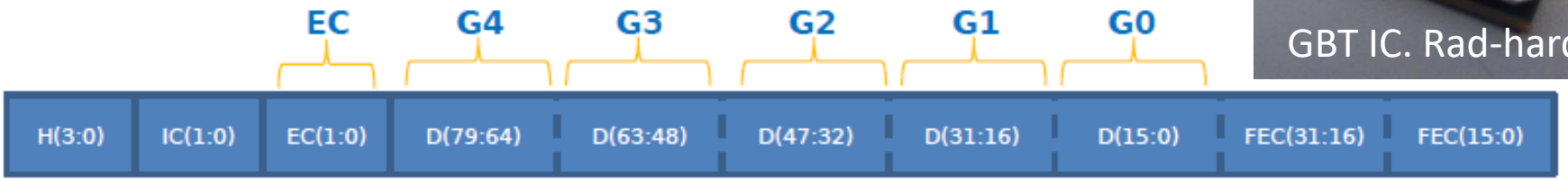


FLX712 components

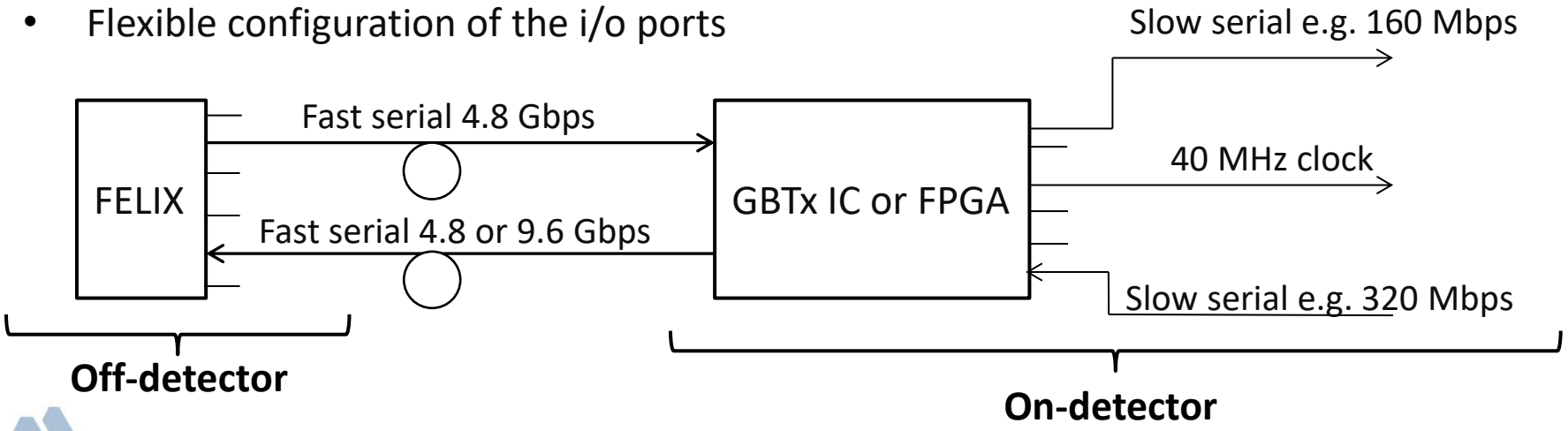


GBT Protocol

- The protocol provides aggregation and deaggregation of multiple slower data streams into a single fast serial link
  - A slow serial link (aka e-link) is driven by a selected set of bits in the GBT frame

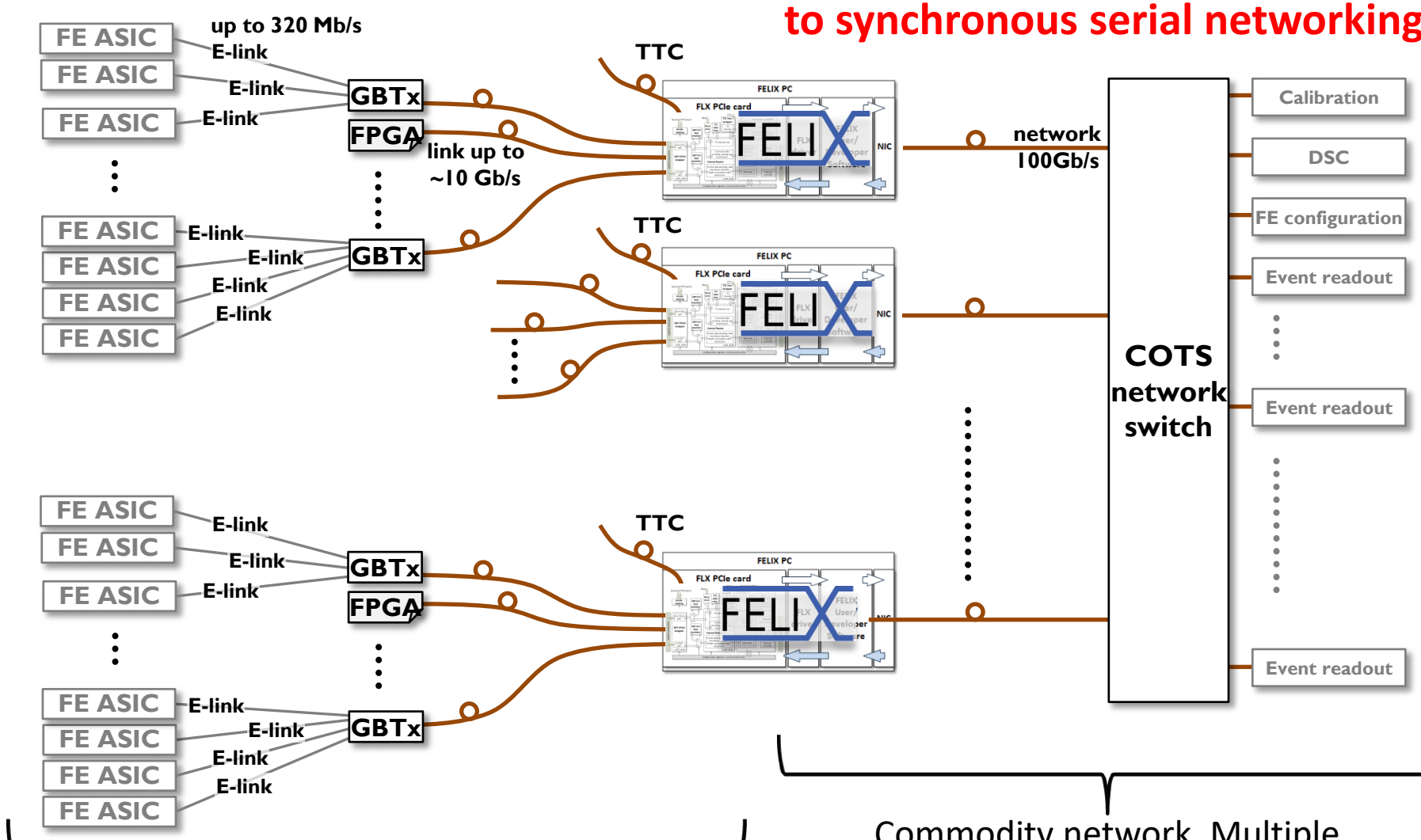


- The GB frame is fully synchronous with the LHC clock
- High fidelity clock (40 , 80, 160, or 320 MHz clock)
  - Trigger and timing control for the on-detector electronics
- Flexible configuration of the i/o ports



FELIX data flow overview

Large-scale flexibility of commodity to synchronous serial networking.



FELIX firmware design

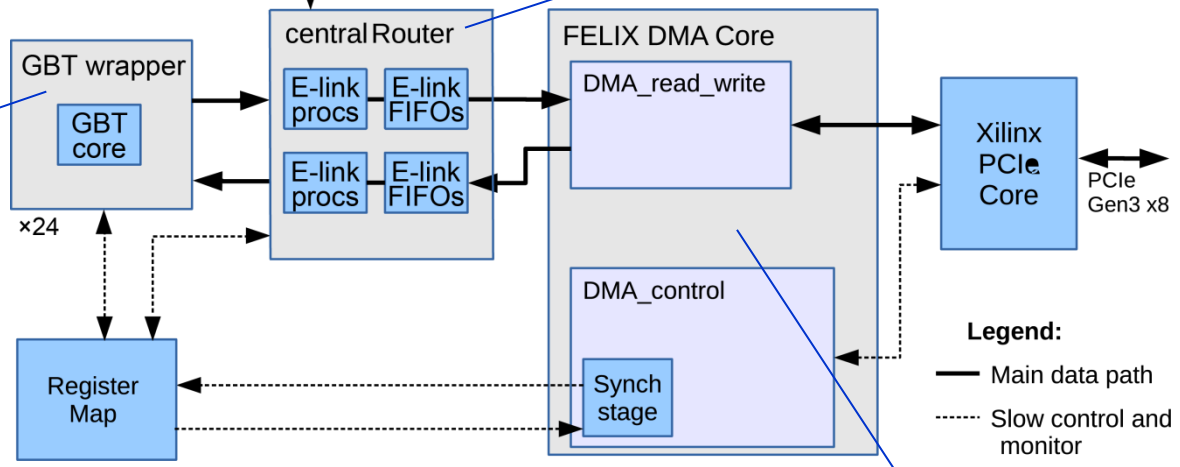
Decoding TTC information and LHC clock recovering

Data routing using E-Link

Optical Link Transceiver using GBT protocol

Two link modes:

GBT-frame mode, Full mode



PCIe DMA engine

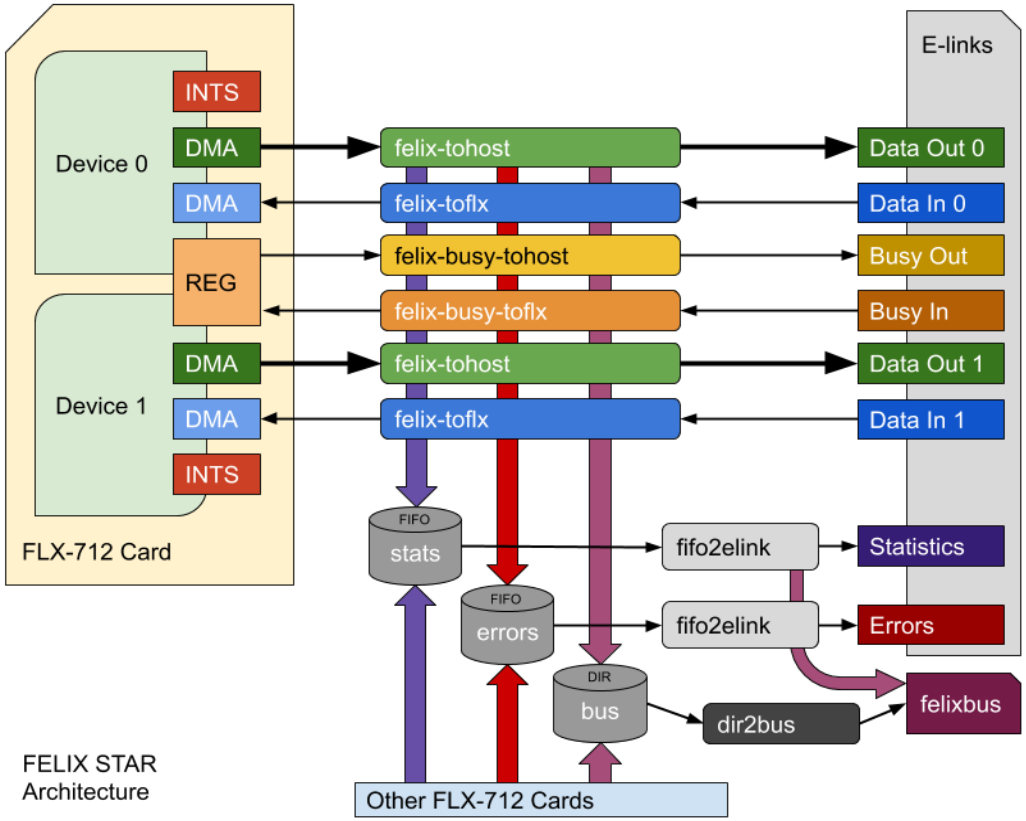
E-link: slow serial electrical links typically from Front end ASICs

24 GBT (4.8G) links

12 Full mode (9.6G) links

48 links for TTC-fan-out

FELIX software



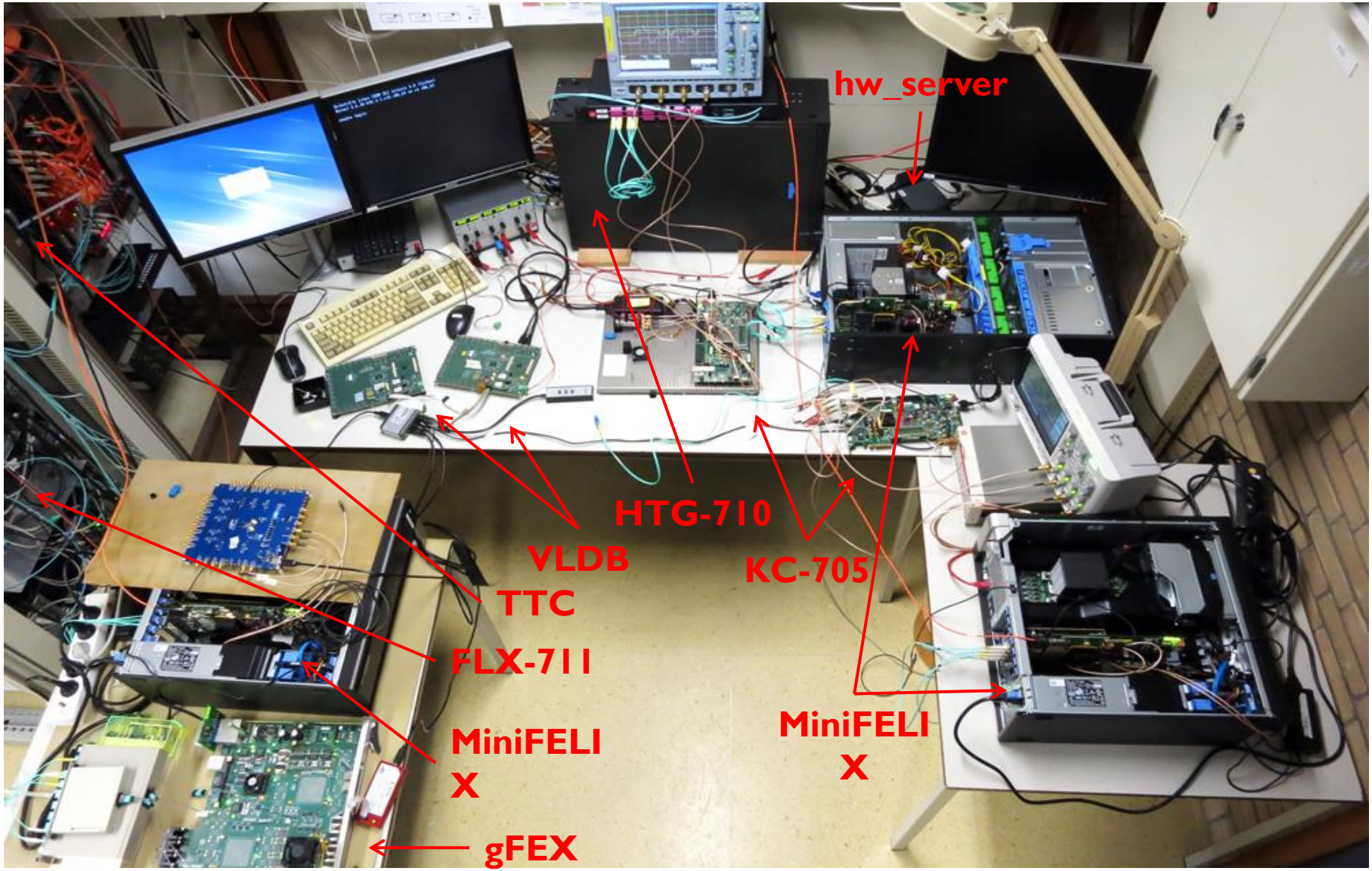
- FelixStar Application

  Data processing pipeline from(to) the PCIe DMA buffer to(from) the NIC
  - NetIO-next is used for data exchanging with network hosts.

    abstracts the low level network implementation.

    POSIX and RDMS backends are supported

Integration of FELIX with the other systems



Integration of FELIX with the other systems

- ATLAS sub-detector test setups, currently implementing FELIX
  - *Liquid Argon Calorimeter*
    - **LTDB** (LAr Trigger Digitizer Board) -- 40+ channels to monitor the FE and operate the TTC distribution
    - **LDPB** (LAr Digital Processing Blade) -- FELIX in FULL mode
  - *Level-1 calorimeter trigger*
    - **gFEX** (Global Feature Extractor): 12 FULL mode links
    - **ROD**, **Hub** for **eFEX** (Electron Feature Extractor) and **jFEX** (Jet Feature Extractor)
    - **TREX** (Tile Rear Extension)
  - *Muon spectrometer*
    - **New Small Wheels (NSW)**
    - **BIS78** (Barrel Inner Small MDT (sector 7/8))
  - *Tile Calorimeter*
    - Test system for Phase-II readout
    - Initial communication established with the Tile PPr board in GBT mode
    - Stepping toward FULL mode communication
  - *Pixel and Strip sensors readout (for the upcoming ITk Inner Tracker)*

Integration of FELIX with the other systems

- *Non-ATLAS detectors connected to FELIX*
  - Several experiments outside the ATLAS collaboration expressed interest in the FELIX system to control and readout their detectors
  - A number of them is actively evaluating FELIX as a possible readout solution
  - DUNE collaboration has chosen FELIX
    - Digitization and buffering of cosmic rate data for Supernova Trigger (~100 sec buffer)

Outlook

- *Prototype hardware platform*
  - Uses Xilinx Versal Prime FPGA
  - Supports PCIe gen4 x16
  - Optional support for optical links with up to 25 Gb/s
  - Recent tests of the PCIe gen4 interface are promising
- *Development of a prototype firmware for ATLAS*
  - Higher trigger rate: 100 kHz → 1 MHz
  - support new detector systems and data transmission protocols
  - lpGBT and 64b/67b in addition to lpGBT for the optical links
  - 64b/66b, 6b/8b, and a variety of custom serial link protocols for the slower electrical links.
  - The new TTC system will receive data at 9.6 Gb/s instead of 160 Mb/s

Summary and prospects

- FELIX is a router between custom serial links and a commodity network
  - Takes advantage of the latest technology to simplify the ATLAS readout
- In LHC Run-3 (2021-2023) FELIX will be used for selected detectors and trigger systems.
  - FELIX firmware and the software are mature
  - Most of the boards have been produced
- Ongoing efforts:
  - Integration with the ATLAS on-detector (front-end) systems
  - Development of FELIX board and firmware for LHC Run-4.