X2O: A MODULAR ATCA DESIGN WITH COST OPTIMIZATION OPTIONS

A. MADORSKY FOR X2O TEAM

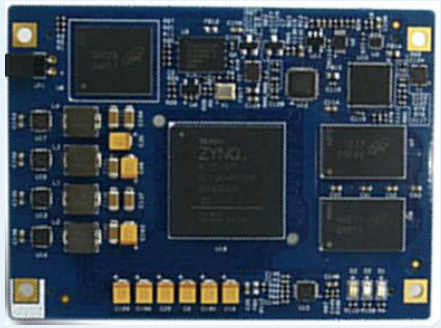
X2O: INTRODUCTION

- X2O is a modular system in ATCA standard
- Designed with cost optimization in mind
- Uses lower-cost parts and materials
- Customizable for user's needs

X20 APPROACH

- Eliminate base board altogether
- Large heat sink as mechanical platform
- Just 3 major mechanical parts:
  - Heat sink
  - Top rail
  - Bottom rail
- Standard Front panel

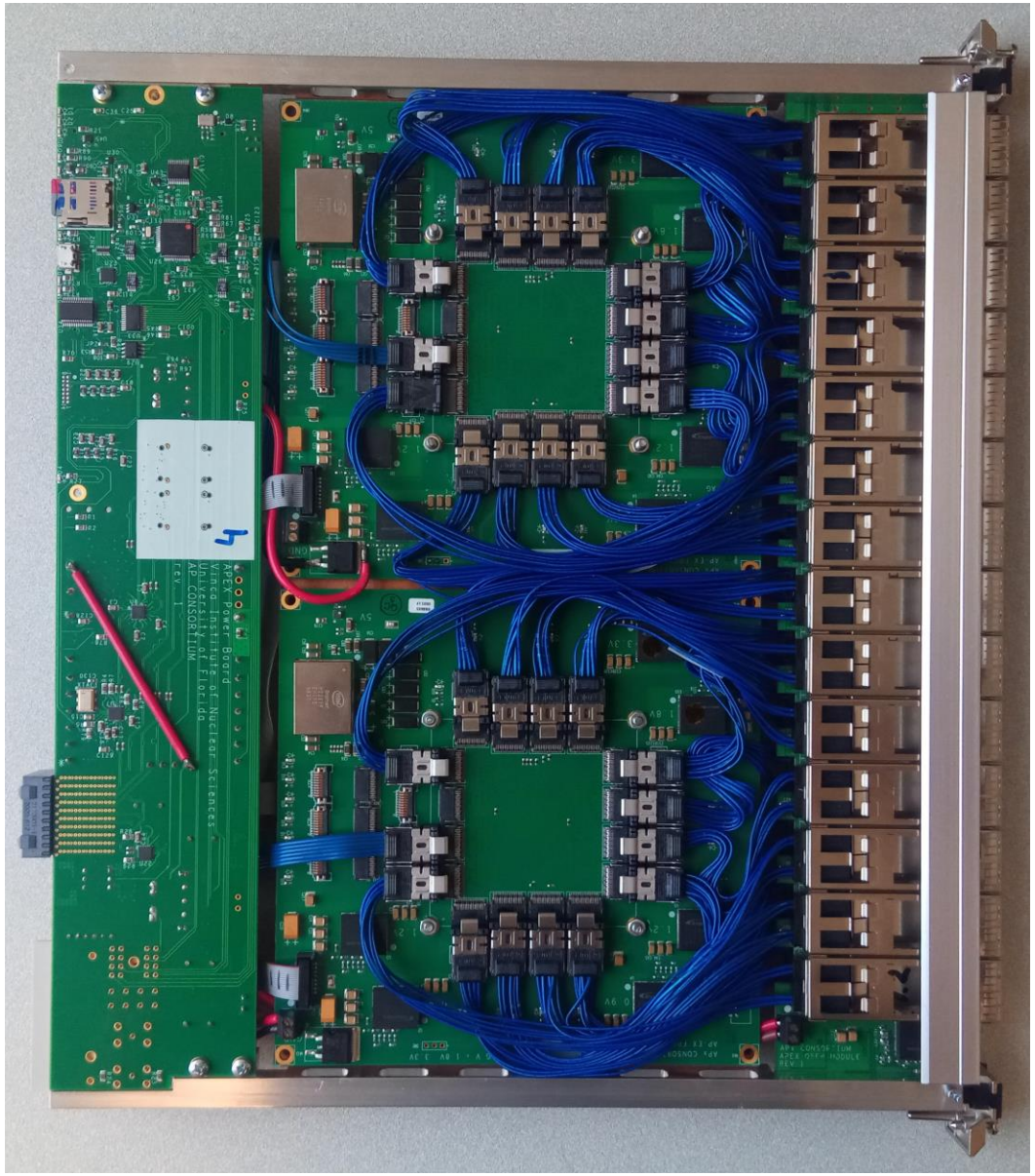
X20 COST OPTIMIZATION

Component	Cost-optimized part	Image
Optical links	Vendor: FS P/N 25G: QSFP28-SR4-100G P/N 10G: QSFP-SR4-40G	
Control interface	Vendor: MyIR P/N: MYC-C7Z015 Based on ZYNQ Used as both IPMC host and control interface	
PCB material	Vendor: Isola P/N: 370HR (generic FR-4) Should be easy to replace with halogen-free material	

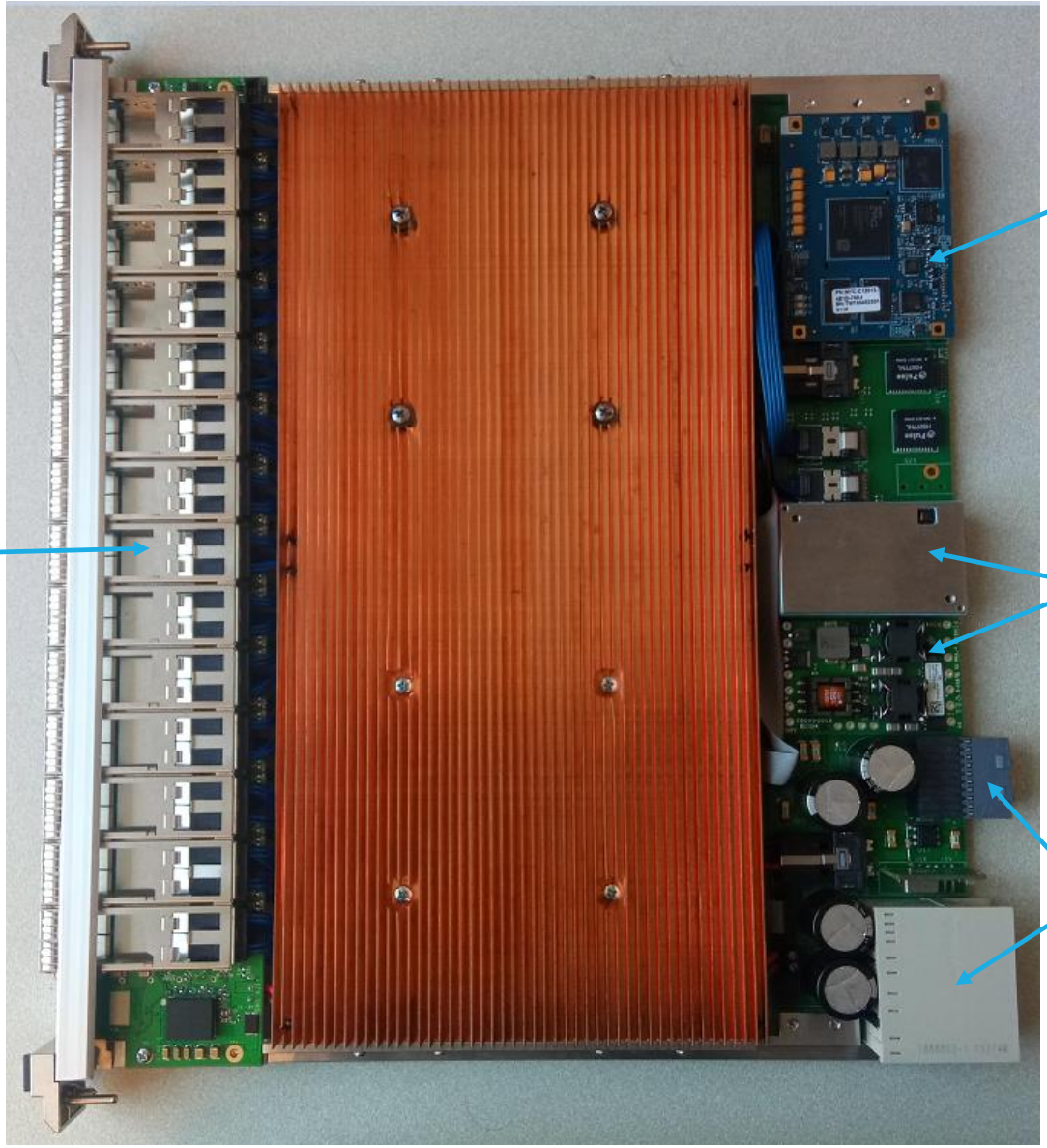
MODULES

- FPGA modules are attached to heat sink
- Optical module near front panel
- Power module near backplane
  - Also contains ZYNQ mezzanine

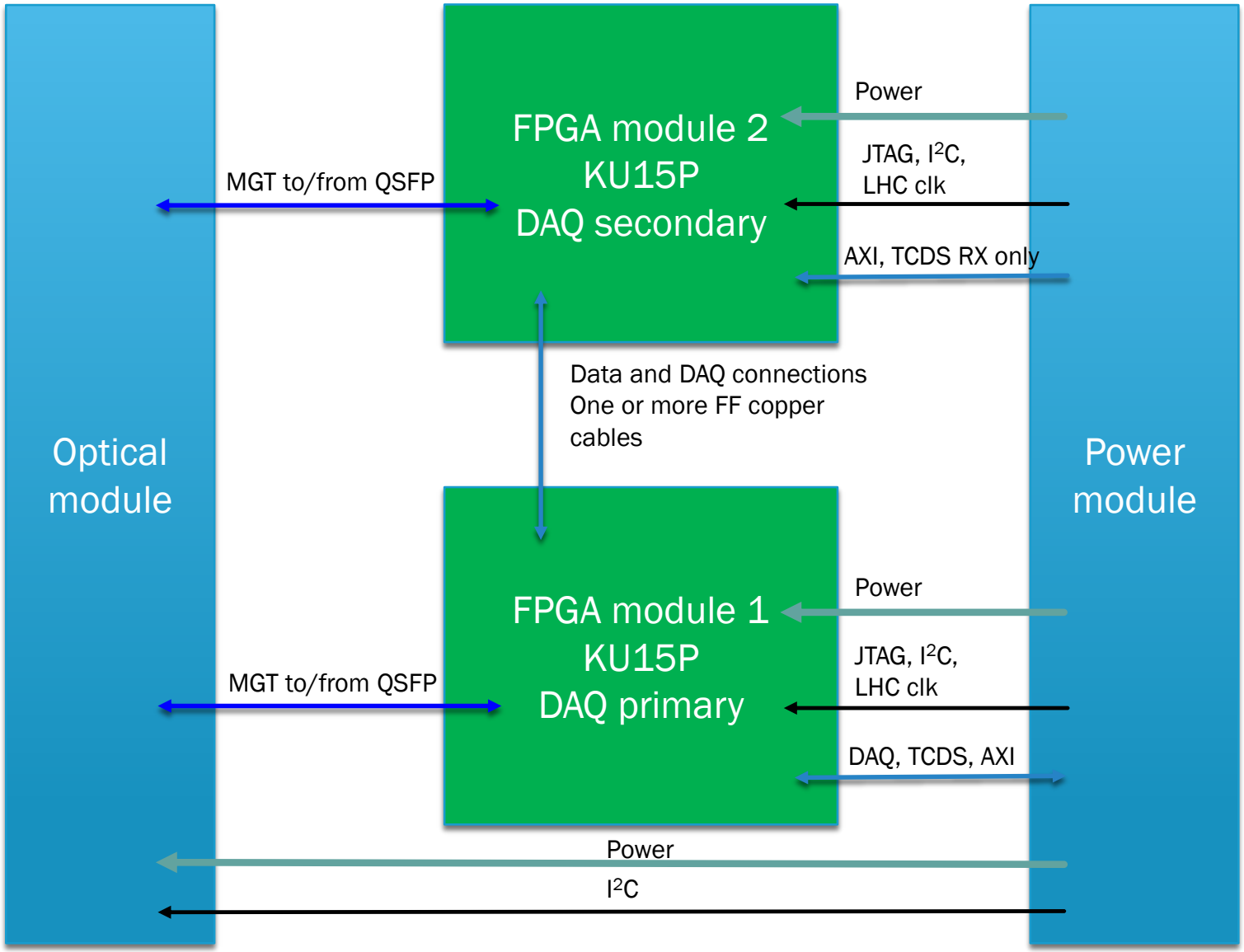
- Approximate costs of the unit:
- All QSFPs populated with 25G devices: $13,000
- All QSFPs populated with 10G devices: $11,400



DETAILS


ZYNQ module
QSFP+ cages
Up to 28 pcs
DC-DC converters
Backplane
connectors

MODULE CONNECTIONS



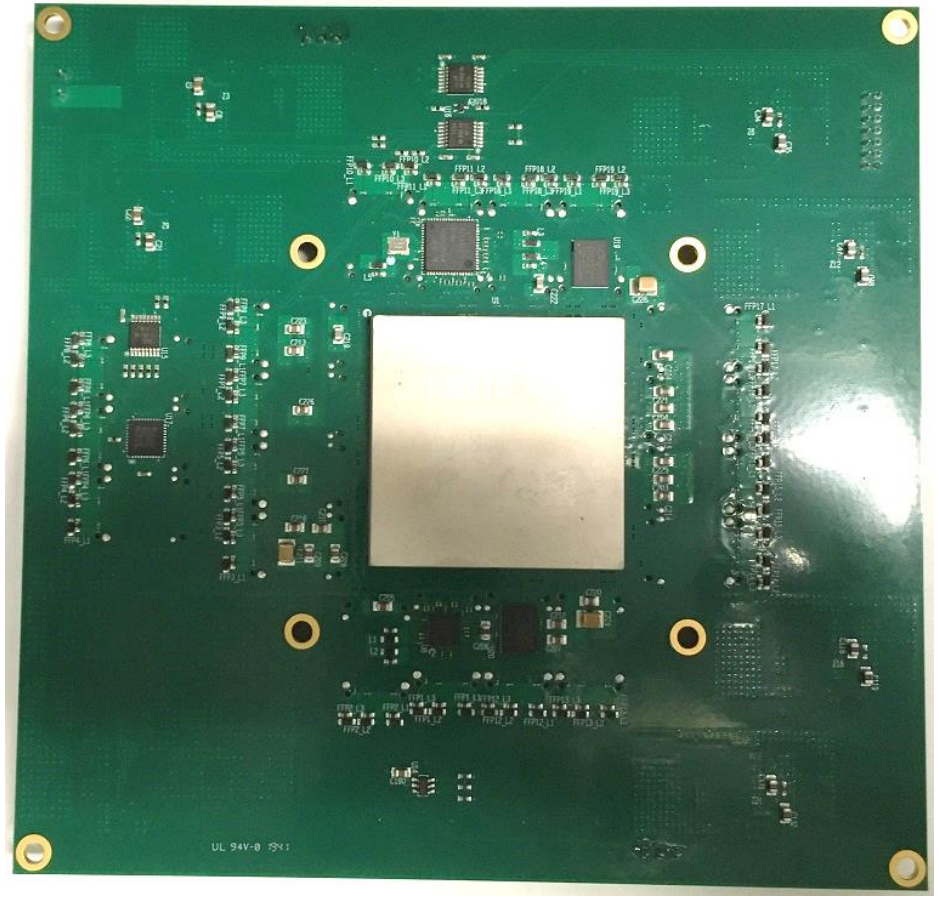
CONNECTING CABLES

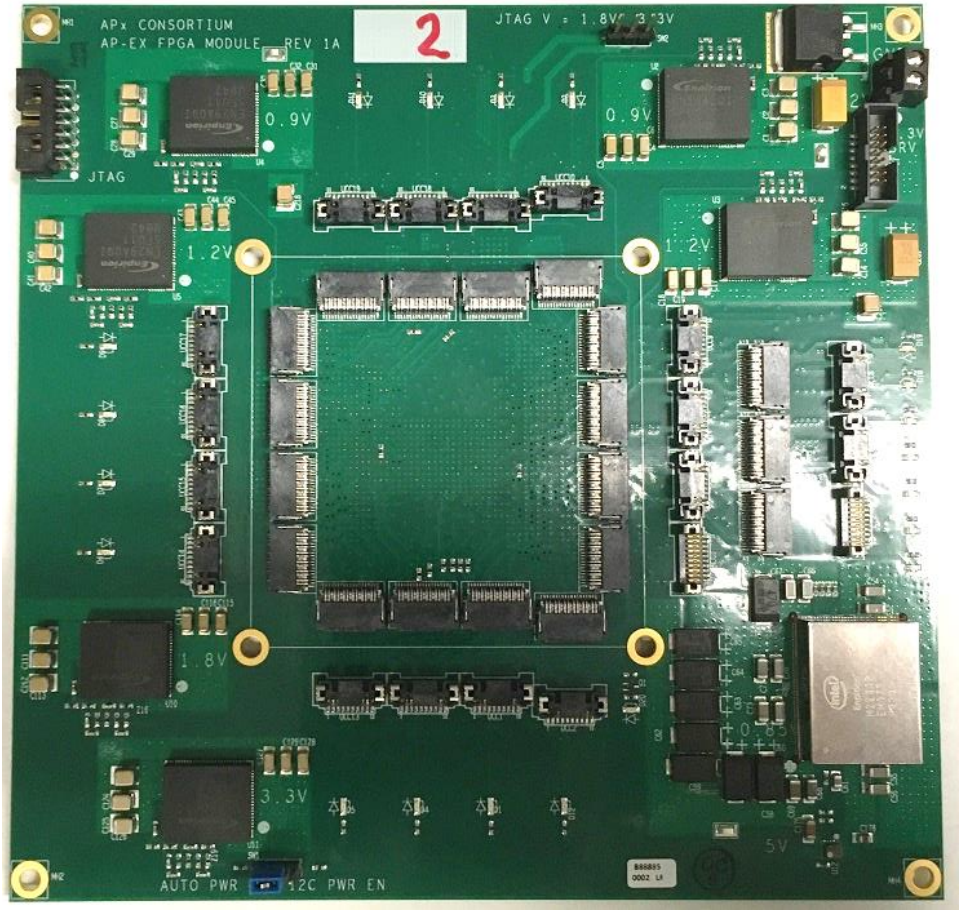
Firefly copper cable

Firefly to QSFP copper cable

Flat ribbon cable, 1.27 mm pitch

X20 KU15P MODULE





Size: ~150 x 150 mm

X20 KU15P MODULE

- 370HR material
  - generic inexpensive FR-4
  - 12 layers
  - Backdrilling on top and bottom
  - No blind/buried vias
- KU15P FPGA
- 19 Firefly connectors for all available MGTs
  - As close as possible to FPGA
  - All 25G connections under 1”
  - All 16G connections under 2”
- Some of them are used for connection to ZYNQ and to another FPGA module
  - Via electrical cables
- Most are used for QSFP modules
- Two external SDRAM chips, 128 Mb each
- 80A VCCINT supply
- 10A MGT supplies
  - GTH and GTY separately
  - Intel “Enpirion” family component specifically designed for low-noise power
  - Directly feeding MGTs without intermediate linear regulators

X20 QSFP MODULE

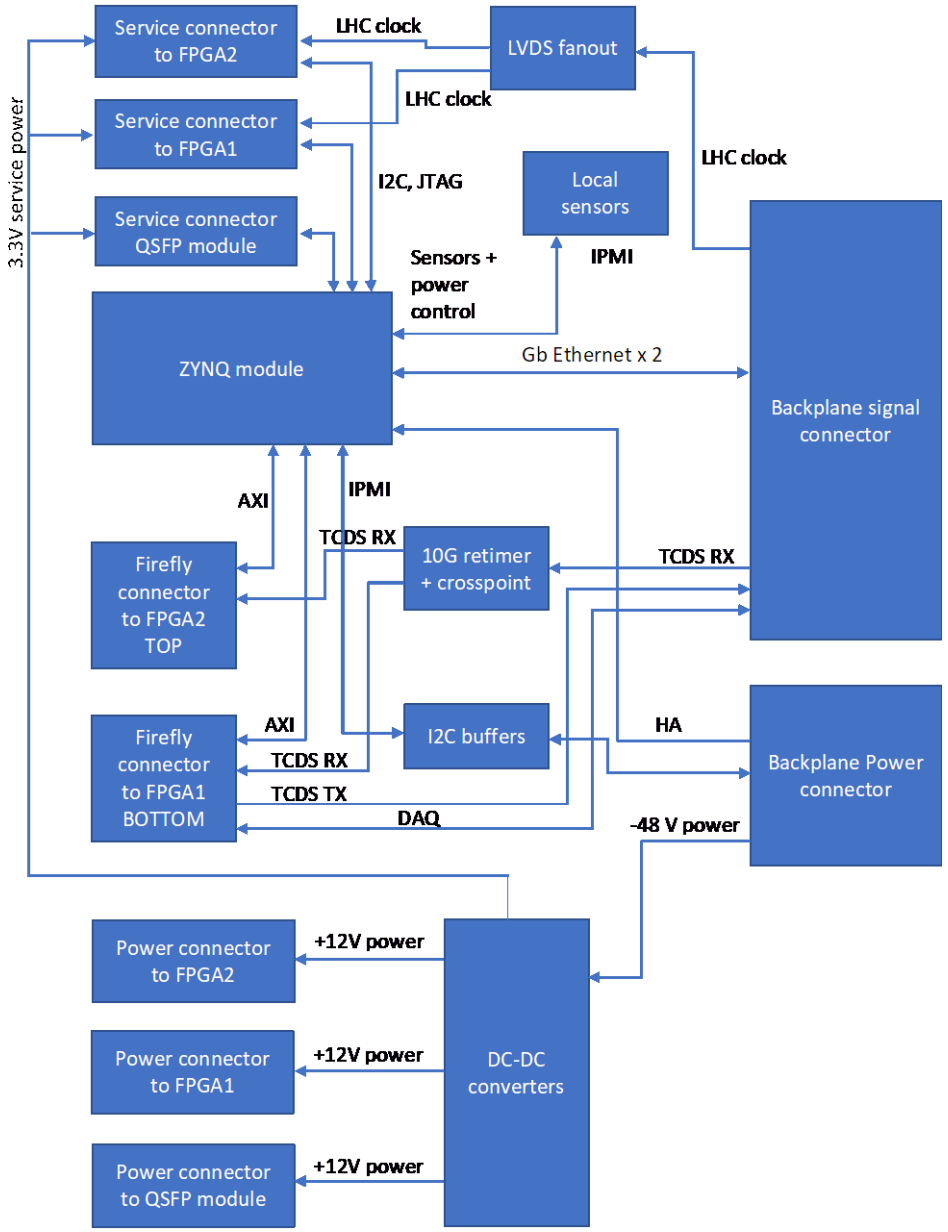
- Up to 28 QSFP cages on the front panel
- Compatible with 10G and 25G QSFP links
  - Each QSFP device has 4 RX and 4 TX channels
- Also compatible with electrical cables
- I2C connection to all QSFP modules from Power module
  - Controlled by ZYNQ

X20 POWER MODULE

- Designed in collaboration with Vinca Institute for Nuclear Sciences (Serbia)
  - Vladimir Rekovic (PI)
  - Ana Jelisijevic (Engineer)
- PCB made in US
- Assembly done in Serbia (IRITEL)

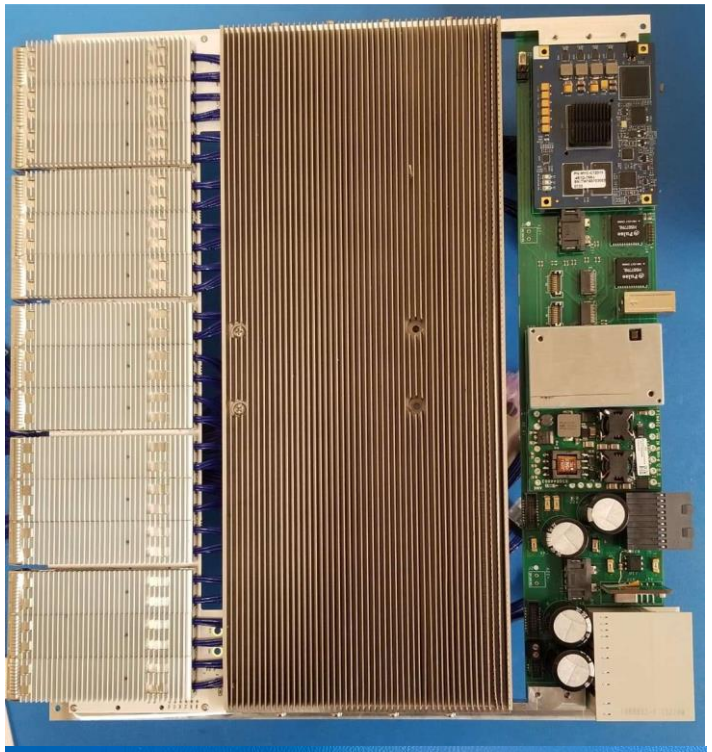
POWER MODULE

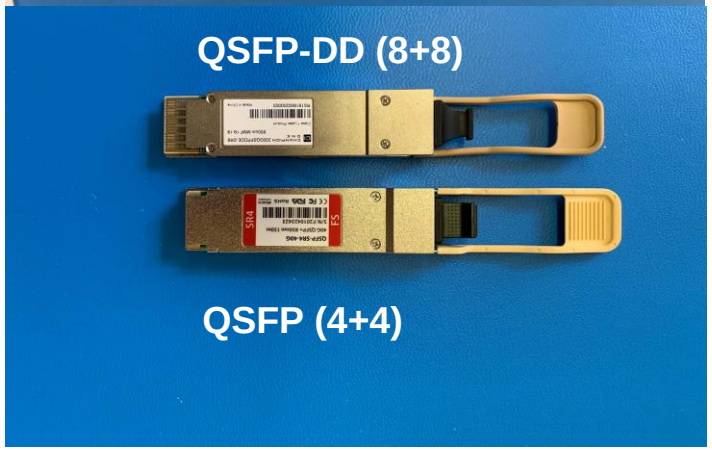
- Functions:
  - Power conversion from -48V to
    - +12V payload
    - +3.3V service
  - ZYNQ Control module
    - CENTOS7 system
    - Main control interface for the board
    - Also runs IPMC software
  - Connections to FPGA modules:
    - LHC clock
    - I2C interfaces
    - Fast AXI links
    - TCDS signals from backplane
    - DAQ path to/from backplane



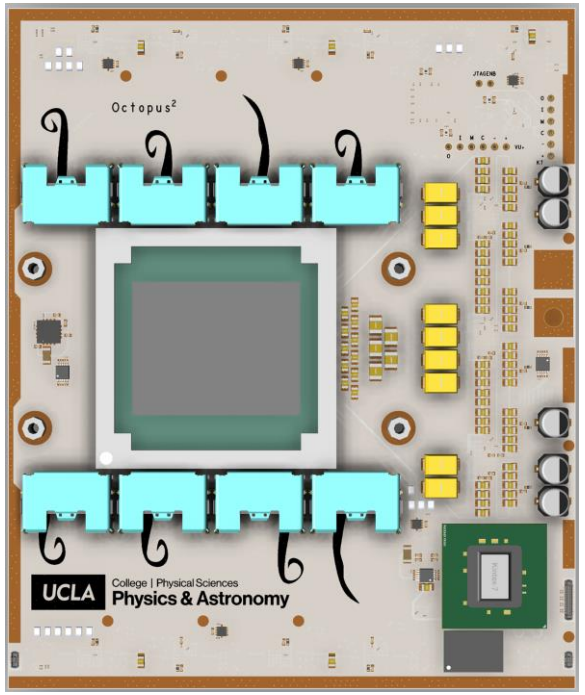
UCLA: X20 - 2577

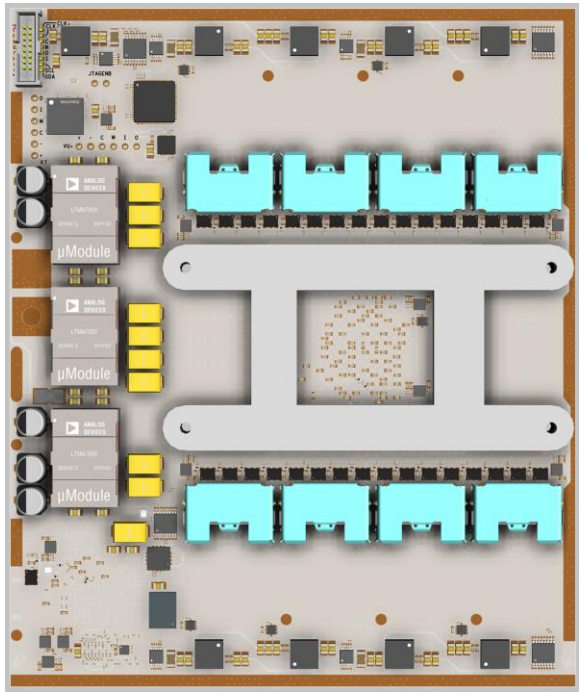
- Variant targeted for intensive processing + high bandwidth applications in the Muon Trigger
  - Supports up to two “Octopus[2]” mezzanines with A2577 package
    - Baseline: 1 given cooling capabilities/constraints in USC
  - Baseline FPGA: VU13P (also VU9P/11P compatible)
  - Much larger FPGA: ~3.3 x KU15P
- 15 cage Optical module with latest QSFP -DD (double-density) optics
  - 8 RX+ 8 TX per pluggable
    - 120 RX+120 TX total
  - Industry standard. Multi-vendor availability and competitive cost
- **Optical module, power module and mechanical parts received and tested**





UCLA: OCTOPUS² MEZZANINE

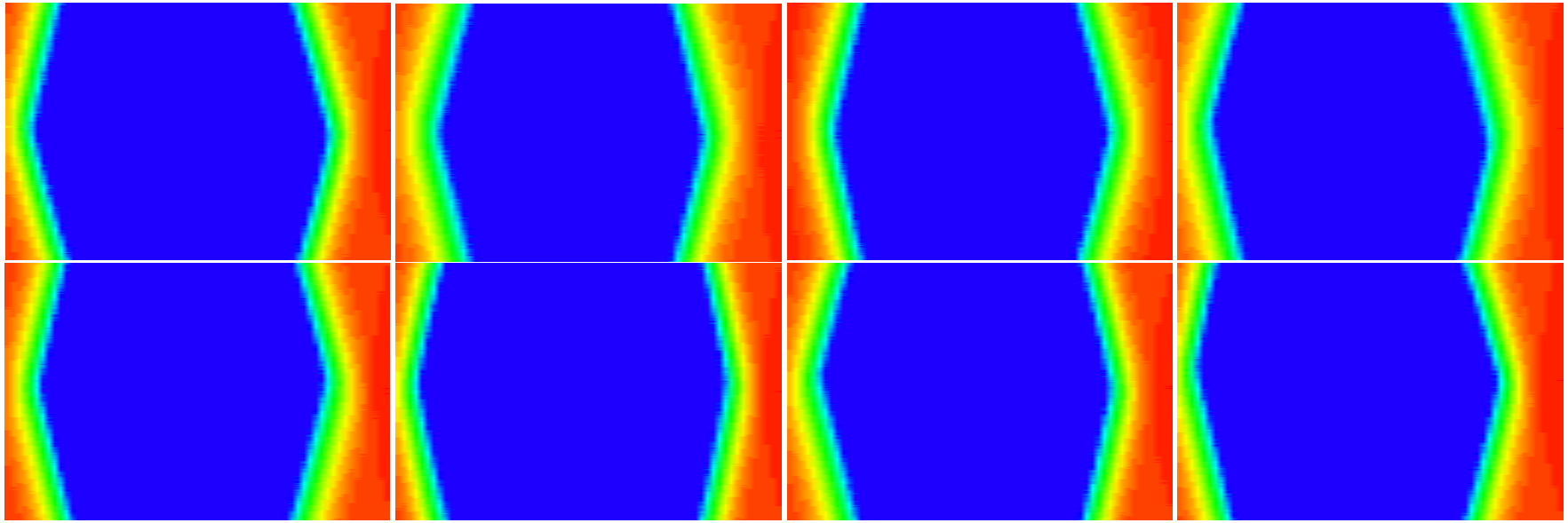




- Small form factor: 12.5 x 15 cm ⟶ Two fit in one ATCA slot
  - Mounts on heatsink
- Uses 8 high speed connectors on each side sending directly the high speed signals to cages through high quality copper [Samtec F-QSFP-DD or F-QSFP]
  - Double sided design provides trace lengths < 1 cm for all 128 links
- Up to 300A of core power
- **PCBs made, boards currently in assembly**

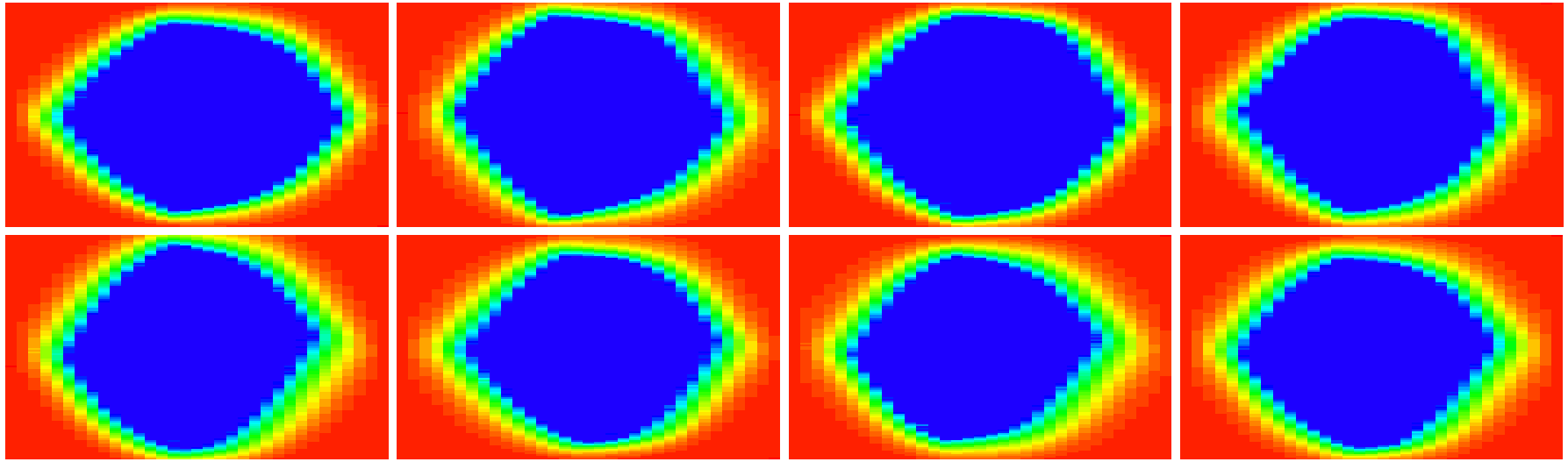
Material interchangeable with Halogen-free material

TESTS WITH QSFP, 25G



- Eyes ,FS modules, 25.78G, PRBS-31, with CDR
- Cannot intentionally disable CDR in these units

TESTS WITH QSFP, 16G



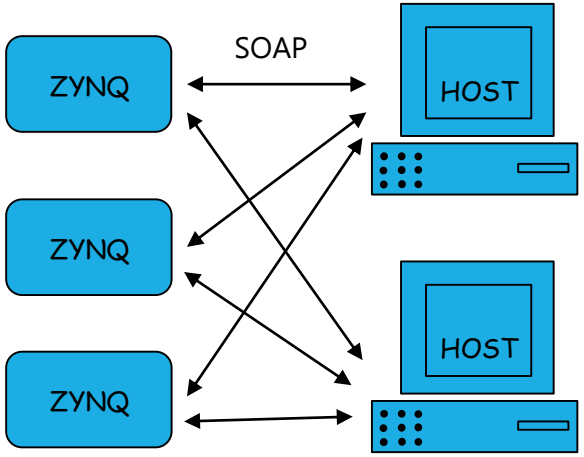
- Eyes, FS modules, 16G, PRBS-31
- At 16G CDR is automatically disabled
- Also tested at 10G with 10G QSFP links

IPMC SOFTWARE

- Derived from Open-source BMC project:
  - http://www.coreipm.com/
- Runs under CENTOS7 and CENTOS8 on ZYNQ module
- Supports all functions necessary for board operation
- Status:
  - All basic functionality implemented and tested
- Embedded Linux system under 32-bit ARM architecture (armv7hl):
  - Petalinux kernel version 2020.1
  - CentOS 8
  - XDAQ version 16 (future release)

XDAQ-CORE ON ZYNQ - 7000 DEVICE

- XDAQ is the CMS framework and library for system configuration, control and monitoring
- Investigated using XDAQ on ZYNQ. Reasons:
  - Would like to use CMS-standard SOAP messaging for communication with ZYNQ devices
  - Minimal rework is needed in existing SWATCH cells and other software
- XDAQ was successfully compiled for ZYNQ-7000 device
  - Thanks for XDAQ team for a lot of help!
- SOAP communication tested successfully



XDAQ process running on ZYNQ

```
[root@localhost xdaq_mgt_application]# ./mgtRun.sh
AsyncDNSResolver: fopen(/etc/resolv.conf) failed: No such file or directory
09 Dec 2020 01:02:08.629 [3020849168] WARN  root <> - Not able to resolve hostnames via DNS on host localhost
09 Dec 2020 01:02:08.631 [3020849168] INFO  localhost.p:33333 <> - xdaq version: 05.05.01, compiled on Nov 28 2020 at 02:22:54, 32bit
09 Dec 2020 01:02:08.633 [3020849168] WARN  localhost.p:33333 <> - cannot open file /etc/default.profile, trying next
09 Dec 2020 01:02:08.633 [3020849168] WARN  localhost.p:33333 <> - cannot open file /root/etc/default.profile, trying next
09 Dec 2020 01:02:08.633 [3020849168] WARN  localhost.p:33333 <> - cannot open file /opt/xdaq/share/default/profile/default.localhost.profile, trying next
09 Dec 2020 01:02:08.634 [3020849168] WARN  localhost.p:33333 <> - cannot open file /opt/xdaq/share/default/profile/default.profile, trying next
09 Dec 2020 01:02:08.641 [3020849168] INFO  localhost.p:33333 <> - Loaded profile: /opt/xdaq/etc/default.profile
09 Dec 2020 01:02:08.648 [3020849168] INFO  localhost.p:33333 <> - core::b2innub version: 02.05.02, compiled on Nov 28 2020 at 02:48:57
09 Dec 2020 01:02:08.653 [3020849168] INFO  localhost.p:33333 <> - core::i2outils version: 04.00.00, compiled on Nov 28 2020 at 02:30:40
09 Dec 2020 01:02:08.666 [3020849168] INFO  localhost.p:33333 <> - core::executive version: 04.01.01, compiled on Nov 28 2020 at 02:43:50
09 Dec 2020 01:02:08.690 [3020849168] INFO  localhost.p:33333 <> - core::pthttp version: 04.06.00, compiled on Nov 28 2020 at 02:31:34
09 Dec 2020 01:02:08.702 [3020849168] INFO  localhost.p:33333 <> - core::ptfifo version: 04.03.01, compiled on Nov 28 2020 at 02:37:43
09 Dec 2020 01:02:08.708 [3020849168] INFO  localhost.p:33333 <> - core::xrelay version: 04.01.00, compiled on Nov 28 2020 at 02:47:55
09 Dec 2020 01:02:08.724 [3020849168] INFO  localhost.p:33333 <> - core::hyperdaq version: 05.03.00, compiled on Nov 28 2020 at 02:47:41
09 Dec 2020 01:02:08.725 [3020849168] DEBUG localhost.p:33333 <> - Create application descriptor for class: executive::Application id: 0
09 Dec 2020 01:02:08.771 [3020849168] INFO  localhost.p:33333.executive::Application.lid(0) <> - Log URL not set (was already console)
09 Dec 2020 01:02:08.771 [3020849168] INFO  localhost.p:33333.executive::Application.lid(0) <> - Changed Log level to INFO
09 Dec 2020 01:02:08.790 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - Adding header Access-Control-Allow-Origin:*
09 Dec 2020 01:02:08.791 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - Adding header Access-Control-Allow-Methods:POST, GET, OPTIONS
09 Dec 2020 01:02:08.791 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - Adding header Access-Control-Allow-Headers:x-requested-with, soapaction
09 Dec 2020 01:02:08.791 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - Adding expire rule image/png:PT4300H
09 Dec 2020 01:02:08.791 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - Adding expire rule image/jpg:PT4300H
09 Dec 2020 01:02:08.792 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - Adding expire rule image/gif:PT4300H
09 Dec 2020 01:02:08.792 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - Adding expire rule application/x-shockwave-flash:PT120H
09 Dec 2020 01:02:08.792 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - Adding expire rule application/font-woff:PT8600H
09 Dec 2020 01:02:08.792 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - Adding expire rule text/css:PT4300H
09 Dec 2020 01:02:08.794 [3020849168] INFO  localhost.p:33333.pt::http::PeerTransportHTTP.lid(1) <> - No security policies on this server
09 Dec 2020 01:02:08.835 [3020849168] INFO  localhost.p:33333 <> - emtf::mgtConfigurator version: 01.00.00, compiled on Nov 30 2020 at 22:56:28
09 Dec 2020 01:02:08.843 [3020849168] INFO  localhost.p:33333 <> - Ready.
```

UF IPMC SOFTWARE (LINUX USER SPACE)

UF IPMC software is based on the Open Source **coreIPM** project (http://www.coreipm.com, source code author: **Gokhan Sozmen**).

Currently UF IPMC already runs on ZYNQ (MYC-C7Z015) on the APEX Power Module.

Current status:

- All basic functionality implemented and tested within ATCA standard.
- Supports access to CONFIG, FRU and SDRs information through config files in human-readable *.toml* format.
- Supports sensor handling in Abnormal Operation Stage (e.g. Temperature sensors)
- Provided usage instruction to add and configure user's custom sensors.
- Supports Power control.

ATCA shelf manager recognizing one of our sensors

```
# clia board -v -x 14

Pigeon Point Shelf Manager Command Line Interpreter

Physical Slot # 14
9c: Entity: (0x0, 0x60) Maximum FRU device ID: 0x00
    PICMG Version 2.3
    Hot Swap State: M4 (Active), Previous: M3 (Activation In Process),
 Last State Change Cause: Normal State Change (0x0)
    Device ID: 0x00, Revision: 0, Firmware: 1.00 (ver 1.0.0), IPMI ver
 2.0
    Manufacturer ID: 000000, Product ID: 7000, Auxiliary Rev: 00000000
    Device ID String: "UF IPMC"
    Global Initialization: 0xc, Power State Notification: 0x0, Device
Capabilities: 0x2b
    Controller provides Device SDRs
    Supported features: 0x2b
        "Sensor Device" "SDR Repository Device" "FRU Inventory Device"
 "IPMB Event Generator"

9c: FRU # 0
    Entity: (0x0, 0x60)
    Hot Swap State: M4 (Active), Previous: M3 (Activation In Process),
 Last State Change Cause: Normal State Change (0x0)
    Device ID String: "UF IPMC"
    Site Type: 0x00, Site Number: 14
    Current Power Level: 0x02, Maximum Power Level: 0x14, Current Powe
r Allocation: 0.0 Watts

# clia sensordata 9c 4

Pigeon Point Shelf Manager Command Line Interpreter

9c: LUN: 0, Sensor # 4 ("TEMP1")
    Type: Threshold (0x01), "Temperature" (0x01)
    Belongs to entity (0xc1, 0x60)
    Status: 0xc0
        All event messages enabled from this sensor
        Sensor scanning enabled
        Initial update completed
    Raw data: 33 (0x21)
    Processed data: 33.000000 degrees C
    Current State Mask: 0xda
        At or Below Lower Critical Threshold
        At or Above Upper Non-Critical Threshold
        At or Above Upper Critical Threshold
```

SENSORS

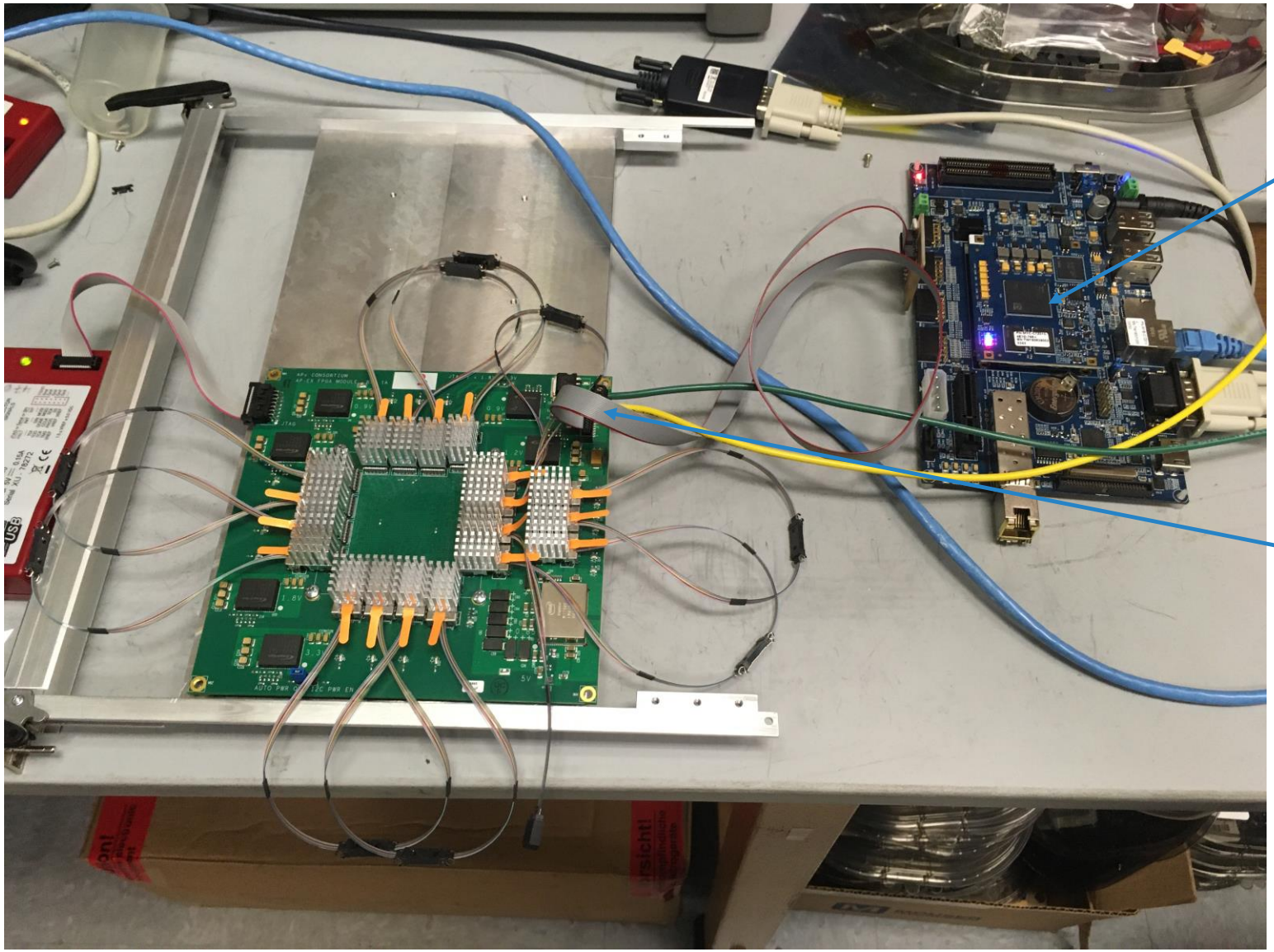
- Users can include their own sensors
- I2C readout
- Adjustable readout period
- Customizable readout procedure
  - User defines programming I2C switches, etc
- Customizable reaction to sensors
- Any sensor can be made available for IPMC readout
- Optimized fast power fault detection capabilities

X20 STATUS

- Prototypes of all modules produced and tested
  - Power module
  - KU15P module
  - QSFP module
- One completely assembled board tested
  - Including thermal tests at full power (~240W)
- Units currently in operation:
  - One in UF
  - One in CERN
  - UCLA has power module, getting ready to test with their FPGA and QSFP-DD modules.
- More KU15P modules in assembly
  - Reworked in collaboration with Vinca Inst. Of Nuclear Sciences.
- Already have more Power and QSFP modules

BACKUP

FULL TEST WITH FIREFLIES

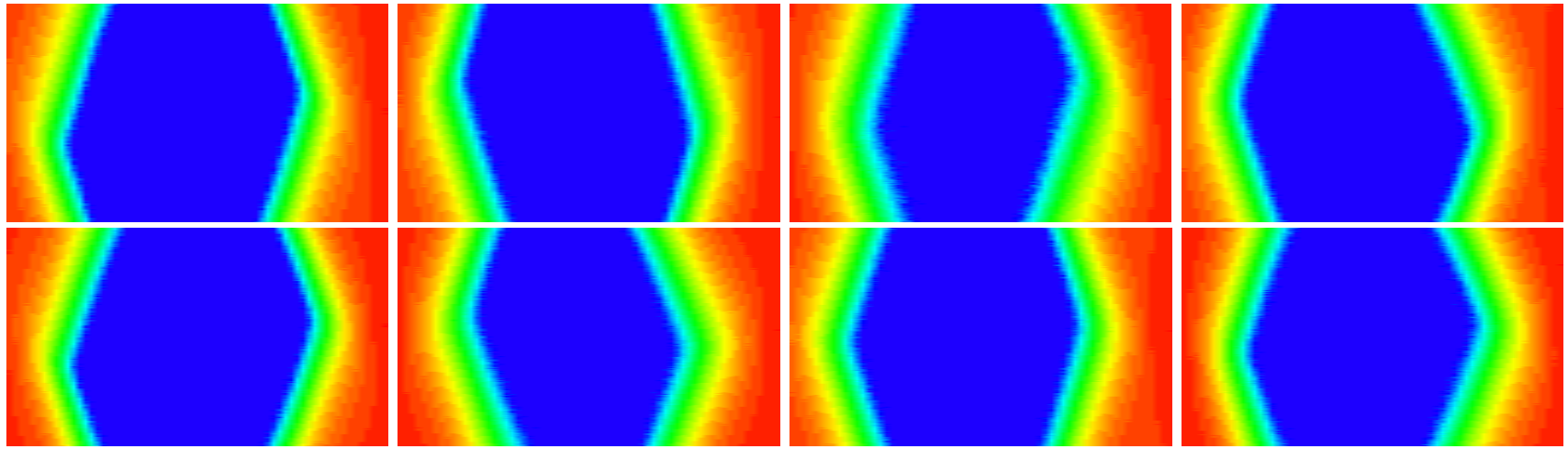


ZYNQ module (on its own evaluation base so far)

Slow control cable:

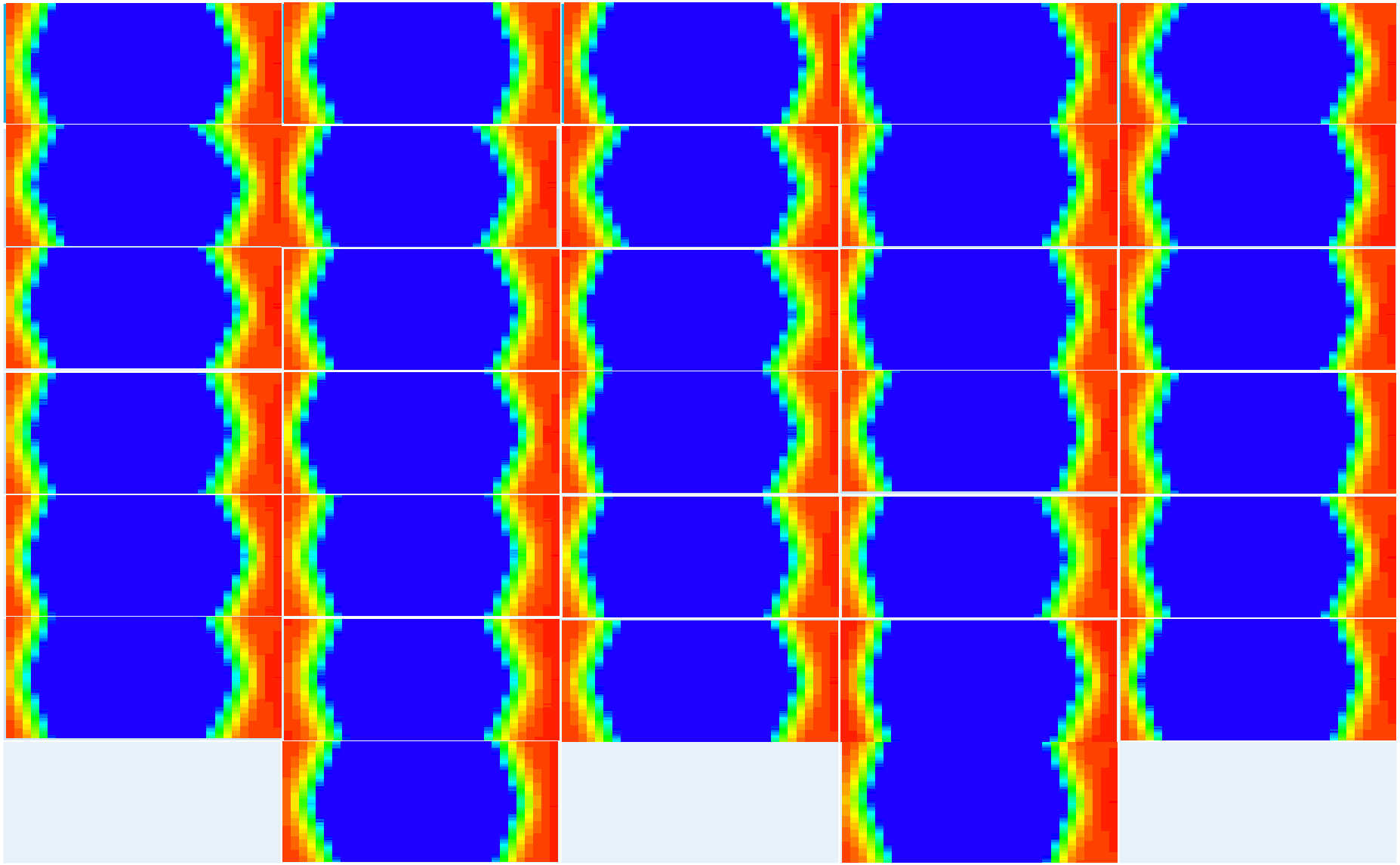
- JTAG
- I^2C
- LHC clock

EYES, FIREFLY 25.78G, NO CDR, PRBS-31, LONGEST PCB LINES

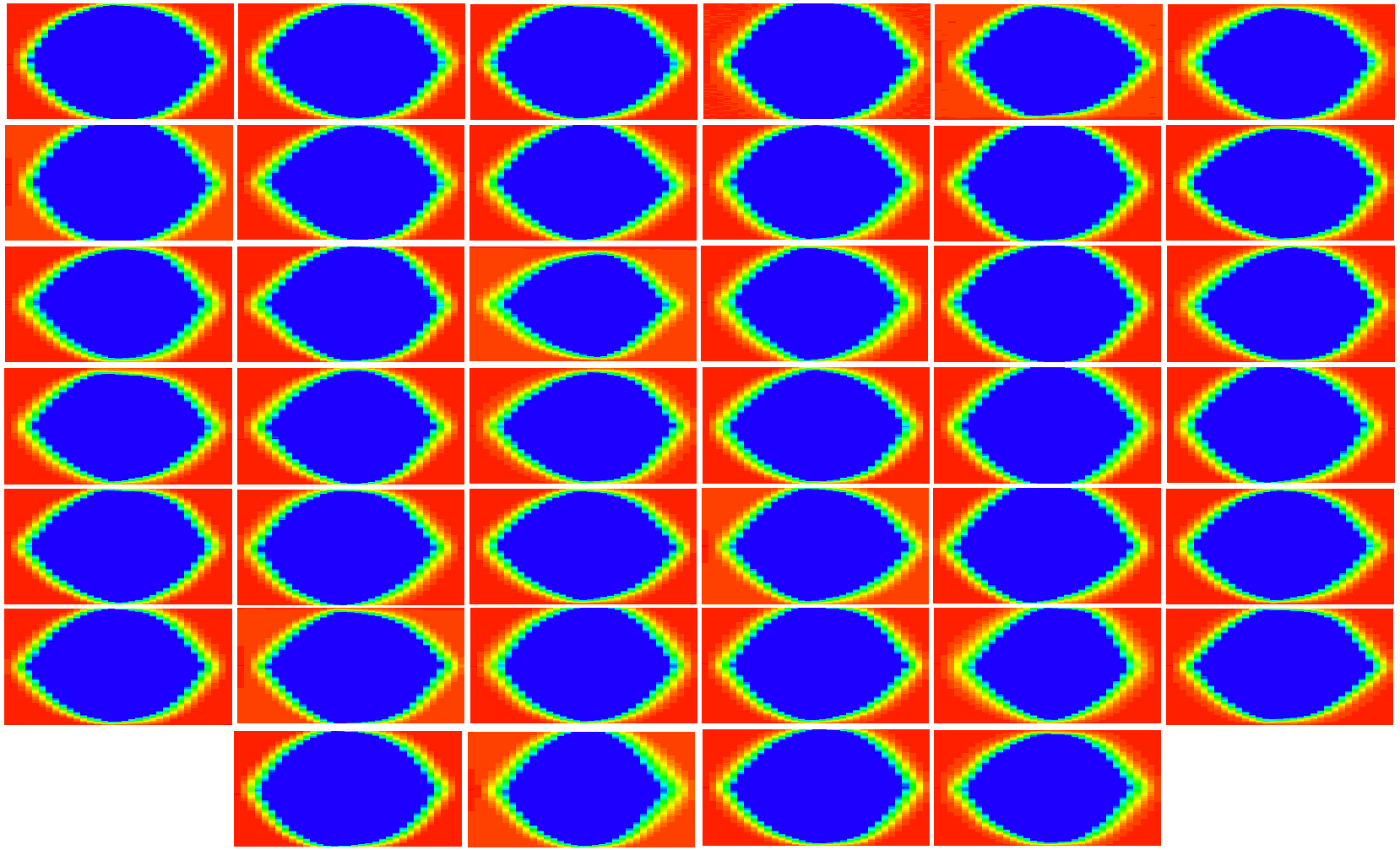


Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	RX Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enable
Ungrouped Links (0)														
Found Links (8)							Reset	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	Multiple	950 mV (11000)	
Found 0	MGT_X0Y4/TX	MGT_X0Y0/RX	25.781 Gbps	1.682E12	0E0	5.944E-13	Reset	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
Found 1	MGT_X0Y7/TX	MGT_X0Y1/RX	25.781 Gbps	1.682E12	0E0	5.944E-13	Reset	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
Found 2	MGT_X0Y6/TX	MGT_X0Y2/RX	25.781 Gbps	1.682E12	0E0	5.945E-13	Reset	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	4.08 dB (01111)	950 mV (11000)	
Found 3	MGT_X0Y5/TX	MGT_X0Y3/RX	25.779 Gbps	1.683E12	0E0	5.943E-13	Reset	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
Found 4	MGT_X0Y1/TX	MGT_X0Y4/RX	25.781 Gbps	1.682E12	0E0	5.947E-13	Reset	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
Found 5	MGT_X0Y2/TX	MGT_X0Y5/RX	25.781 Gbps	1.682E12	0E0	5.947E-13	Reset	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
Found 6	MGT_X0Y3/TX	MGT_X0Y6/RX	25.781 Gbps	1.682E12	0E0	5.946E-13	Reset	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
Found 7	MGT_X0Y0/TX	MGT_X0Y7/RX	25.787 Gbps	1.682E12	0E0	5.946E-13	Reset	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	

EYES, FIREFLY AT 26G, CDR ENABLED, PRBS-31



EYES, FIREFLY 16G, NO CDR, PRBS-31



POWER FAULT DETECTION

- Have to provide power fault detection on payload modules
  - Moderately high speed: 1 ms or so preferable
  - Reading ADC value for each power supply every ms is cumbersome
- Solution: use Power OK flags
- All DC-DC converters provide such outputs
- Payload modules should connect them to a single I2C register
- Reading that register is fairly quick
- Additionally, plan to use interrupt signal from I2C register that reacts to changes
- That allows for extremely fast reaction to faults, if required
  - Purely in firmware, no software involvement
  - Not implemented yet