ETROC: ETL ReadOut Chip for CMS MTD

with few comments on future precision timing & position detector R&D or challenges ahead

Ted Liu (Fermilab)

March 19th, CPAD
Panel Discussion on Fast Electronics for Timing Detectors
ETROC bump-bonded to LGAD,
To handle 16x16 pixels
Each 1.3 mm x 1.3 mm

Requirement:
ASIC contribution to
time resolution < ~40ps
L1 buffer latency: 12.5 us
65nm

Main challenge:
Deal with small signal size
(down to ~6fC, at end of operation)
Low power consumption < 1W/chip
(about ~2-3mW/pixel)

ETROC: ETL ReadOut Chip

Preamp/Disc
low power
TDC

Waveform sampler (monitoring purpose)

ASIC design: FNAL&SMU
(also in collaboration with lpGBT team)
Testing: FNAL/SMU/UC/KN/CNU
with help from Torino/UCSC/ALTIROC teams...
ETROC Development: *divide & conquer*

**ETROC0:** 1x1 pixel channel with preamp + discriminator (submitted Dec 2018)

*The first prototype chip works well and agrees with simulation*

~10ps achieved with charge injection, passed 100MRad TID testing

~30ps achieved in beam test with preamp waveform

**ETROC1:** 4x4 clock tree, preamp + discriminator + TDC (submitted Aug 2019)

*The first full chain precision timing prototype*

Standalone ETROC1 charge injection testing works well and agrees with simulation: The full chain and new TDC and the 4x4 clock tree

~10ps achieved with full chain and over 4x4 array

Bump bonded with LGAD sensor: bema test on going

**ETROC2:** 8x8 → 16x16, the first full size and full functionality prototype

*Design on going, to be ready by end of 2020*

ETROC2 PLL prototype works well

ETROC2 Waveform sampler prototypes works well

The main digital design implemented in FPGA emulator

**ETROC3:** 16x16 (full size & full functionality)

*We have followed this plan since the project started (Sept. 2018) ...*
ETROC building blocks vs sizes (65 nm)

16x16 pixel cell array (1.3mm x 1.3 mm)

Preamp/Disc

low power TDC

81 um X 67 um

90 um X 94 um

467 um X 166 um

Preamp

Discriminator

TDC

300um x 800um

3.2GS/s waveform sampler

FNAL/SMU

For future R&D: 1.3mm x 1.3mm to ~100 um x 100um: a factor of ~170 in pixel size, also power budget if ~1W/chip is still the budget, perhaps also clock distribution by no means straightforward ...

Need to think very hard on system design at all levels to relax ASIC requirements (detector layers, more power/cooling budget, larger pixel size, charge sharing, 28nm/beyond and 3DIC ....)
How could 3DIC help to scale to smaller pixel size for precision position & timing detectors

3DIC Technology

Earlier multi-tier stacking concept for pattern recognition

An open flexible architecture for precision position and timing detector (one example below)

- readout and interfaces
- Hit buffer
- TDC and Clock distribution
- preamp/discriminator
- Sensor pixels (~100 um x ~100um each)

3DIC allows repartition of the design blocks vertically for the whole signal processing chain...
also allows combination of different technologies...
to combine the best of the world (e.g. front-end)

3DIC is promising in the future. For near future, more realistic approach is perhaps to keep the pixel size not too small (a few 100 um x a few 100 um), relax timing requirement per hit, relax power constraint ...

“A New Concept of Vertically Integrated Pattern Recognition Associative Memory”
Backup slides
ETROC power consumption update (TDR/simulation/measured)

Final ETROC0/1 design simulation results vs measured

<table>
<thead>
<tr>
<th>Circuit component</th>
<th>Power per channel [mW]</th>
<th>Power per ASIC [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamplifier (low-setting)</td>
<td>0.67 0.76 0.74</td>
<td>171.5 190</td>
</tr>
<tr>
<td>Preamplifier (high-setting)</td>
<td>1.25 1.31 1.27</td>
<td>320 325</td>
</tr>
<tr>
<td>Discriminator</td>
<td>0.71 0.87 0.84</td>
<td>181.8 215</td>
</tr>
<tr>
<td>TDC</td>
<td>0.2 0.07 0.1</td>
<td>51.2 26</td>
</tr>
<tr>
<td>SRAM</td>
<td>0.35 0.25 (new)</td>
<td>89.6 64</td>
</tr>
<tr>
<td>Supporting circuitry</td>
<td>0.2 0.2 (reserve)</td>
<td>51.2 51</td>
</tr>
<tr>
<td>Global circuitry</td>
<td></td>
<td>200 226.5</td>
</tr>
<tr>
<td>Total (low-setting)</td>
<td>2.13 2.13</td>
<td>745 773</td>
</tr>
<tr>
<td>Total (high-setting)</td>
<td>2.71 2.66</td>
<td>894 908</td>
</tr>
<tr>
<td>Total (highest setting)</td>
<td></td>
<td>2.91 972</td>
</tr>
</tbody>
</table>

- Measurements agree with simulation of ETROC0 and 1 design
  - TT corner numbers shown, mostly agree reasonably well
  - TDC power is assuming 1% occupancy....
    - At 10% occupancy, from 0.1mW to 0.32mW (0.22mW x 256 = 56mW)
    - Will need to add 56mW to the total power IF 10% TDC occupancy.

We are still within 1W/chip spec

Ted Liu, ETROC
3/19/21
Overall expected ETROC performance

**Time resolution**

<table>
<thead>
<tr>
<th>Circuit component</th>
<th>35 ps</th>
<th>40/46</th>
<th>45/50</th>
<th>32/35</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGAD+ preamp/discriminator + TDC bin</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time-walk correction residual</td>
<td>&lt; 10 ps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal clock distribution</td>
<td>&lt; 10 ps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System clock distribution</td>
<td>&lt; 15 ps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Per hit total time resolution</td>
<td>41 ps</td>
<td>45/50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Per track (2 hits) total time resolution</td>
<td>29 ps</td>
<td>32/35</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Power consumption (TDR)**

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*With safety margin: design specification is ~35ps per track (~50ps per hit), < ~60ps per track at end of life (~80 ps per hit)*

*With some safety margin: design specification is ~1W per chip*
From ETROC0 to ETROC1 to ETROC2/3

ETROC0
- Submitted in Dec. 2018
- Analog Front-end
- First round beam test early 2020, reached ~30ps
- Good

ETROC1
- Submitted in Aug. 2019
- 4 X 4 pixel array with full front-end including TDC
- Chips received middle Dec 2019
  - TDC block: good
  - Full chain standalone: good
  - Beam test: just started

ETROC2
- Aim to submit by end of 2021
  - Designed to be compatible with 16 X 16 pixel array with full functionalities
  - Key new design blocks:
    - Waveform sampler:
      - 1st ADC mini-ASIC good
      - 8-channel sampler chips received in May 2020 good
    - PLL: submitted in May 2020
      - Good, passed SEU

ETROC3
- Aim to submit in 2022
- Pre-production version

Since project started Sept 2018, Designed 5 different kinds of prototype chips to address different design challenges: All successful
### Jitter measurements with charge injection

**ETROC0:**
- Charge injection \(\rightarrow\) preamp \(\rightarrow\) discriminator \(\rightarrow\) scope

**ETROC1 4x4 clock (H) tree**
- Charge injection \(\rightarrow\) preamp \(\rightarrow\) discriminator \(\rightarrow\) TDC

#### Leading Edge Jitter at Low Power

<table>
<thead>
<tr>
<th>Injected Charge (fC)</th>
<th>Leading Edge Jitter (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>50</td>
</tr>
<tr>
<td>5</td>
<td>45</td>
</tr>
<tr>
<td>10</td>
<td>40</td>
</tr>
<tr>
<td>15</td>
<td>35</td>
</tr>
<tr>
<td>20</td>
<td>30</td>
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<tr>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>30</td>
<td>20</td>
</tr>
<tr>
<td>35</td>
<td>15</td>
</tr>
</tbody>
</table>

#### Table

<table>
<thead>
<tr>
<th>Row</th>
<th>Col 0</th>
<th>Col 1</th>
<th>Col 2</th>
<th>Col 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>9.60</td>
<td>9.66</td>
<td>11.54</td>
<td>11.42</td>
</tr>
<tr>
<td>1</td>
<td>11.91</td>
<td>9.73</td>
<td>11.37</td>
<td>10.07</td>
</tr>
<tr>
<td>2</td>
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<td>10.84</td>
<td>10.31</td>
</tr>
<tr>
<td>3</td>
<td>10.95</td>
<td>8.76</td>
<td>9.64</td>
<td>9.48</td>
</tr>
</tbody>
</table>

**with bare ETROC1**
ETL precision timing **challenges**

- Low Gain Avalanche Detectors (LGADs)
  - Basic unit: Module (4x6 cm$^2$)
    - 2x4 cm$^2$ LGAD bump-bonded to 2 ETROC ASICs mounted on two sides of cooling plates
  - Two layers/disks per endcap mounted on the HGC nose (~2 hits per track)
  - 50ps per hit $\rightarrow$ 35ps per track
  - $1.6 < |\eta| < 3.0$, +/- 3m surface ~14 m$^2$; ~8.5 M channels
  - Nominal fluence: $1.6 \times 10^{15} n_{eq}/cm^2$ (@ 3000 fb$^{-1}$)

- LGAD gain modest: 10-30
  - Landau contribution: ~30-40ps
  - Front-end contribution kept < ~40ps

- Extract precision timing from
  - small LGAD signal (6fC – 20fC)
  - at end of operation
  - With low power: < 4mW/channel
MTD electronics system
ASIC design: The System Point of View

**ASIC:** Application Specific Integrated Circuit

**ASIC:** A System design that Includes a Chip

Proper System Design is the Key to the success of any challenging ASIC project

A good design is a compromise between system design and ASIC design
Design aspects for precision timing detector

• Design methodology to optimize front-end design from system point of view
• Single layer detector vs multi-layer (ETL design: 1 layer $\rightarrow$ 2 layer)
• System power and cooling constraint and how it influences ASIC design
• Precision clock distribution considerations: from system to detector, to chip, to pixel and to each TDC delay unit
• Design for monitoring and calibration considerations
• Time-frame of ASIC development: “several miniASICs vs. single full ASIC”
• ...

Will not have time to get into these ....

Proper System Design is the Key to the success of any challenging ASIC project

A good design is a compromise between system design and ASIC design
ETRO C status

• ETRO C0
  • Charge injection done
  • Cosmic done
  • Laser testing done
  • TID test to 100Mrads done
  • Beam testing ~30ps achieved in beam

• ETRO C1 (good progress made despite COVID this year)
  • TDC extensively tested: excellent performance (<~6ps resolution)
  • Full array full chain ETRO C1 charge injection testing: results good
  • ETRO C1 and 5x5 LGAD sensor bump-bonded
    • Laser testing followed by beam testing (Feb – April 2021)

• ETRO C2
  • PLL mini-ASIC: initial test results good
  • Waveform sampler prototype: works well
  • ETRO C emulator: design completed, firmware advanced
    • Fast command decoding, pixel DAQ readout, system interfaces
    • The main digital blocks being prototyped in the emulator
  • Clock tree: from ETRO C1 4x4 to ETRO C2 16x16

Only a few highlights shown in the talk .... Due to limited time.
From ETROC0 to ETROC1 to ETROC2/3

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- Key new design blocks prototyped
  - Waveform sampler:
    - 1st ADC mini-ASIC good
  - 8-channel sampler chips good
  - PLL mini-ASIC good

ETROC3
- Aim to submit in Nov 2022
- Pre-production version

Since project started Sept 2018,
Designed 5 different kinds of prototype chips to address different design challenges:
All successful

Ted Liu, ETROC
ETROC0 summary

- Design started Sept 2019, submitted Dec 2019
  - Only three months: design implementation/verification
  - Design was optimized using LGAD simulation from Nicolo
    - For charge from ~20 fC down to 6 fC, or LGAD gain down to ~10

- ETROC0 Testing:
  - Charge injection done
  - Cosmic done
  - Laser testing done
  - TID test to 100Mrads done (all good)
  - Beam testing ~30ps achieved (waveform analysis)
    - Achieved with two independent setups

See backup slides for some details (53-60)
Measured waveforms at the output of the amplifier
Gain of external amplifier: -10

simulated waveforms at the output of the on-chip analog buffer
The analog buffer has a typical gain about 0.7
ETROC0 jitter: measured vs simulation

ETROC0 post-layout simulation vs testing results using 25ps risetime external pulse injection

Summary of the charge injection testing:
Discriminator leading edge jitter measurements agree with chip post-layout simulation

Power consumption for preamp and discriminator all match with simulation

11/4/20
A simple ETROC0 Beam Telescope (3 boards)

Jan-Feb 2020

Simple "suitcase" setup in parasitic mode running at FNAL MTest

120 GeV proton Beam

Ch 3 2 1

3/19/21

Ted Liu, ETROC
A simple Beam Telescope (with 3 HPK-ETROCO0 boards)

Jan-Feb 2020

Simple "suitcase" setup in parasitic mode running at FNAL MTest

\[
\sigma_2 = \sqrt{0.5 \cdot (\sigma_{21}^2 + \sigma_{32}^2 - \sigma_{31}^2)}
\approx 33 \text{ (ps)}
\]

April – May 2020 parasitic run cancelled due to COVID-19

Ch1/2/3 waveforms

120 GeV proton Beam

3/19/21
MTD Beam Test Setup at FNAL MTest

- HPK-ETROC0 testing with **full tracking**
- MTD Beam Test Setup at FNAL MTest
  - Independent scintillator provides trigger
  - Telescope provides proton track
  - Oscilloscope saves waveforms
  - Study $\Delta t$(LGAD,MCP)

Cold box
- LGAD boards on cooling blocks
- MCP (Photek) time reference
ETROC0 with waveform analysis
Feb 2020

Strip and Pixel Telescope

HPK-ETROC0 testing with full tracking

MTD Beam Test Setup at FNAL MTest
- Independent scintillator provides trigger
- Telescope provides proton track
- Oscilloscope saves waveforms
- Study $\Delta t$(LGAD,MCP)

$\sigma = 31$ ps
ETROCO0 testing beam results

Preamp performance with beam data
ETROC0 test beam result

Using discriminator output

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**CMS Preliminary**

FNAL TB Feb 2020, HPK 3.1, ETROC0

- HPK 3.1, 1.3x1.3 mm²
- ETROC0 Discriminator output
- $\alpha_{\text{photek}} = 8$ ps, subtracted

**Graph:**

- Low power, -20C
- Low power, 20C
- High power, -20C
- High power, 20C

**Legend:**

- Time resolution after TOT correction, with photek contribution subtracted

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3/19/21

Ted Liu, ETROC
ETROC1 pixel: uses ETROC0 front-end

ETROC0 is used directly in ETROC1

The TDC is brand new design (has to be ultra low power)
~ one year development effort
ETROC1

- Design started Jan 2019, submitted in Aug 2019
  - Main new component: brand new TDC
    - Specially developed for ETROC application: ultra low power consumption
  - First attempt with H tree clock distribution over 4x4 array
  - Full chain: preamp + discriminator + TDC + readout
    - *First full chain precision timing prototype*

- ETROC1 testing
  - TDC: *excellent performance (<~6ps resolution)*
  - Full array full chain ETROC1 charge injection: *good*
  - ETROC1 and 5x5 LGAD sensor *bump-bonded*
    - *Laser testing (on going) followed by beam testing (Dec – Feb 2021)*

*A few highlights shown next, will skip some slides during the talk*
ETROC1 TDC Design

• TDC requirements
  • TOA bin size < ~30ps, TOT bin size < ~100ps
  • Lower power highly desirable
    • *ETROC TDC design goal:* < 0.2mW per pixel

• ETROC TDC design optimized for low power
  • A simple delay line without the need for DLL’s to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time

• *In-situ delay cell self-calibration technique*
  • For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
  • Crucial to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)
Self-Calibration: Twice-Recording Method

- Each hit registered twice at two consecutive clock edges
- Use known clock period for “on the fly” self-calibration of delay line

The two measurements can be used:
- to calibrate the delay.
- to reduce digitization errors.

Animation by Jin-yuan Wu (FNAL EE Engineer)
The TOA vs the threshold look reasonable.
- The higher the threshold, the late the discriminator fires (smaller TOA Code)
- With one feature observed:
  - When the threshold is approaching the peak, the TOA/TOT/Cal are not well determined, which is not unexpected
  - Some of the discriminator pulses didn’t reach to ‘high’ level due to the small inputs
  - Usually accompanied by wrong Cal value
- In real operation, this would only happen to very small signal

PA in default gain, low power

**Time of Arrival (TOA) with charge injection**
TOA mean and std

With sensor bump-bonded
On a different board/chip (pixel 0)
Now with sensor capacitance loaded

Bare ETRCO1, pixel 13
- 1 LSB = 18 ps
- PA in default gain, low power
ETROC1 TOT mean and std with charge injection

Performance as expected
Jitter vs Laser intensity: initial result

Preliminary results

Preamp at low power

Laser -> preamp -> discriminator -> TDC

*Testing on going, being improved ....*
ETROC bump-bonded to LGAD,  
To handle 16x16 pixels  
Each 1.3 mm x 1.3 mm

Requirement:  
ASIC contribution to  
time resolution < ~40ps  
Deal with small signal size  
(down to ~6fC, at end of operation)  
Power consumption < 1W/chip  
(about ~2-3mW/pixel)

L1 buffer latency: 12.5 us  
65nm

ETROC: ETL ReadOut Chip

Preamp/Disc  
low power  
TDC

16x16 pixel cell array

clock distribution  
all the way  
into each pixel

Waveform sampler (monitoring purpose)

ASIC design: FNAL&SMU collaboration  
Testing: FNAL/SMU/UIC/KNU/CNU  
(in collaboration with lpGBT team)
Measured TOA bin size based on self-calibration (online)

320 MHz period (3.125ns) / 18ps ~ 174

- ~18 ps bin size from the calibration code
- Good uniformity among pixels

**Performance as expected**
ETROC1 Beam Telescope design

Just like ETROC0 telescope, in a suitcase, simple setup
ETROC1 Beam Telescope

- **Hardware setup**
  - Three-boards beam telescope
  - Trigger on one board (e.g. B1) and record data from all three boards, and study single pixel timing resolution with $\Delta(t_i - t_j)$
  - Clock distribution and data readout among different boards must be synchronized

Bare ETROC1 works well: see [ETL front-end: ETROC](#) at the MTD Annual Review in 10/2020
Single board DAQ system working
3-board telescope DAQ firmware is being tested now
Dedicated beam time starting this Wed (Feb 3rd, 2021)
LGAD + ETROC interface

ETROC1

Guard-rings: Floating or/and at ground

Gain layer

n-silicon Inversion layer

p-stop floating

Positive charged traps

p-n junction

oxide

pad n contact

p-bulk

HV = -200V

front end electronics

bump connection

particle track
### Requirements for the ASIC

**ATLAS HGTD: ALTIROC spec**

Key requirement: Time resolution per track, combining multiple hits, is 30 ps at the start of lifetime to 50 ps after 4000 fb⁻¹ => Time resolution /hit must be < 35 ps at start and 70 ps at the end of lifetime.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum jitter ($\sigma_{\text{elec}}$)</td>
<td>25 ps at 10 fC at the start of the HL-LHC and 70 ps for 4 fC at the end</td>
</tr>
<tr>
<td>TDC contribution</td>
<td>&lt; 10 ps</td>
</tr>
<tr>
<td>Time walk contribution</td>
<td>&lt; 10 ps</td>
</tr>
<tr>
<td>Clock contribution</td>
<td>&lt; 15 ps</td>
</tr>
<tr>
<td>TDC conversion time</td>
<td>&lt; 25 ns</td>
</tr>
<tr>
<td>Clock phase adjustment</td>
<td>100 ps</td>
</tr>
</tbody>
</table>

- **PAD size**: $1.3 \times 1.3 \text{ mm}^2 \times 50 \mu\text{m}$ => $C_{\text{det}} = 4 \text{ pF}$
- **ASIC size and channels /ASIC**: 2x2 cm² 15x15=225 channels/ASIC
- **Single PAD noise (ENC)**: < 3000 e⁻ or 0.5 fC
- **Minimum threshold**: 2 fC
- **Dynamic range**: 4 fC to 50 fC

- **TID Tolerance**: 2 MGy (inner modules replaced after each 1000 fb⁻¹, middle ring after 2000 fb⁻¹)
- **Full chip SEU probability**: < 5 % / hour
- **Trigger rate (latency)**: 1 MHz L0 (10 μs) or 0.8 MHz L1 (35 μs)
- **e-link driver bandwidth**: 320 Mbit/s, 640 Mbit/s and 1,28 Gbit/s

**Voltage and Power dissipation per ASIC**: 1.2V and 300 mW cm⁻² => 1.2 W/ASIC (225 ch) or 4.4 mW/channel and 200 mW for the common part

**Main contributors to time resolution**

$$\sigma_{\text{hit}}^2 = \sigma_{\text{Landau}}^2 + \sigma_{\text{clock}}^2 + \sigma_{\text{elec}}^2$$

with $$\sigma_{\text{elec}}^2 = \sigma_{\text{Time walk}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{TDC}}^2$$

ASIC designed in CMOS 130 nm