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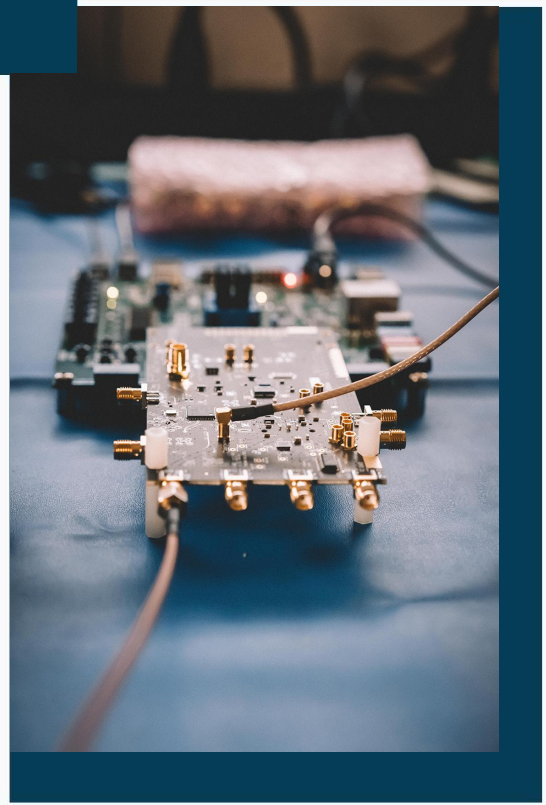

FAST ELECTRONICS FOR LGADs

CPAD MEETING
FAST ELECTRONICS FOR TIMING DETECTORS

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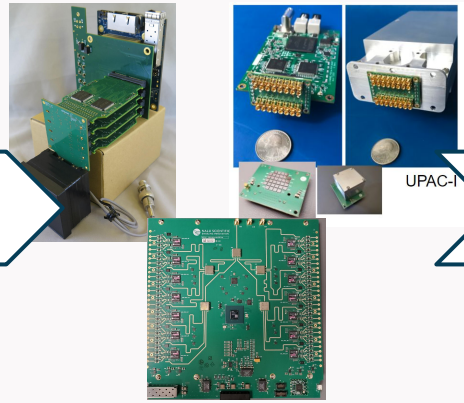
Work partially funded by various US DOE SBIR Awards

TECHNOLOGY

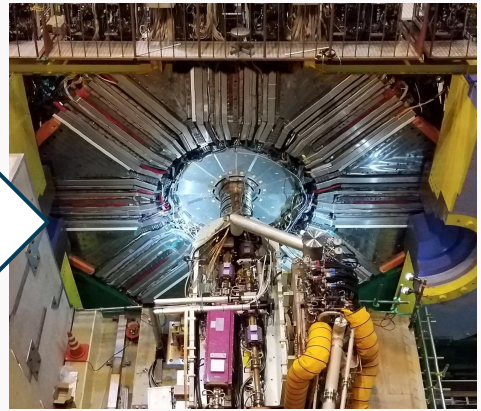
Waveform Digitizing for Time of Flight Detection:
COMPACT, LOW COST, LOW POWER

OUR TECHNOLOGY

INTEGRATION



APPLICATIONS



VARIOUS FRONT-END CHIPS

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP
- Low cost
- User friendly

SENSORS

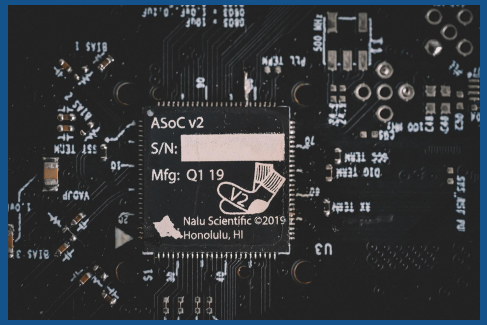
- SiPM
- PMT
- LAPPD
- Antenna arrays

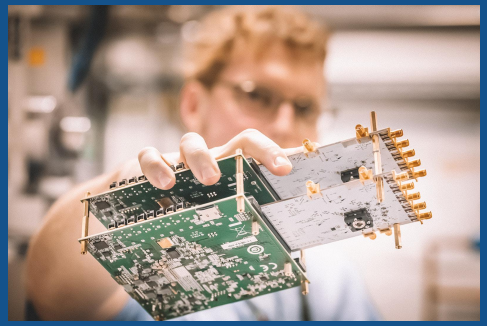
MAIN APPLICATIONS

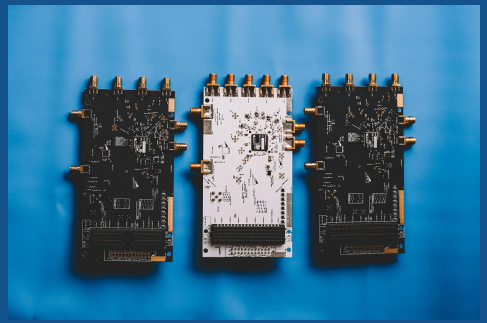
- HEP/NP Readout

SECONDARY APPLICATIONS

- Electron collider experiments
- Beam diagnostics
- Plasma/Fusion diagnostics
- Lidar







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ABOUT NALU SCIENTIFIC

Fast Growing Startup in Honolulu, HI
- $11M in committed funding (US DOE SBIRs, contracts)
- 15 Employees

Integrated Circuits Design
- Analog + digital System-on-Chip (SoC)
- Mixed mode design

Hardware Design
- Field Programmable Gate Arrays (FPGA)
- Complex RF multi-layer Printed Circuit Board (PCBs)

Expertise in:
- Fast timing
- Radiation detection
- Readout electronics for Particle Physics

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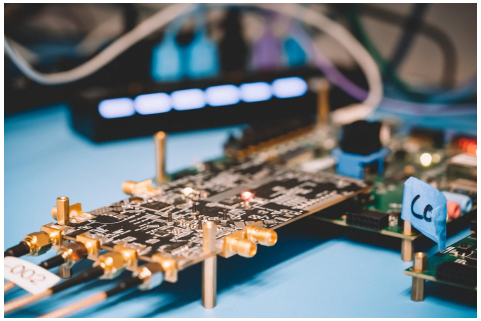
Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	4k	64	80-120	Mar'21
AARDVARC	8-14	2.5	32k	4-8	4-8	Rev 3 avail
AODS	1-2	1	8k	1-4	100-200	Rev 1 avail
STRAWZ	4-6	1.5	4k	64	5-10	2022

- **ASoC**: Analog to digital converter System-on-Chip
- **HDSoC**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option
- **STRAWZ:** Streaming Autonomous Waveform-digitizer with Zero-suppression



All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.

The AC-LGAD Challenge

1. Newly introduced AC-LGADs:
   a. Thin Finely segmented detector
   b. 20- 300 um footprint,
   c. 180 ps rise time
2. Is WFD beneficial? Maybe!
   a. First need to shrink WFD => HPSoC
   b. WFD may enable PSD, charge sharing, etc
   c. WFD may reduce overall need for fine pixels
   d. Preliminary feature extraction on chip
3. Lots of unknowns: Readout, Packaging, Scaling, etc
4. Smaller nodes also attractive: 22, 28nm

Table 1. State of the art readout ASICs with or without waveform storage and/or digitization capability, compared
[1] requires a patented calibration mechanism; [2] in a future revision; [3]chip currently fabricated; [4]chip in design stage; [5]effectively much larger with virtualization

Name	Tech. (nm)	#Ch	Speed (GSa/s)	Buffer Depth (samples)	Power/ch (mW)	Accuracy (uncorrected/corrected)	ADC	Features	Commercial?
SST [SST]	250	4	2	256	40	4.3 ps/2.37 ps	No	-	No
DRS4 [DRS4]	250	9	5	1024	17.5	10ps/1.8ps[1]	No	-	Yes
PSEC4 [PSEC4]	130	6	4-15	256	16.7	1.9 ps	yes	-	No
SAMPIC [Samp]	180	16	3-8.4	64	11.3	35 ps /5 ps	Yes	-	No
LAB4D [LAB4D]	250	1	4	4096	240	10 ps	Yes	-	No
IRSX [IRSX]	250	8	2.8	32768	125	18 ps	Yes	-	No
SiREAD [SiREAD]	250	32	1	2048	40	<100 ps	Yes		Yes
AARDVARC [AARDVARC]	130	4/8	10-15	32768	70	<5 ps at 13.8Gsa/s	Yes	Feature Extraction [2], Self Calibration, Serial	Yes
HdSoC[3]	250	64	1-2	2048	20	<100 ps	Yes	Feature Extraction, Serial	Yes
STRAWZ[4]	65	64	5	2048[5]	<20	<10 ps	Yes	Filtering, Feature extraction, Zero suppression, streaming	Yes
HPSoC	**65**	**100+**	**10+**	**256[5]**	**<2**	**<5 ps**	**Yes**	**Easy integration with sensor arrays, pre-amplification, feature extraction, channel fusion**	**Yes**

Let's connect!

- We have several interesting HEP/NP electronics projects
- We would love to get feedback from end users like you.
- Check us out and follow our updates::
  - Our website: www.naluscientific.com
  - LinkedIn: https://www.linkedin.com/company/naluscientific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