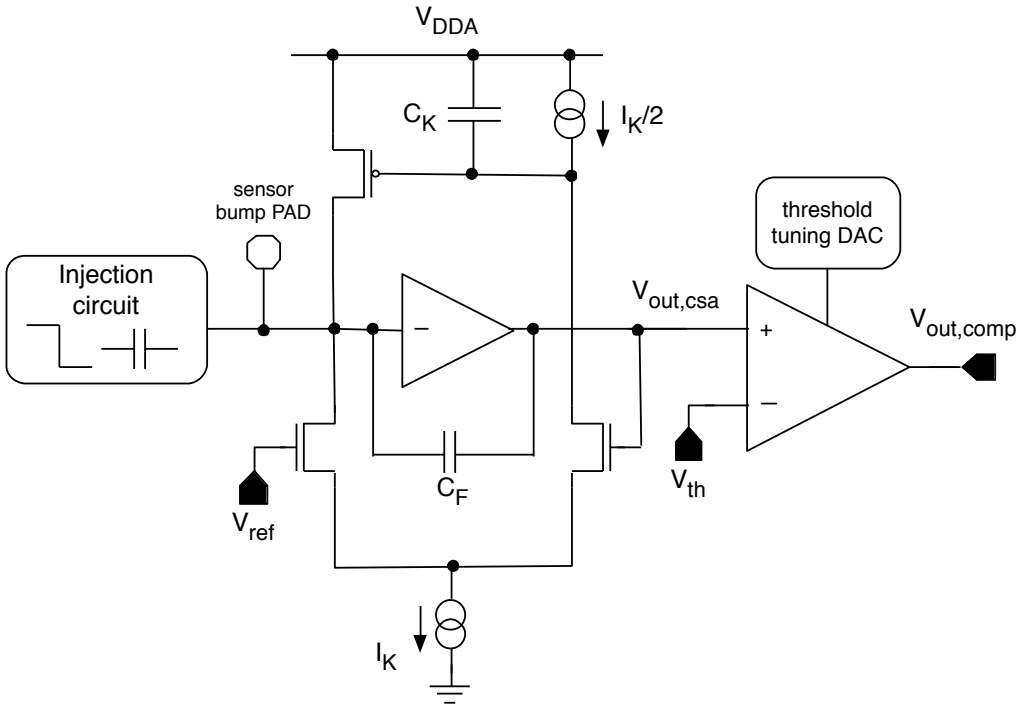
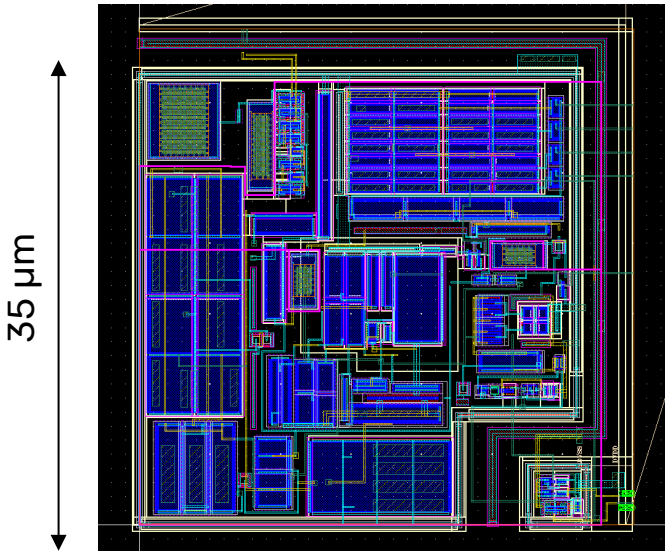
Porting the RD53 Linear front-end in 28nm



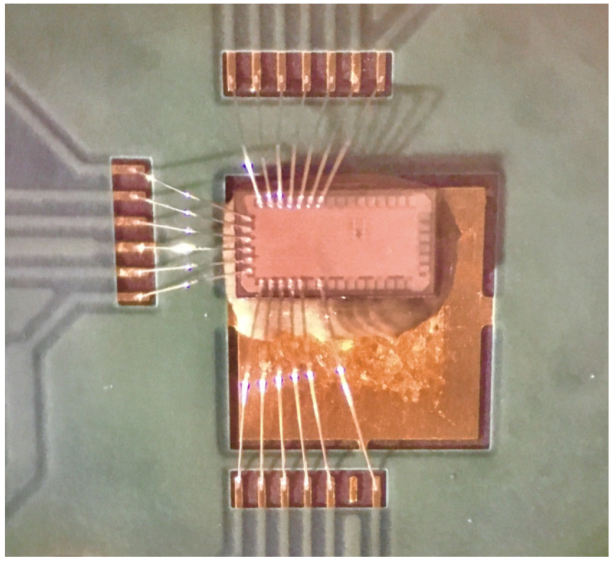
Layout for RD53A

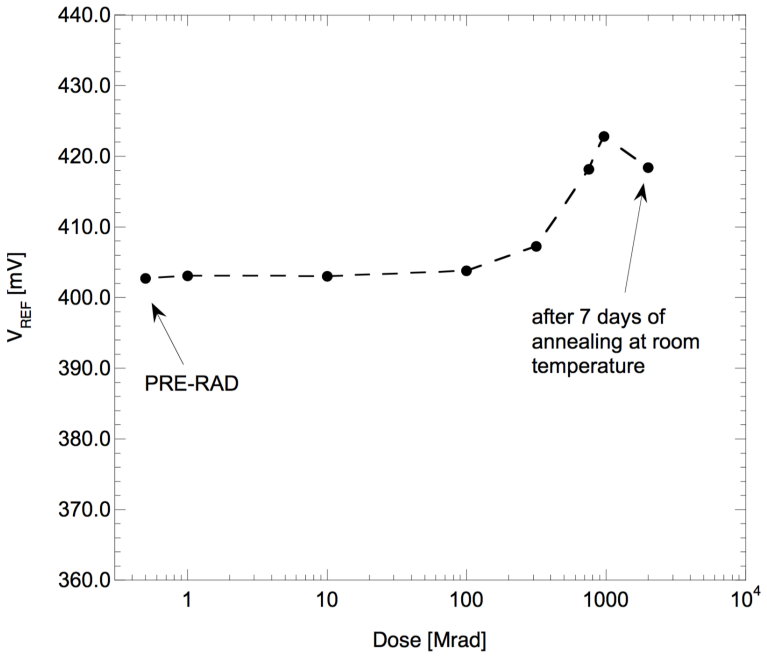


- One stage Krummenacher feedback to comply with the expected large increase in the detector leakage current
- Low power asynchronous current comparator combined with a 40 MHz Time-over-Threshold (ToT) counter for digitization of the signal
- 5 bit local DAC for threshold tuning
- Redesign of the analog front-end with the 28nm CMOS technology (target 25x25um^2 - 20x20um^2)

Building Blocks in 28nm

- A current-mode, rad-hard bandgap has been designed and characterized within the RD53 collaboration
- A modified version, able to withstand a voltage supply of 2V (with core MOSFETs only) has been developed for the SLDO circuit
- Prototypes have been irradiated up to 1Grad with moderate variation (≈ 5%) of the reference voltage
- Redesign of the BGR with the 28nm CMOS process
- The design of a trimming DAC for bias purpose is also foreseen





Previous activity with the 28nm CMOS process

- LVDS driver and receiver have been designed with the HPC 28nm CMOS technology in the first prototype ASIC of the TimeSpot project

- A loopback (RX and TX) has been characterized up to 1Gbps with good results