FaLaPHEL

Fast Links and RadHard Front End with Integrated Photonics and Electronics for Physics

INFN funded project 2021-2023
830 kEuros
35 people and ~13 FTE

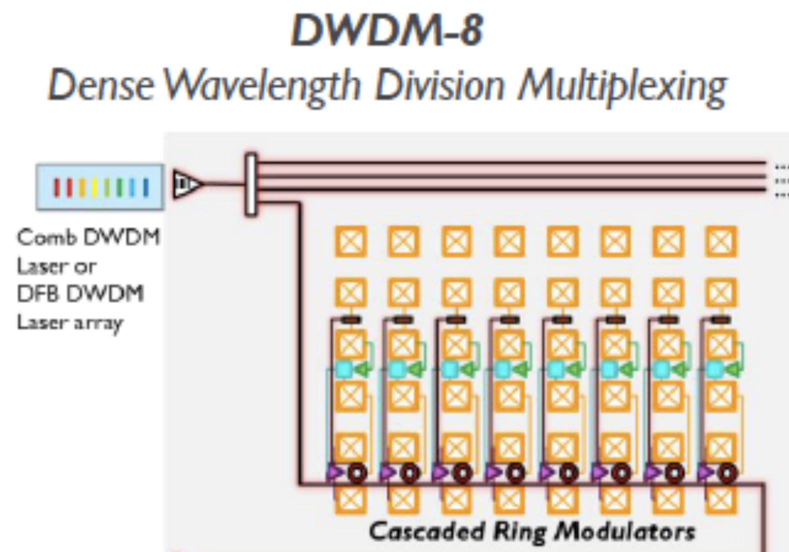
Participant institutes (and group leaders)

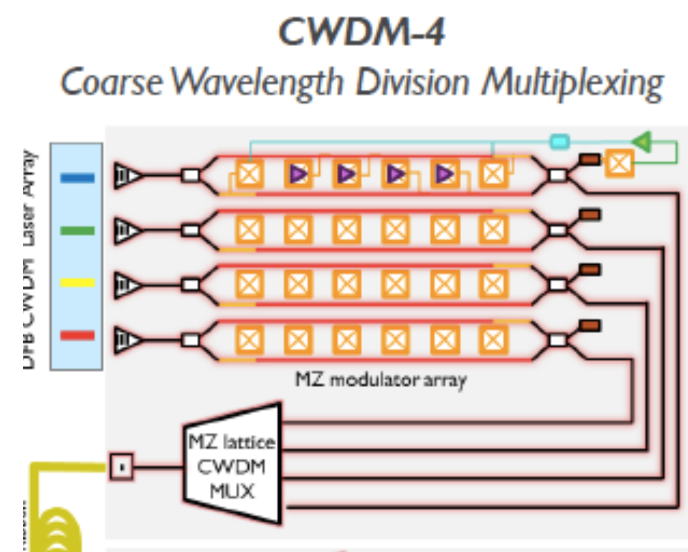
INFN Padova (S. Mattiazzo)
INFN Pavia (L. Gaioni)
INFN Pisa (**F. Palla - P.I.**)
Scuola Superiore S. Anna di Pisa (S. Faralli)
Dip. Ingegneria Informazione UniPisa (S. Saponara)
Dip. Fisica UniMilano (V. Liberali)

Fabrizio Palla - INFN Pisa

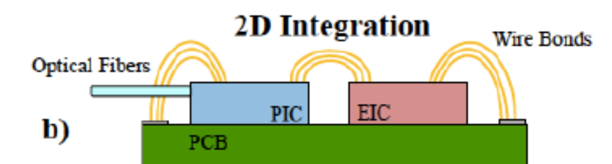
FALAPHEL in short

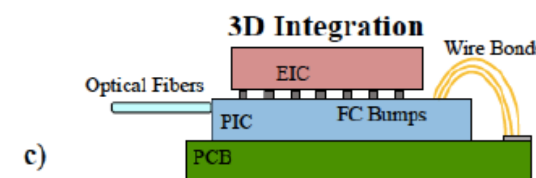
- Development of high-speed and rad-hard Silicon Photonics modulator and 28 nm electronics chips
- Hybrid (3D or 2.5D) integration of Photonic and Electronic chips
  - Aggregated 100 Gb/s links using wavelength division multiplexing or spatial division multiplexing (4 wavelengths)
  - Integrated Front-End electronics

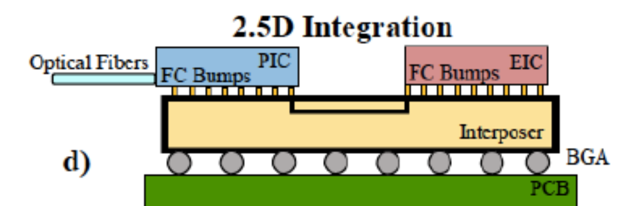




- Parasitic 3D (flip chip) < 2.5D (interposer) < 2D (wire bonds)







plans more in detail ...

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- This project will investigate innovative circuit and system solutions for system-in-package integration of SiPh optical devices and subsystems (high-speed Mach-Zehnder modulators and ring resonator modulators) and high-speed electronics for high rate data transmission (SerDes, Drivers, PLL-based frequency synthesis and data/clock recovery and Front-End) designed to be radiation hard for HEP applications. Moreover, the project will develop front-end blocks (preamplifier, discriminator for A/D conversion, buffering and readout logic) in view of the integration of a matrix of pixel cells in a readout ASIC where data are transmitted off–chip by the high-speed data links.

- We will use the 28 nm TSMC technology node that enables high modulation speeds, low power and promises sufficient radiation hardness to include front-end electronics for inner silicon pixel layers of hadronic colliders. SiPh die will use suitable technology, as the one from IMEC platform that co-integrates a wide variety of passive and active optical components. Hybrid integration of the two dies, such as flip-chip techniques, will be studied, addressing the issues of efficient thermal management and its testability.

- The goal is to fabricate a demonstrator capable of operating at extremely high dose levels (1 Grad), and 100 Gb/s data rate, using wave/space division multiplexing techniques.

28 nm electronics deliverables

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- WP3 (Electronics) design of the fundamental rad-hard and high-speed electronics and test boards
  - Serdes
  - Drivers (targeting 25 Gb/s)
  - Tune circuits
  - PLL/CDR
  - Front-End circuits (preamplifier, discriminator for A/D conversion, buffering and readout logic)
  - DAC/Bandgap

Demonstrator

- Inspired from SIPHOSPACE (ATTRACT) and PHOS4BRAIN (INFN) R&D projects

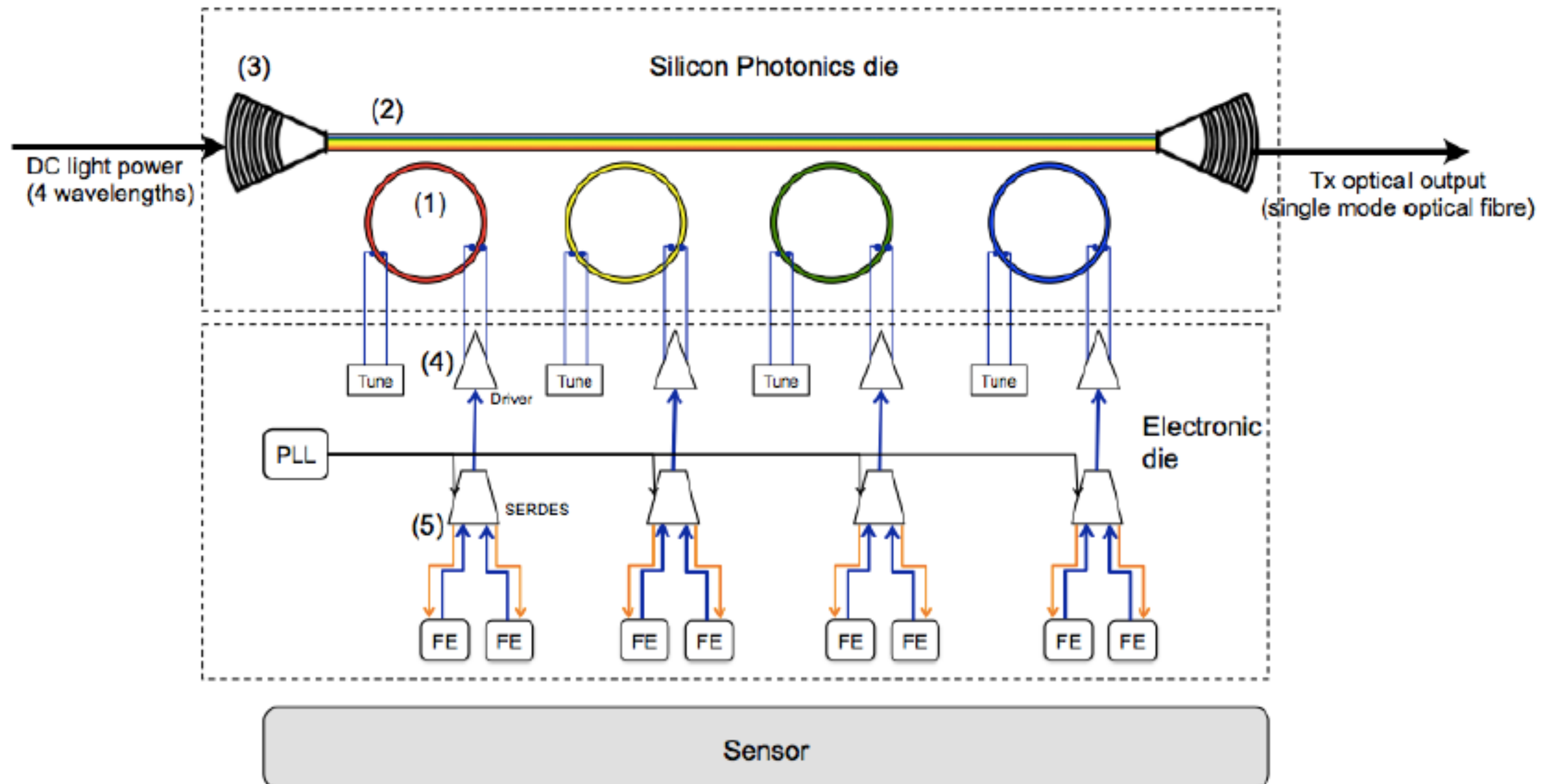

Fig. 2. Schematics of proposed demonstrator. Ring resonators (1) with different and tunable resonator wavelengths are located along horizontally drawn bus waveguides (2) which are connected to optical glass fibres by efficient and robust focusing grating couplers (3). Data from the front-ends (FE) and serializers (5) are sent to the drivers (4). The Front-End (FE) is embedded in the demonstrator but it can be bypassed. The sensor is not part of the demonstrator.

FALAPHEL focus for today

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- Gianluca Traversi (University of Bergamo and INFN Pavia)

  - Analogue circuits: focus on front-end plans in 28 nm

- Gabriele Ciarpi (INFN Pisa)

  - Digital circuits: focus on 28 nm high-speed modulator driver and VCO.

THANK YOU