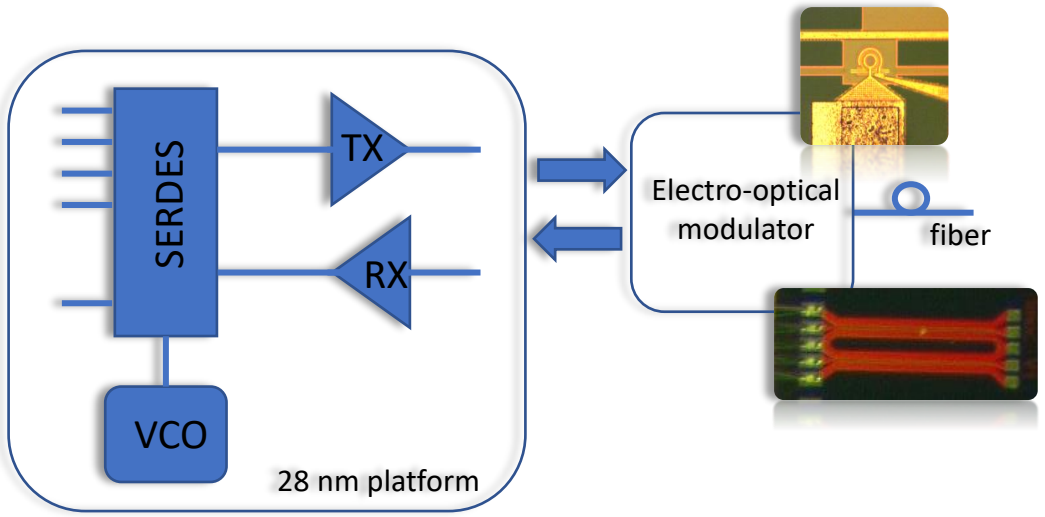
High-speed digital data communication in FALAPHEL project

28 nm vs. *65 nm* technologies for high-speed data communication:

- Higher cut-off frequency ☺
- Lower area ☺
- Lower power ☺
- Higher radiation tolerant ☺
- Greater effects of parasitic elements ☹
- Higher fabrication cost ☹

High-speed architecture:



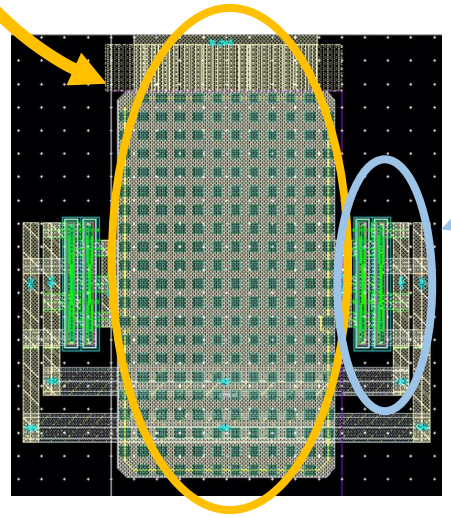
High Frequency PADs and ESD protections in 28 nm

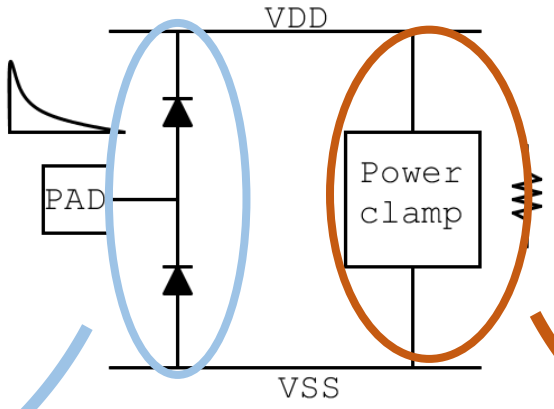
Motivations:

- PADs and ESD protections are not provided by TSMC
- High-speed signals require low capacitance pads and protections
- ESD protections are moving from 2 kV to 500 V HBM levels

Submitted on 28/10/20

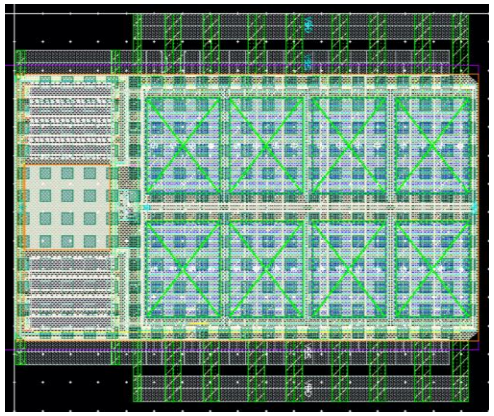
Aluminum wedge bonding pad



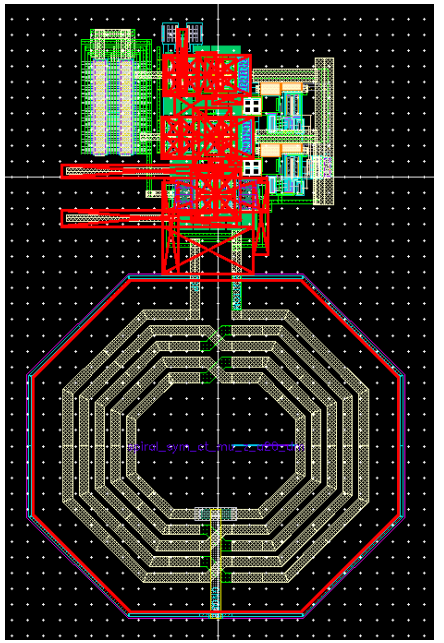


1 kV and 2 kV HBM ESD
(Low capacitance)

Low impedance Power Clamp

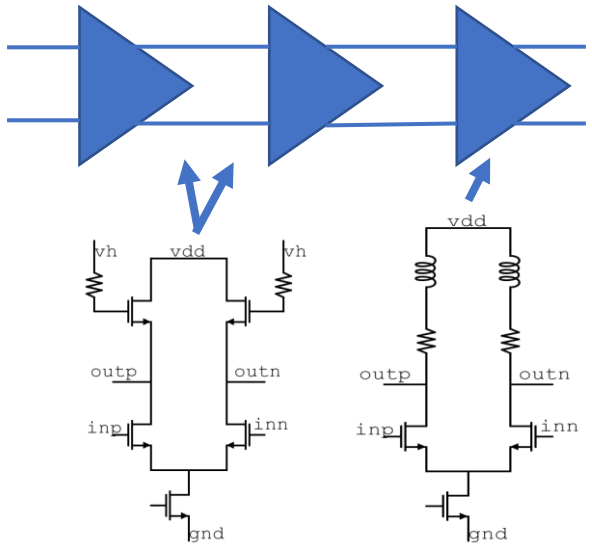


25 Gb/s Ring Resonator Driver in 28 nm



Motivations:

- High-speed communication on optical fibers
- Silicon Photonic as promising technology for electro-optical modulation
- 28 nm technology to reduce the gap with the optical speed
- P-type MOSFETs avoided for radiation hardness increment



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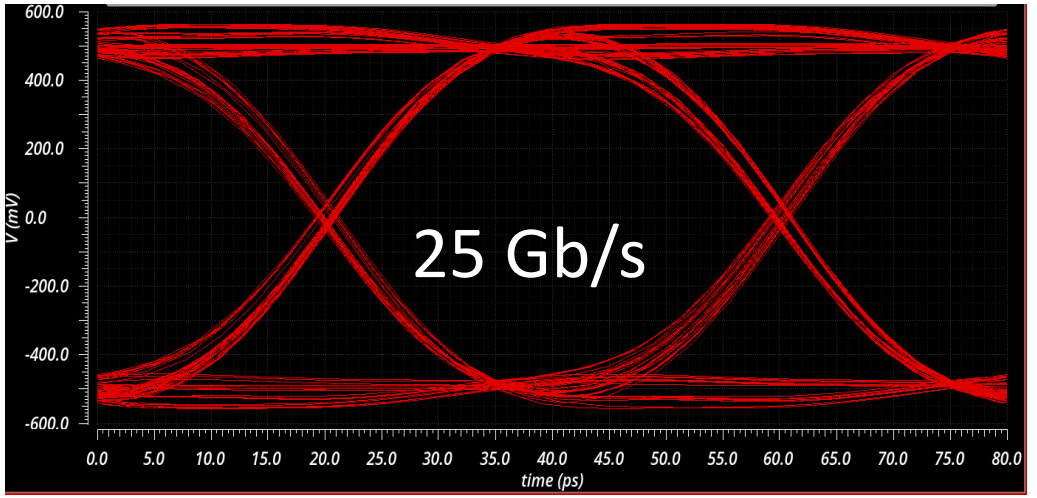
Layout area: 200 x 120 µm^2
Consumption power: 23.85 mW

System simulation with post-layout blocks



Characteristic:

- 50 Ω output resistance
- ±500mV output amplitude
- Passive and active bandwidth enhancement
- Common mode correction

25 GHz LC-tank VCO in 28 nm

Motivations:

- High-speed clock signal for on-chip digital systems (elaboration and transmission)
- Ring oscillators designed in 28 nm showed large PVT variation

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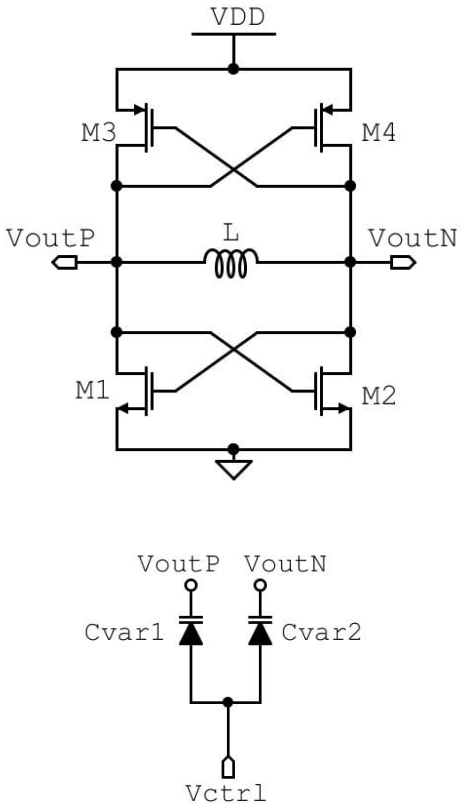
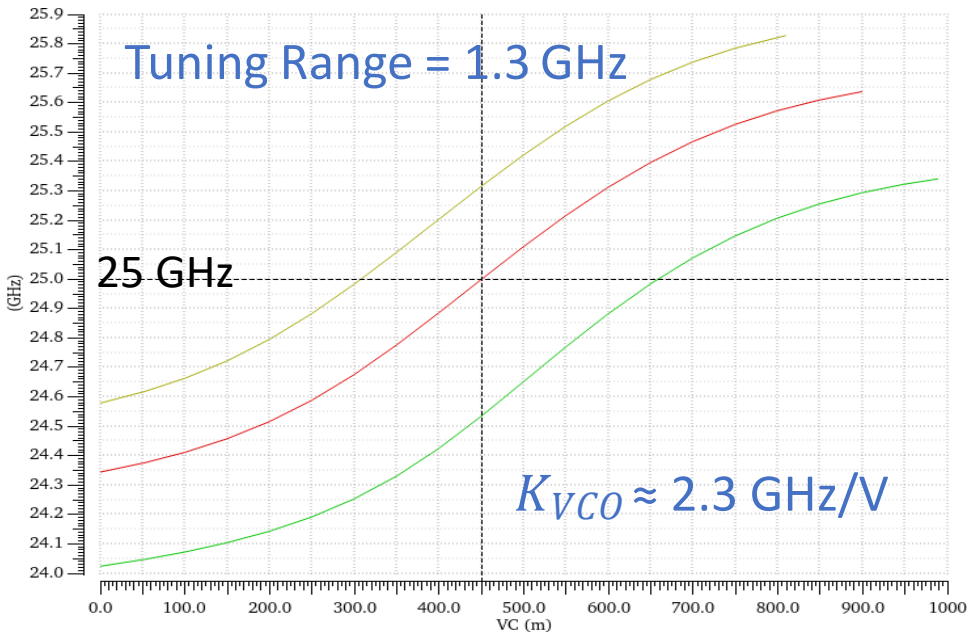
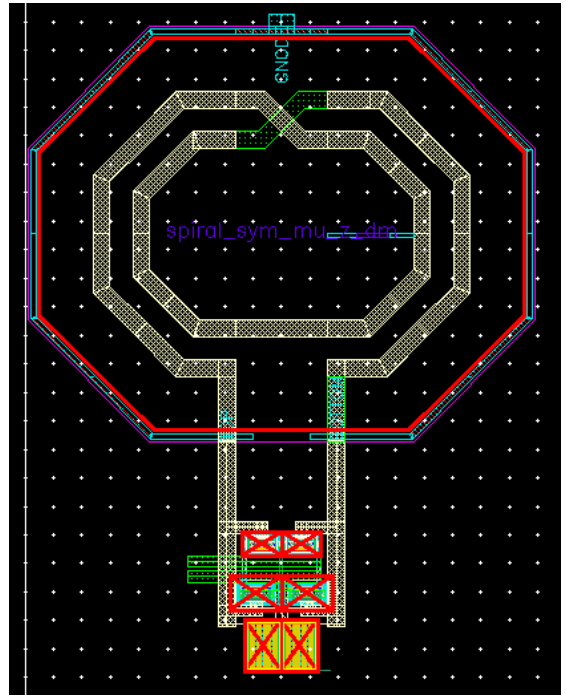




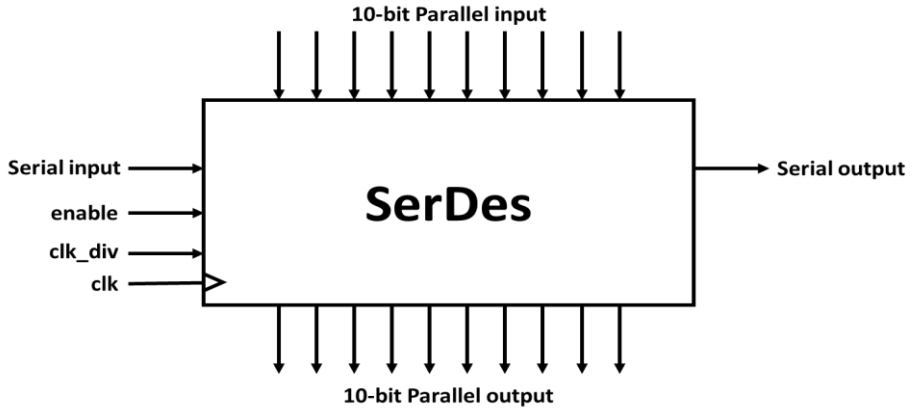


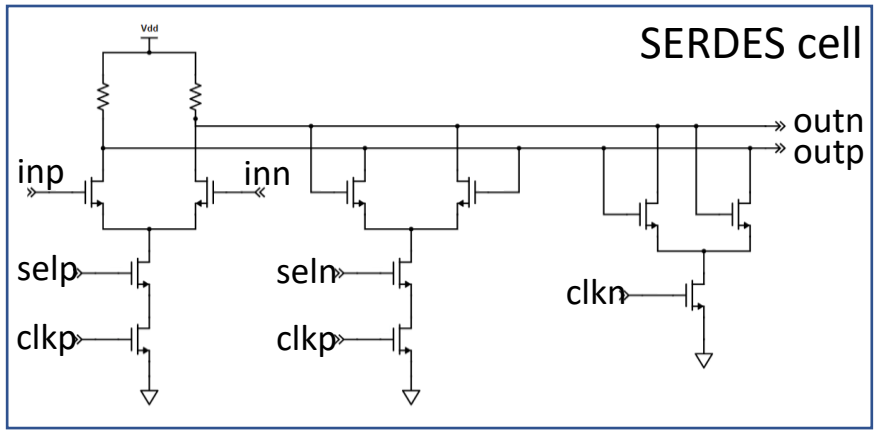
Layout area VCO: 100 x 120 µm^2
Consumption power: 2 mW
Phase noise: -100 dBc/Hz @ 1 MHz

25 Gb/s SERDES in 28 nm (work in progress…)

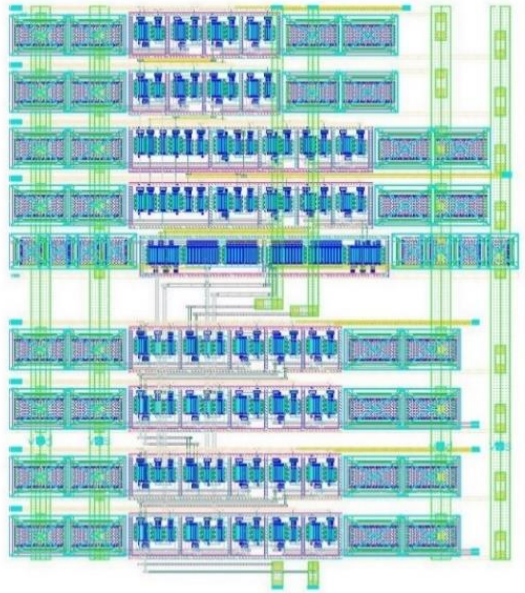
Motivations:

- Parallel to high-speed serial communication conversion and vice versa
- Time Division Multiplexing for area and power reduction
- Custom Current Mode Logic architecture for high-speed





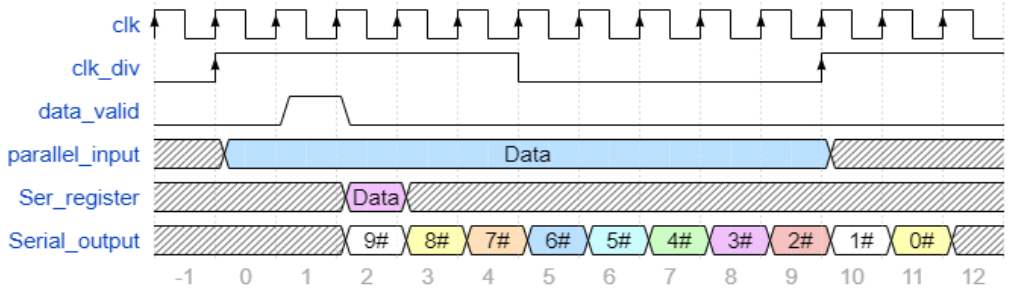
Layout block



Layout area: 60 x 190 µm^2

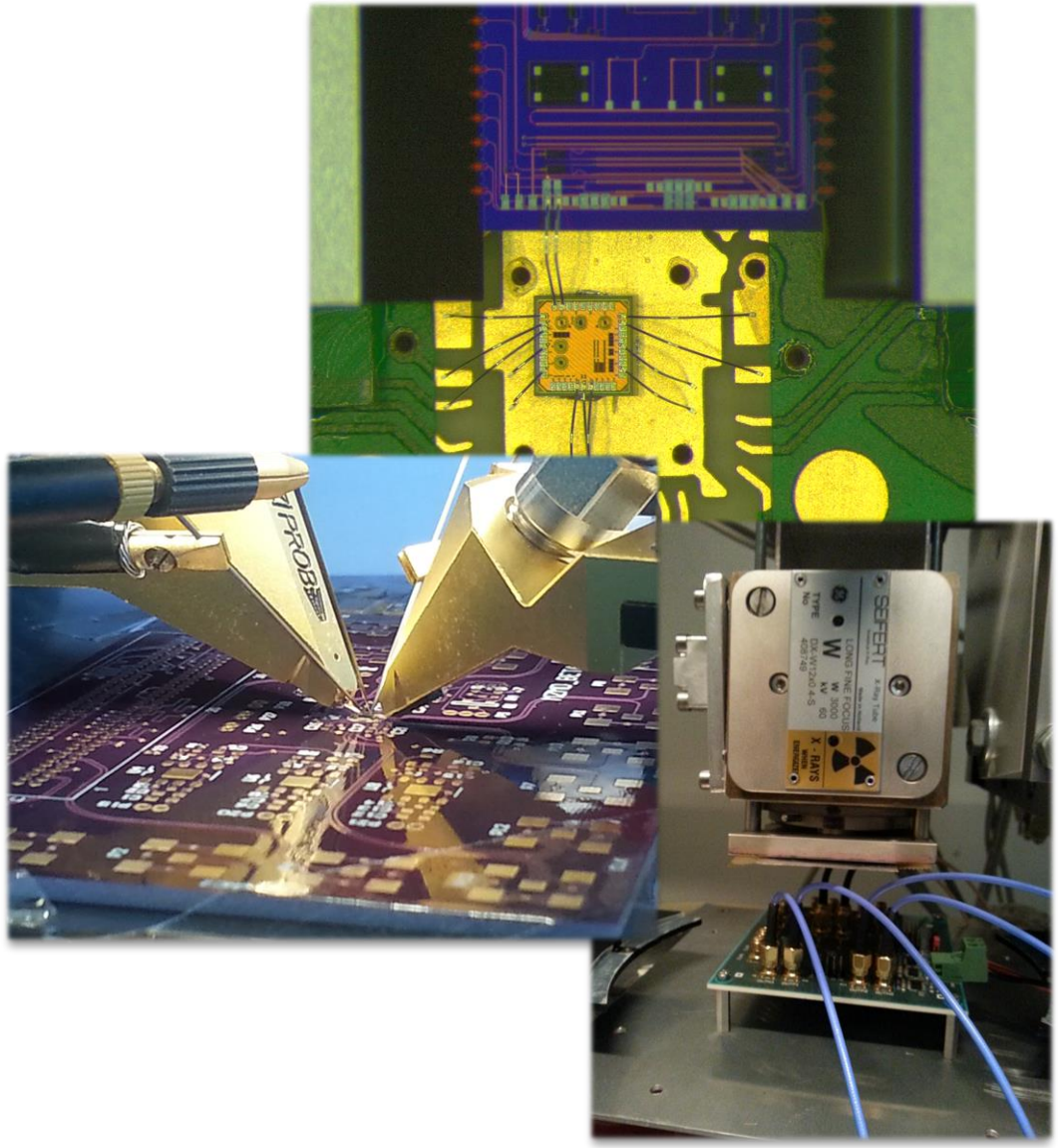
Power consumption: 100 mW

Serialization behaviour



Future steps in 28 nm

- Electrical testing of the submitted 28 nm chip
- Radiation testing of the submitted 28 nm chip
- 25 Gb/s SERDES design conclusion
- 25 GHz Phase Locked Loop design in 28 nm
- 25 Gb/s PIN diodes receiver design in 28 nm
- …



Thanks for your attention