EMPHATIC

Large Acceptance Aerogel RICH Detector

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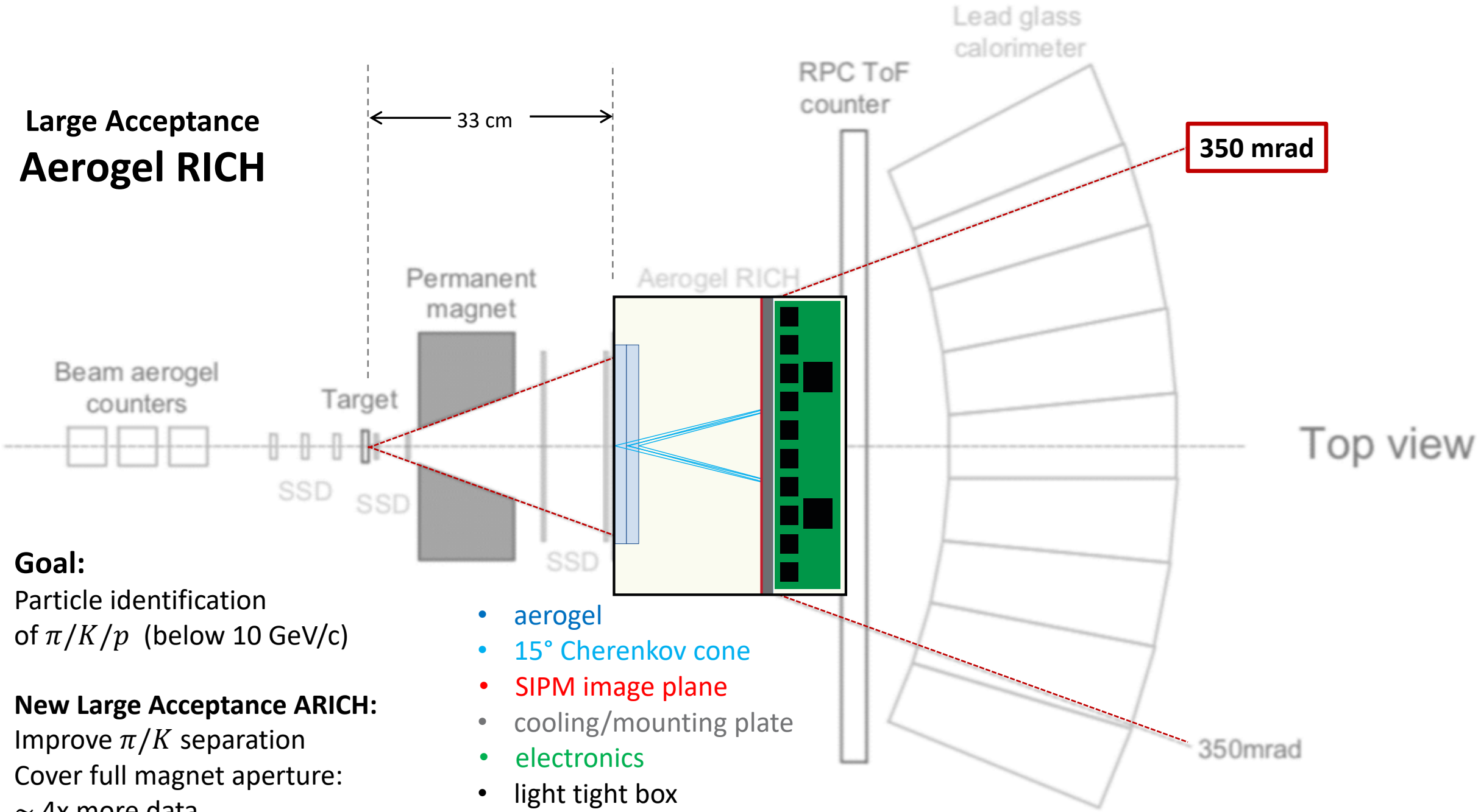
EMPHATIC FWP Review

2021-Jan-22

Aerogel RICH Institutions

Boston • Chiba • FNAL • Regina • Texas • TRIUMF • Winnipeg • York

Large Acceptance
Aerogel RICH



Goal:
Particle identification
of $\pi/K/p$ (below 10 GeV/c)

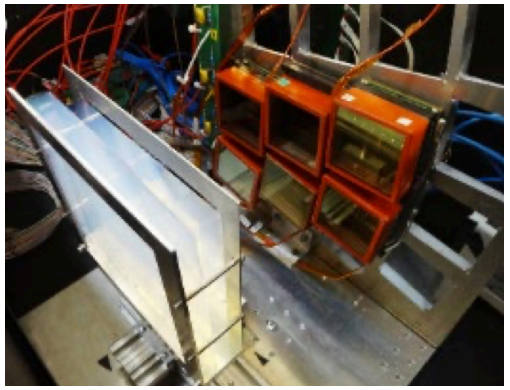
New Large Acceptance ARICH:
Improve π/K separation
Cover full magnet aperture:
$\sim$ 4x more data

- aerogel
- 15° Cherenkov cone
- SIPM image plane
- cooling/mounting plate
- electronics
- light tight box

AEROGEL

- Two aerogel layers
- 15cm x 15cm max (4 panels)
- 2 cm thick each

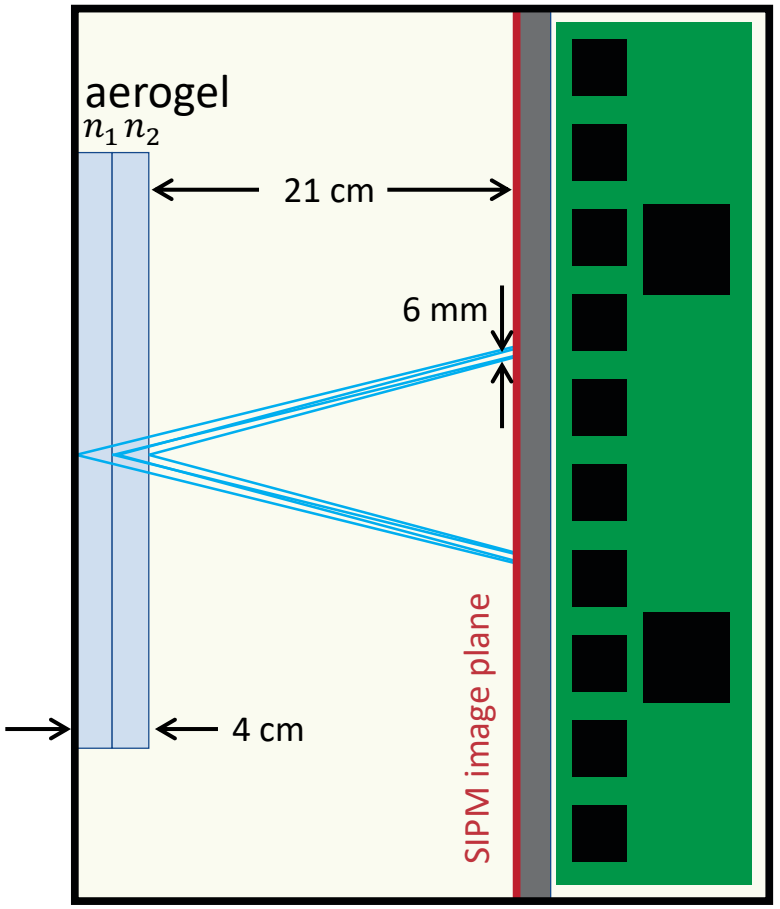
- Proximity focusing
- ~ 6 mm annulus width



- Scattering length 4.6 – 5.6 cm
- Absorption length 200 cm

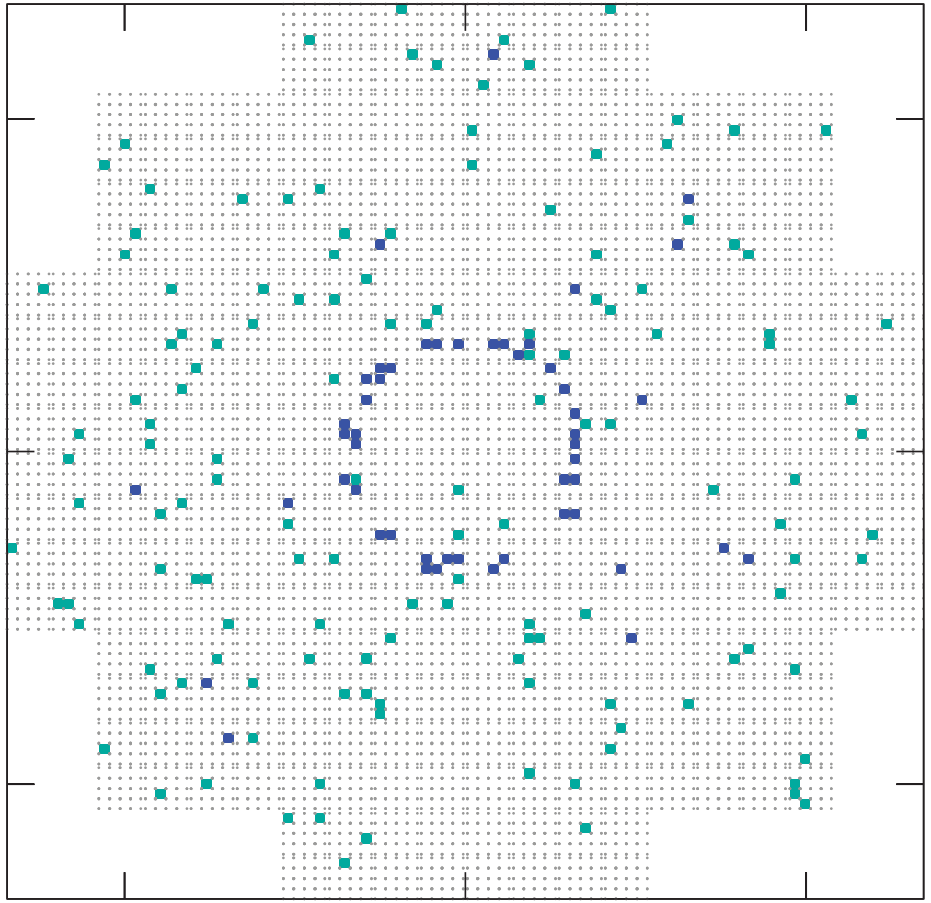
- Developed for Belle II
- Provided by Chiba

Large Acceptance Aerogel RICH



$$n_1 = 1.030$$
$$\theta_C = 13.86°$$

$$n_2 = 1.035$$
$$\theta_C = 14.94°$$

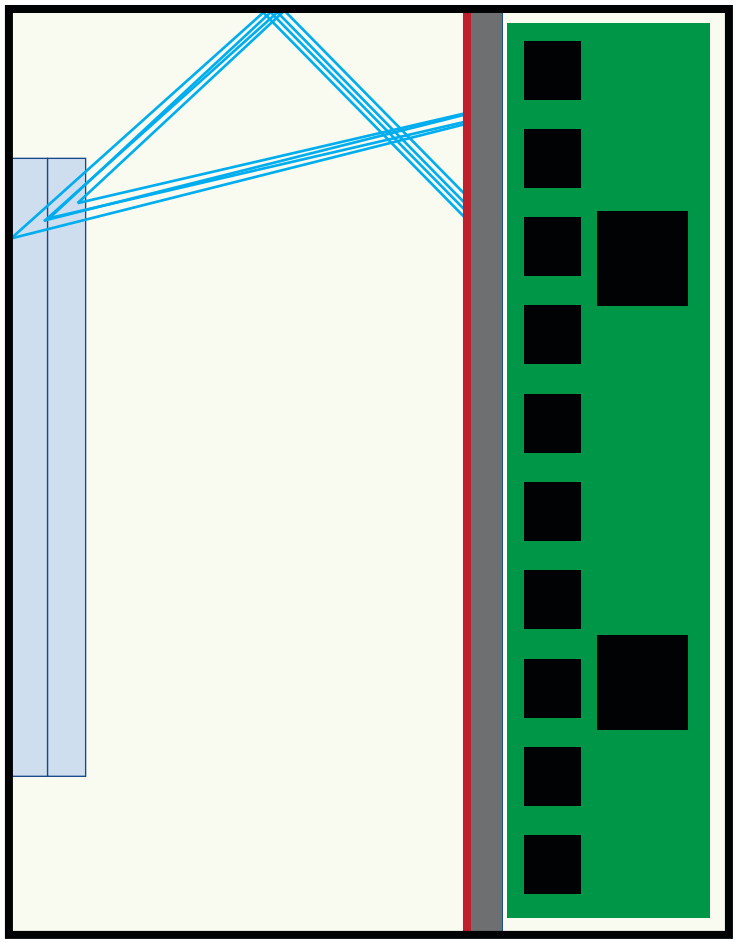


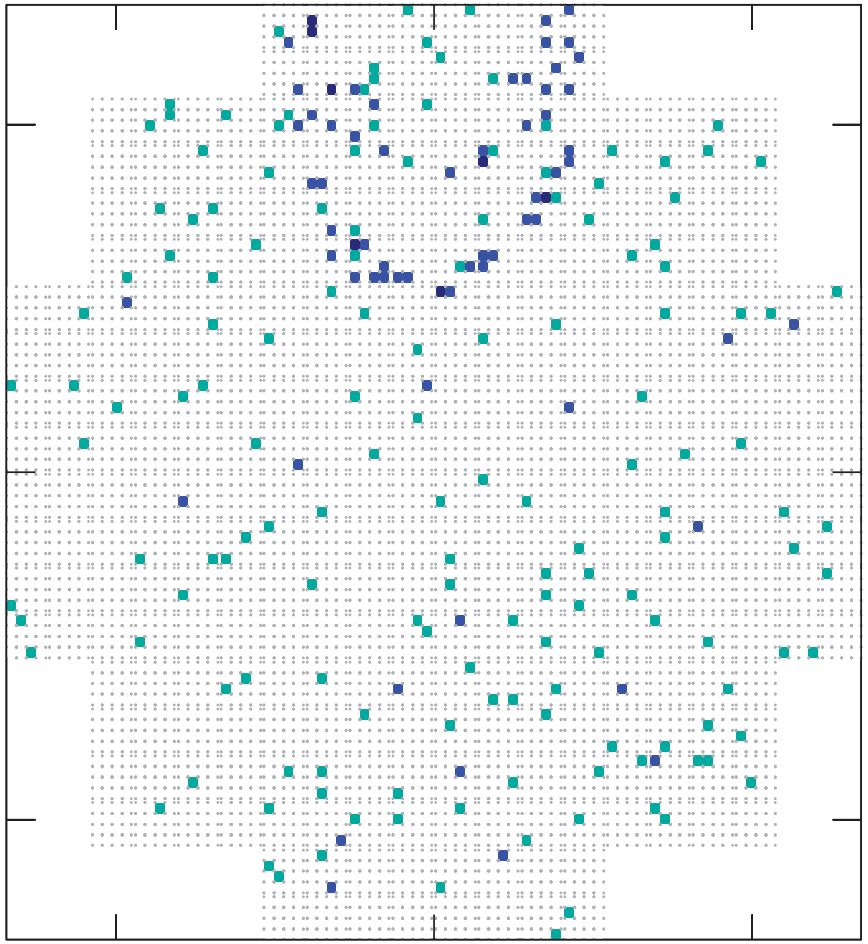
7 GeV/c kaon, 5 ns coincidence, 6.25 MHz dark rate, 20° C

dark hit
Cherenkov hit

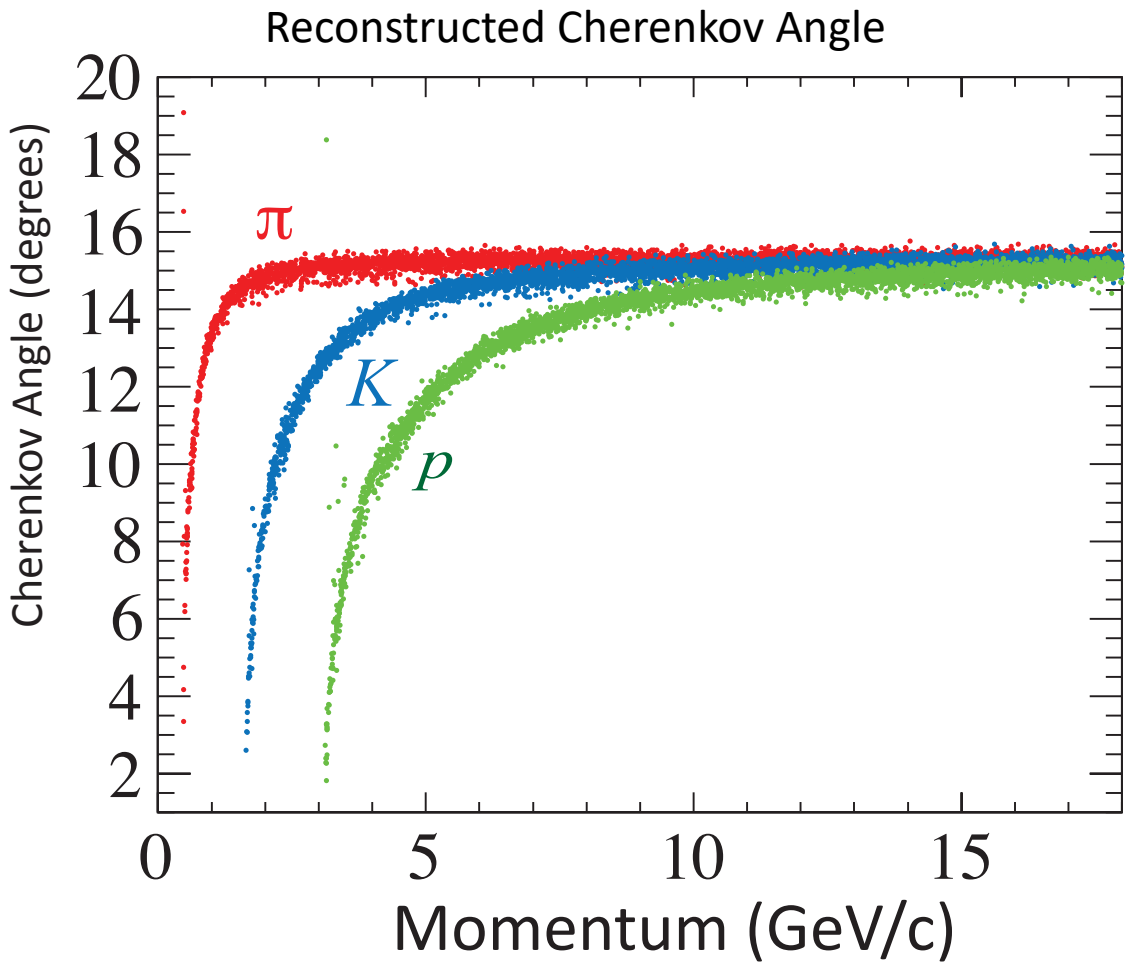
Expect ~60 Cherenkov hits for a single $\beta = 1$ particle

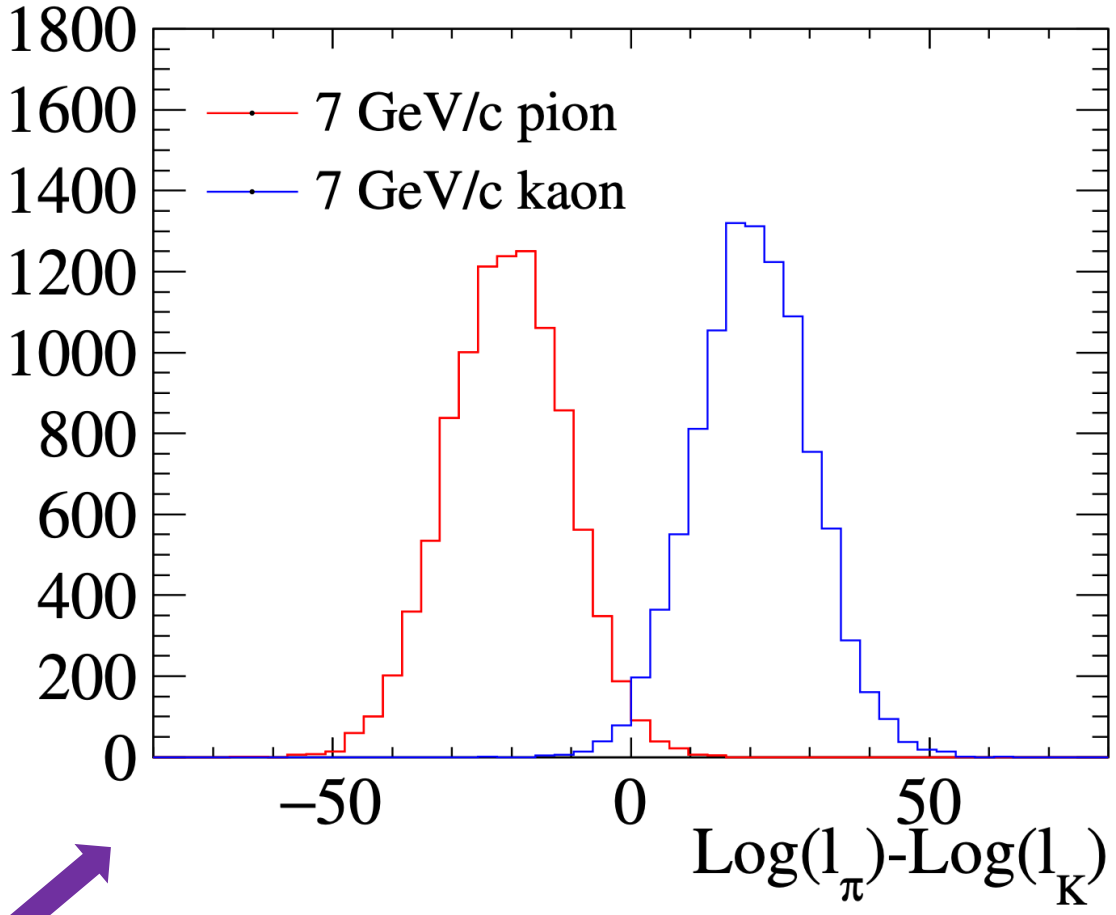
mirror





Possibility of mirrors on sides to increase light collection for large angle events

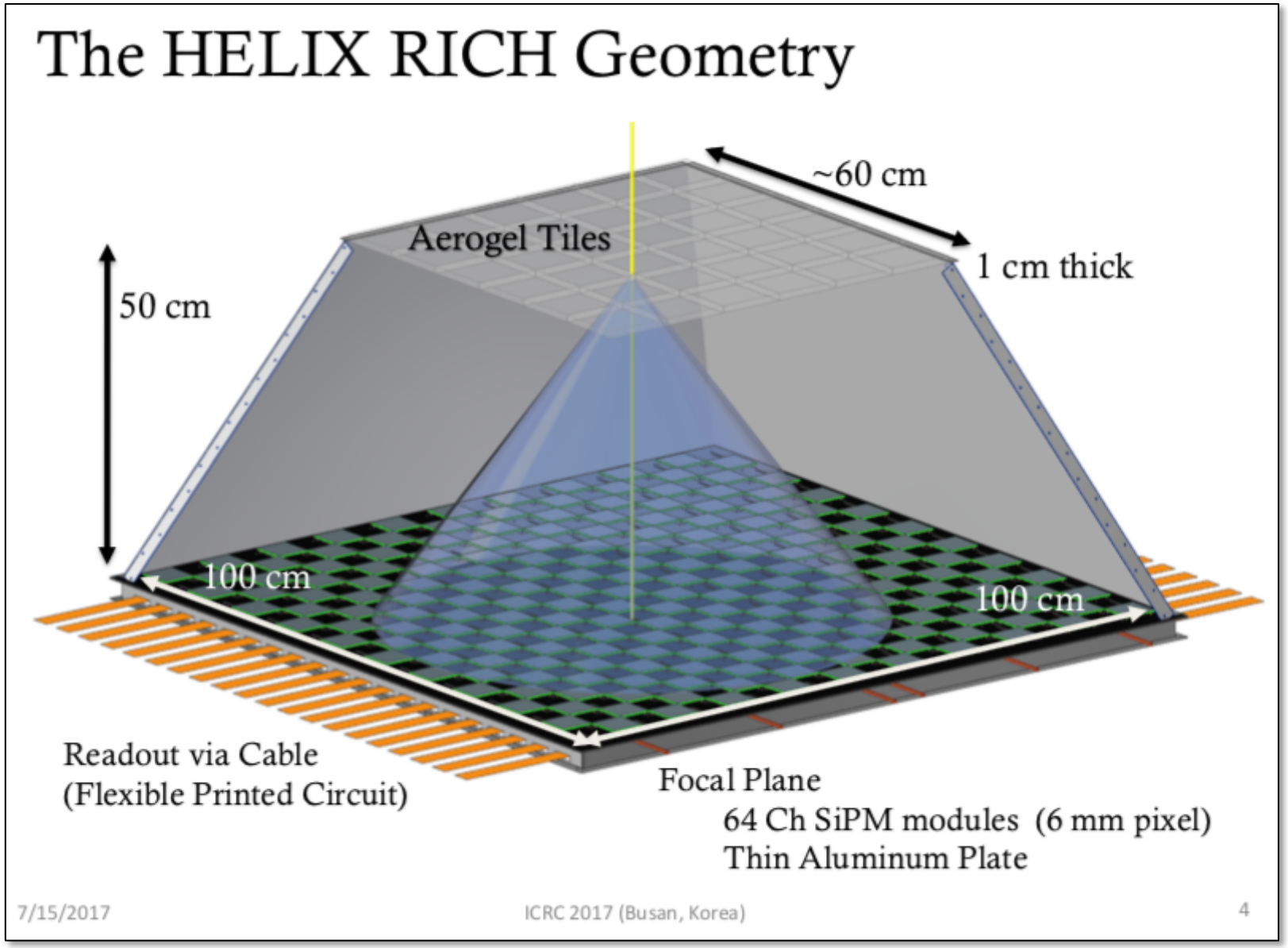




Actual reconstruction is by a likelihood discrimination applied to light pattern for $\pi/K/p$, not by reconstructing the Cherenkov angle. Fitting relies on trajectory determined from upstream tracking.

3σ π/K separation at 7 GeV/c
3σ π/p separation at 13 GeV/c

A similar detector is being developed for the HELIX balloon experiment. We are in contact.

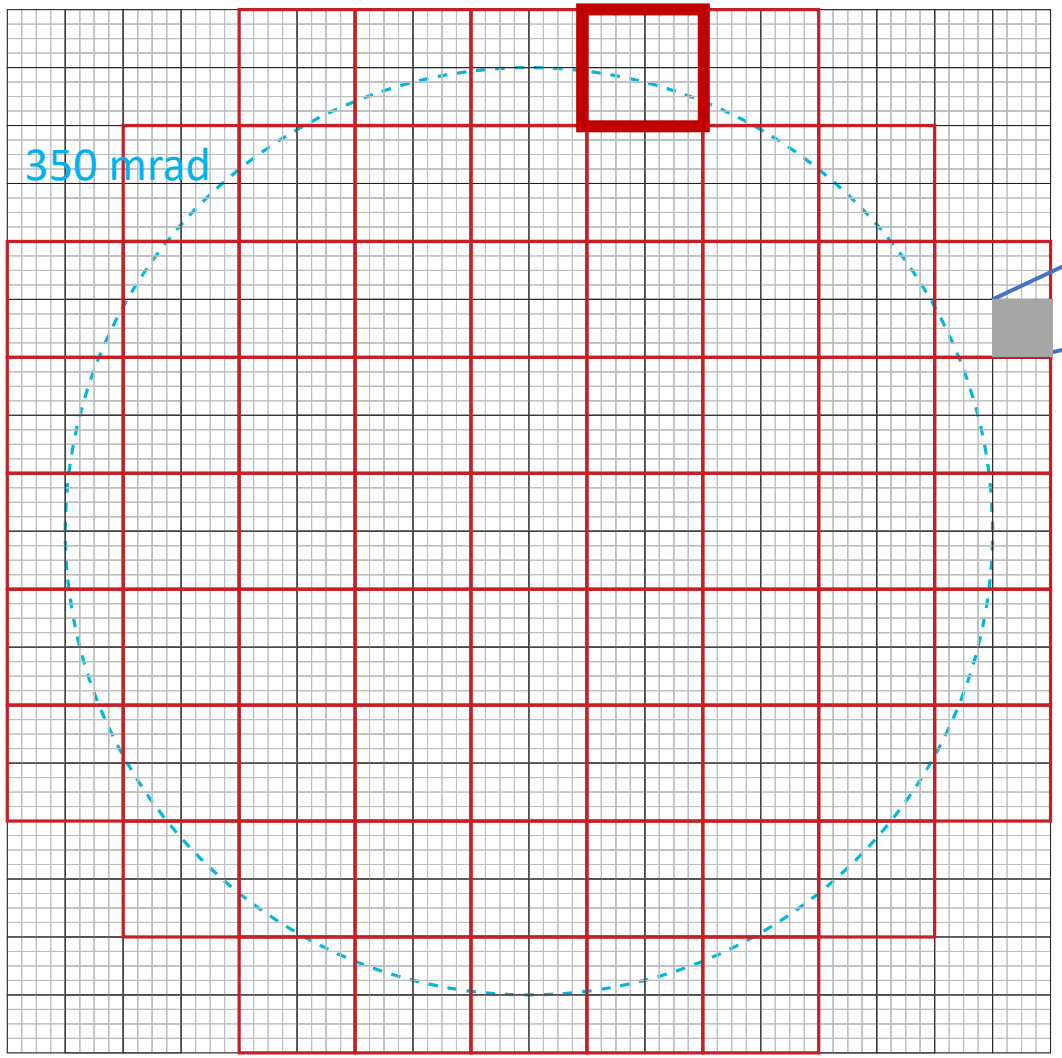


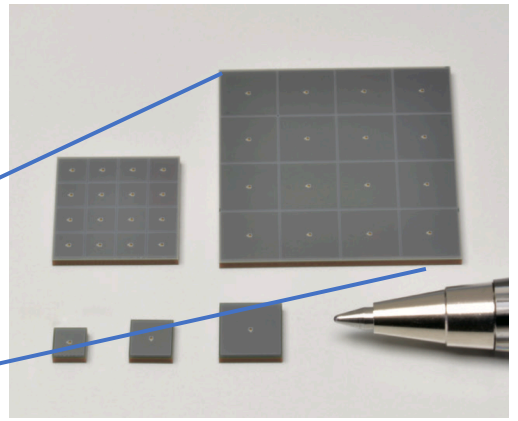
https://www.hamamatsu.com/eu/en/product/type/S14160-6050HS/index.html

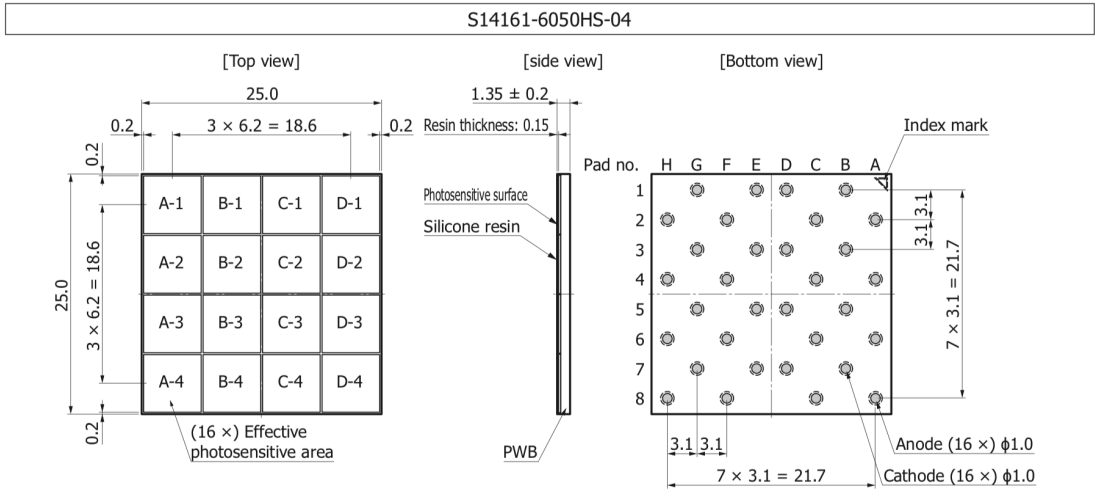
SIPM IMAGE PLANE

9 X 9 LAYOUT

Unit cell: 4 SiPM = 2 CITIROC





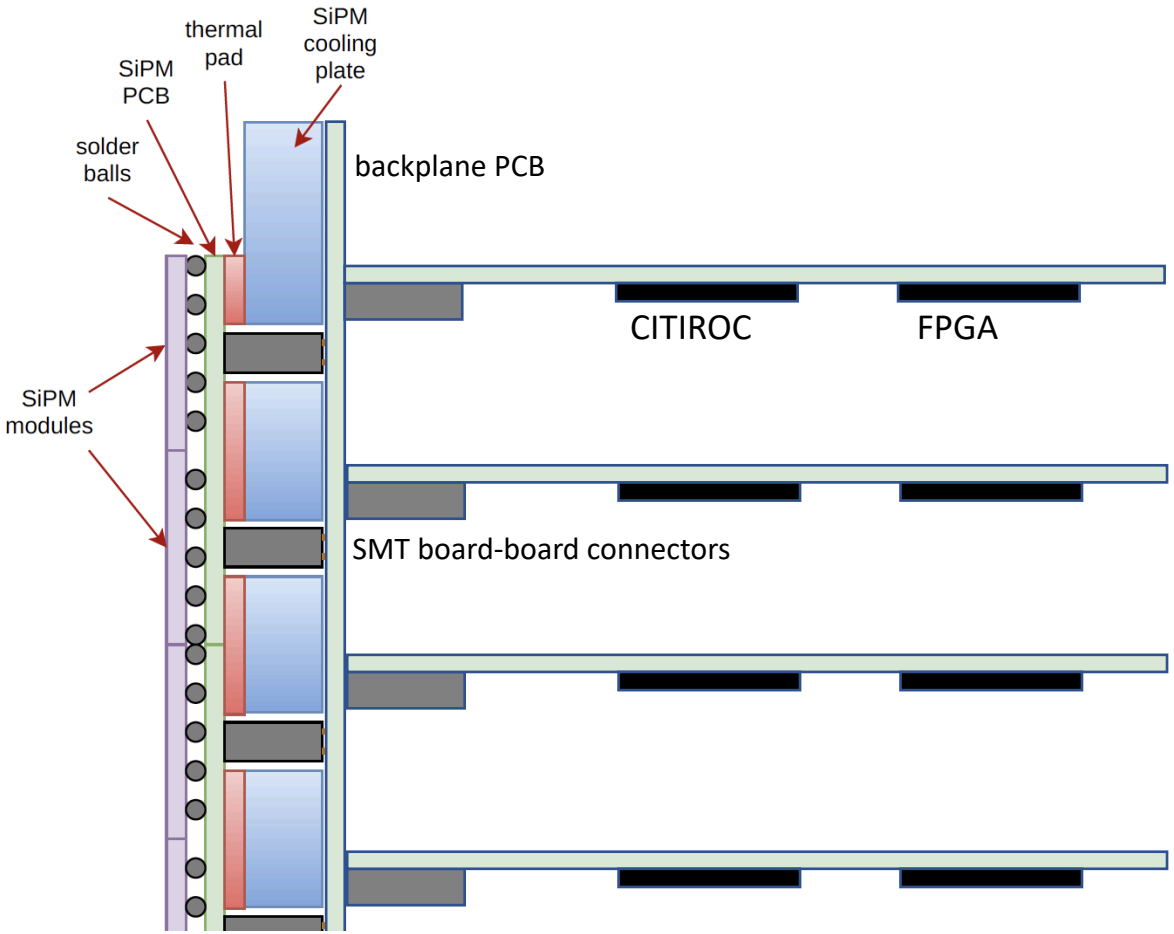


276 - 324 SiPMs required

Some estimates are based on 300 SiPMs, 4800 channels total

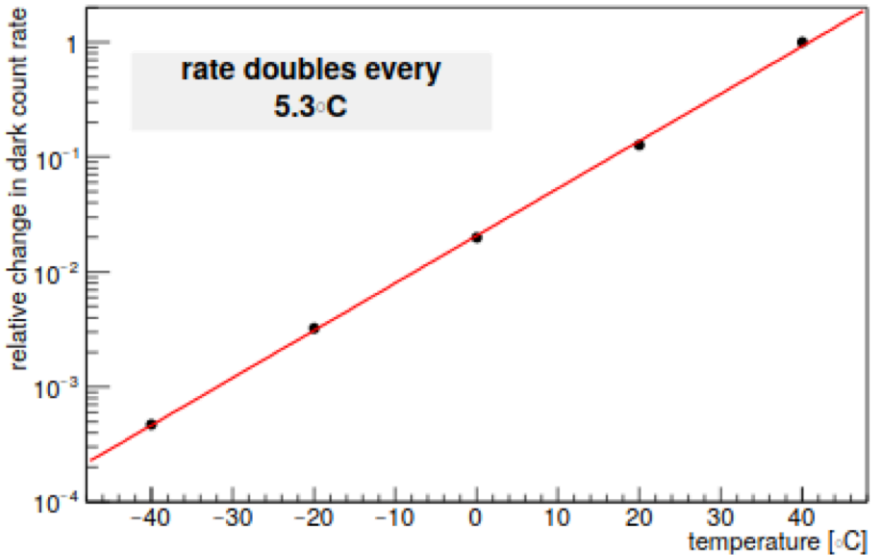
SiPM (Silicon Photomultiplier) also known as MPPC (Multi-Pixel Photon Counter)

COOLING AND MOUNTING PLATE

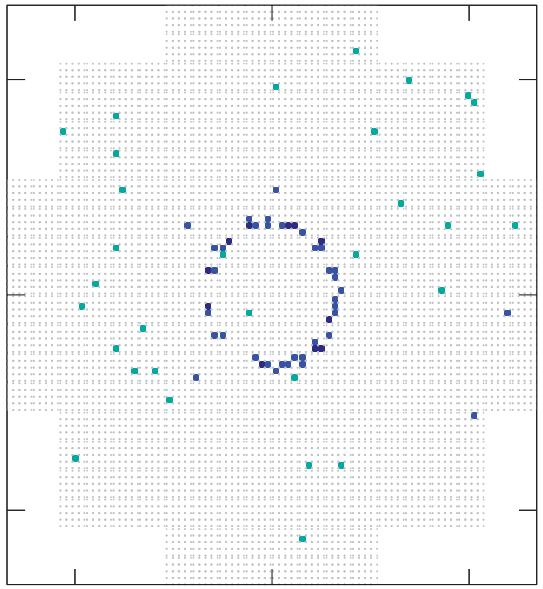


SiPM dissipates negligible power
Can cool plate from edges
Keep other hot electronics (CITIROC, FPGA) separated

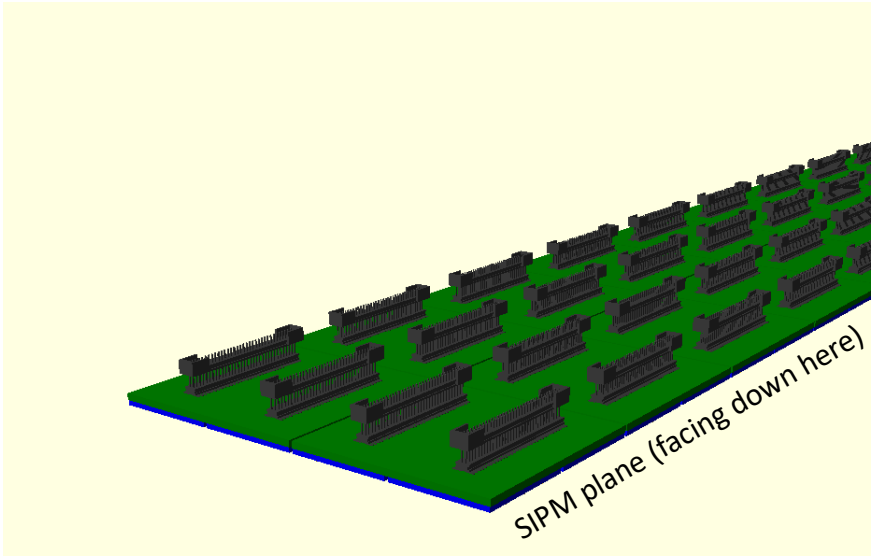
SiPM dark rate strong function of temperature



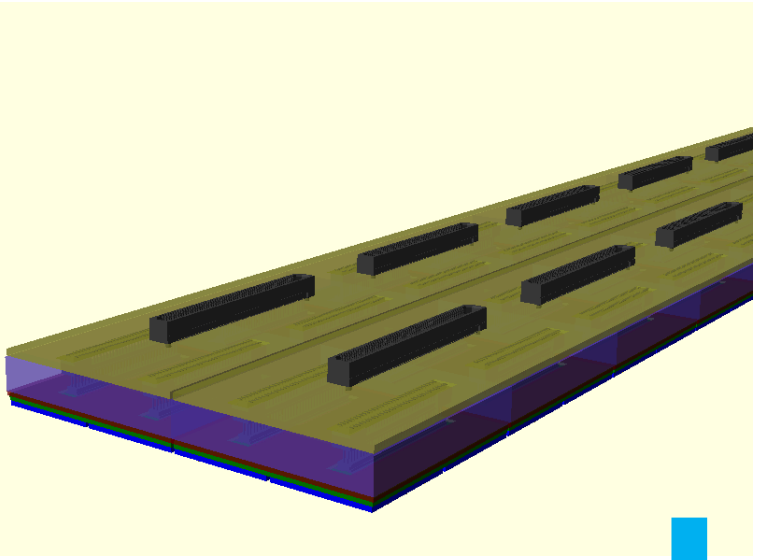
(b) Hamamatsu S13360-3050CS



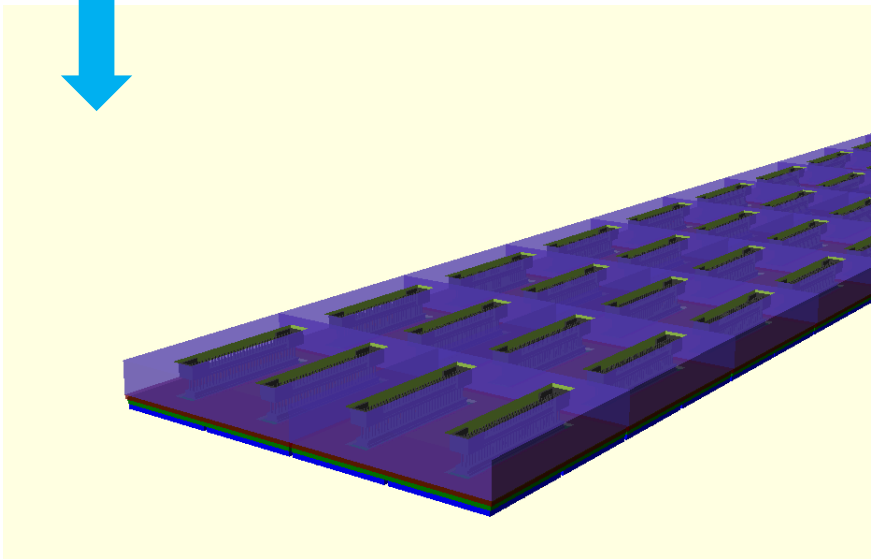
7 GeV/c kaon
5 ns coincidence,
400 kHz dark rate
0° C



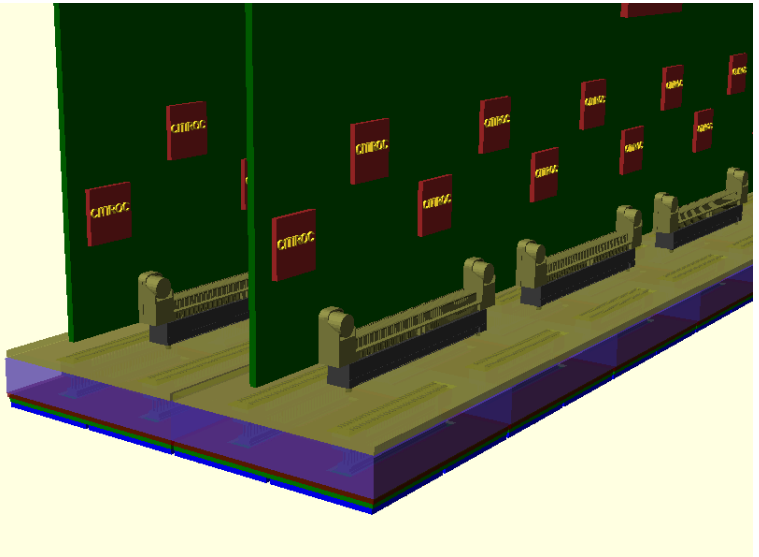
SIPM PCB with SMT connectors on back



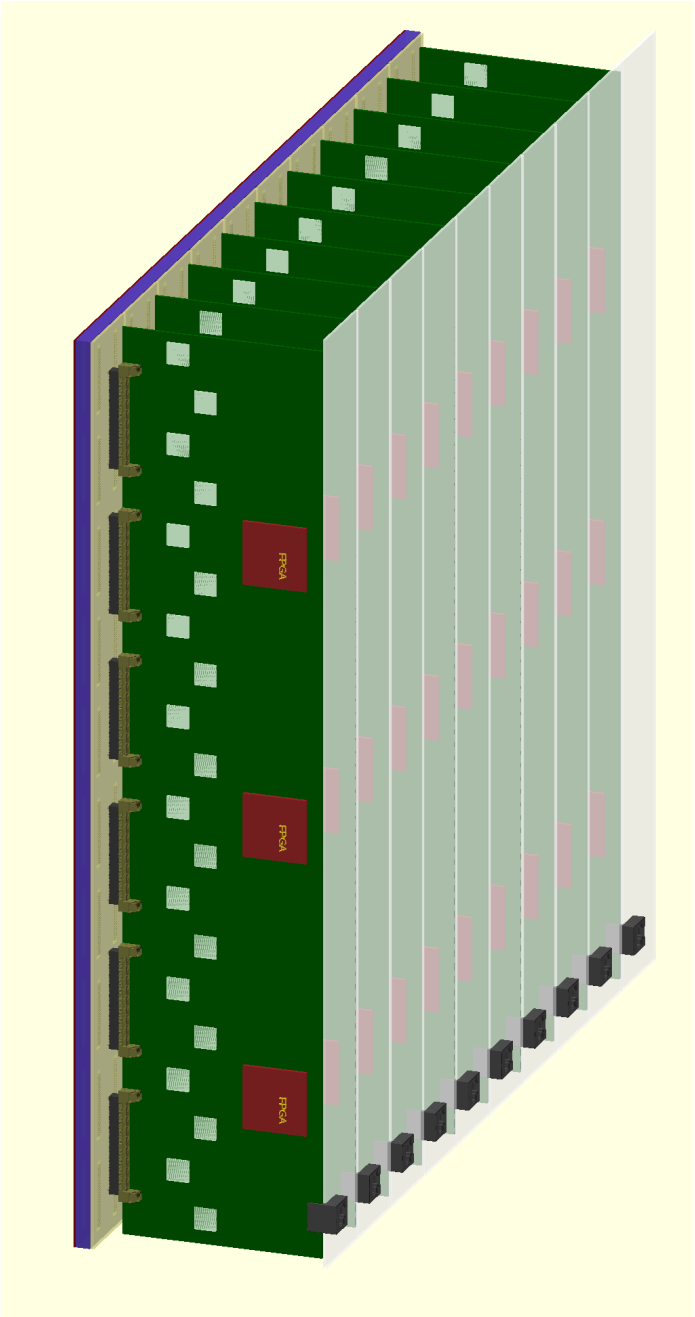
Backplane PCB (will make gas seal)



Aluminum cooling plate, slots for connectors



Readout electronics mounted on backplane

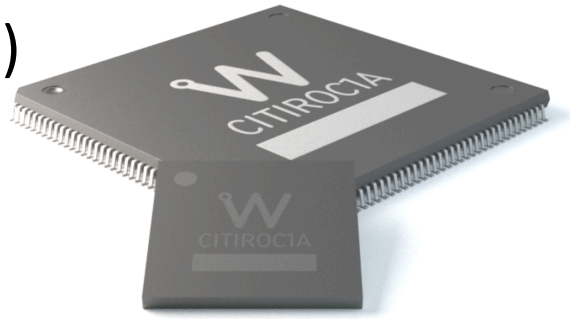


- Top and bottom box sides should have card guides for readout boards
- Cooling plate should be square and extend to edges
- Backplane PCB should be screwed to cooling plate
- Backplane PCB could be split in the middle to save manufacturing cost
- Concept of using “backplane” as gas seal proven in g-2 tracker

ELECTRONICS

Front-end for readout: **CITIROC** (aka WEEROC, distributed by CAEN)

https://www.weeroc.com/products/sipm-read-out/citiroc-1a

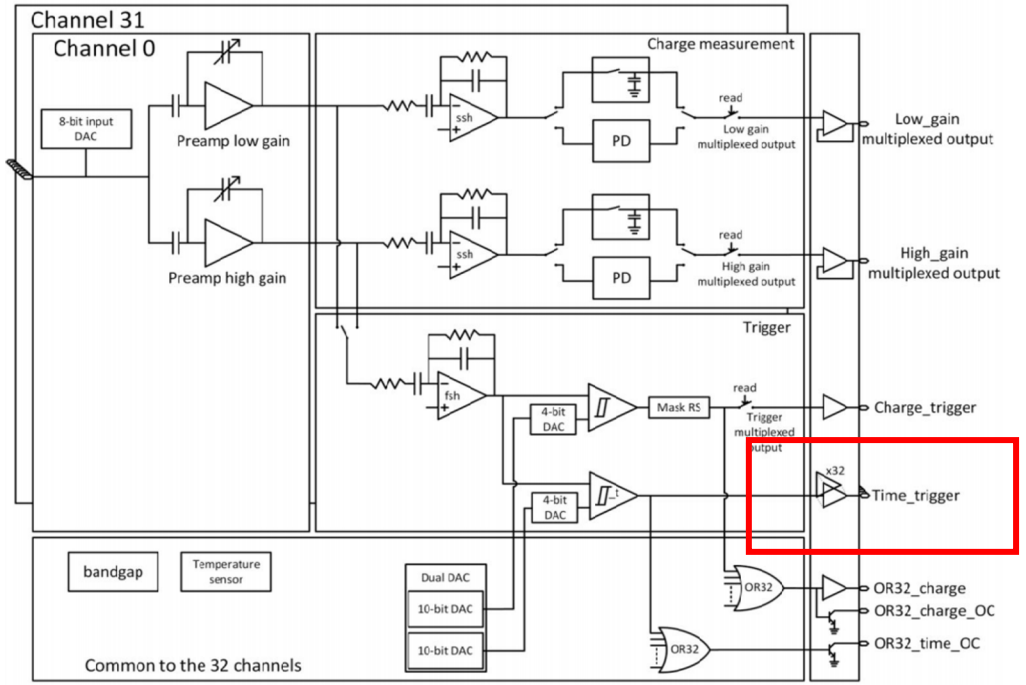


Citiroc 1A allows triggering down to 1/3 pe and provides the charge measurement with a good noise rejection.
Not planning on charge measurement at this time

Moreover, Citiroc 1A outputs the 32-channel triggers with a high resolution timing (better than 100 ps).

An adjustment of the SiPM high-voltage is possible using a channel-by-channel DAC connected to the ASIC inputs.

A7585/DU 85V power supply (candidate)



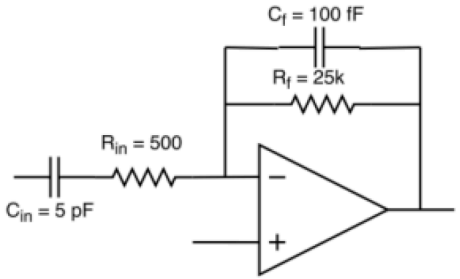
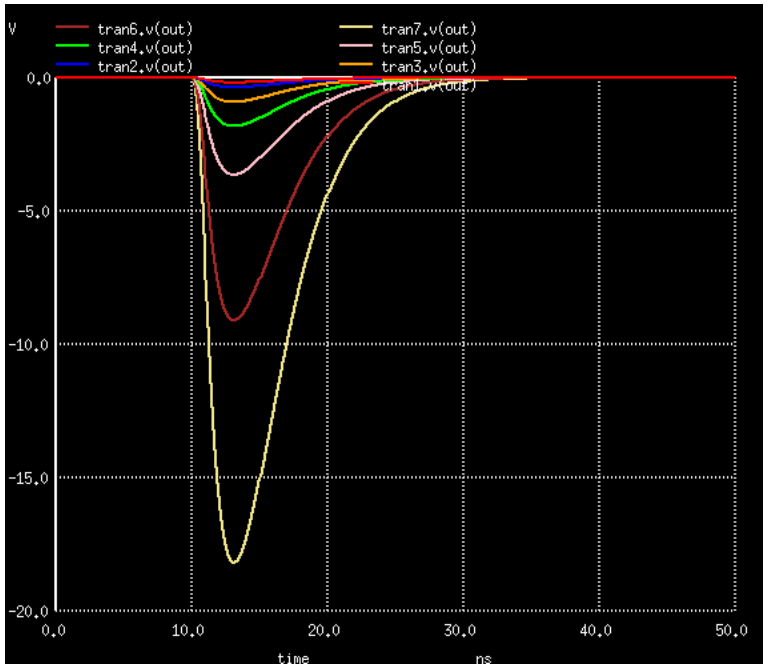


Figure 3 - Fast shaper block scheme

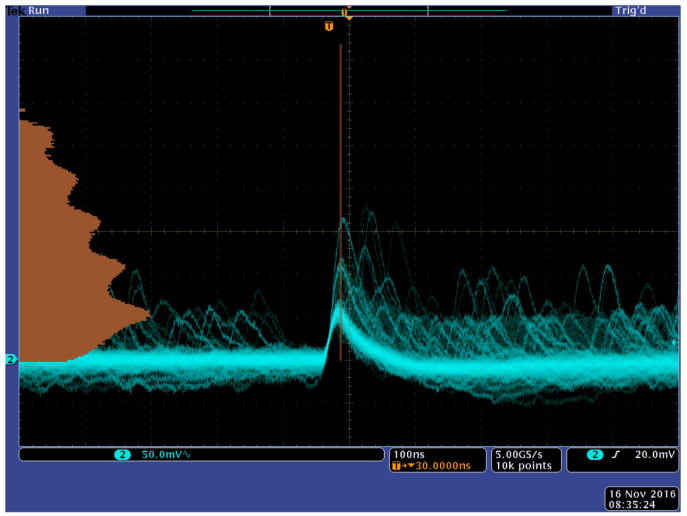
CITIROC shaping circuit (simulation)



Use fast timing to mitigate high dark rate (6.5 MHz at 20°C)

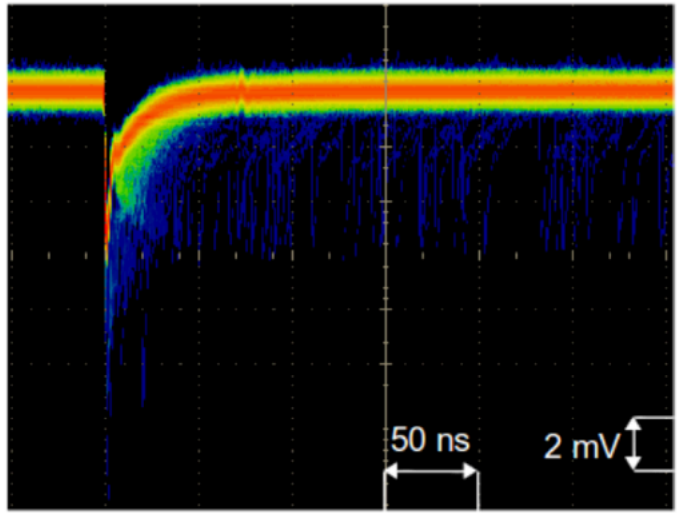
Current simulation assumptions (conservative):
20 ns deadtime (50 MHz spec for CITIROC)
5 ns timing accuracy/precision to reject dark hits

Looking forward to measurements with prototype

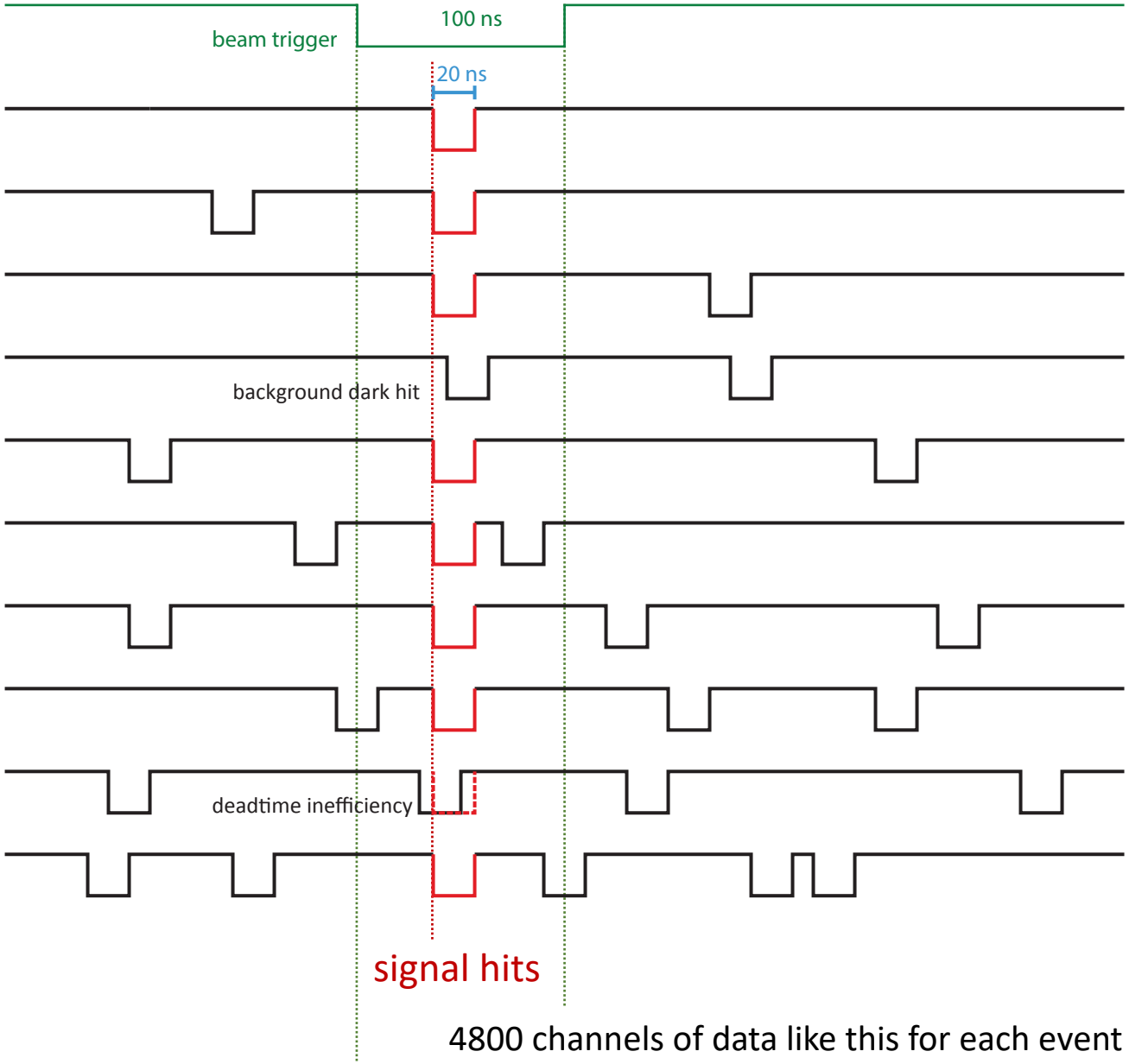


HELIX, ICRC 2017

S13081-050CS



https://arxiv.org/pdf/1703.06193.pdf



4800 channels of data like this for each event

5 MHz dark rate (nominal), 0.5 dark hits/100ns
Dark hit multiplicities shown are representative

Stated maximum rate for CITIROC is 50 MHz (20 ns)
Assume every hit datum is 20 ns

Event size:
2400 dark hits
$\sim$ 200 signal hits (2-3 particles)

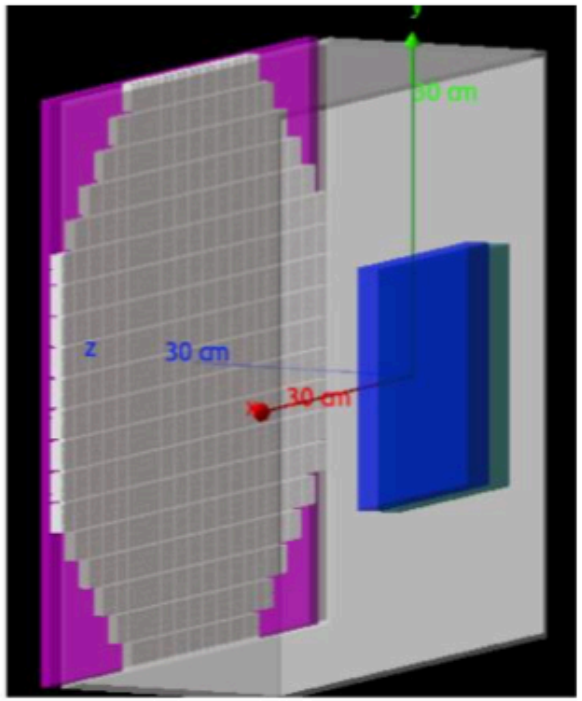
Background dark hits rejected by precise timing
(assume $\Delta T > 5$ ns rejects dark hit, for now)

Signal loss from preceding dark hit: $\sim$10% probability

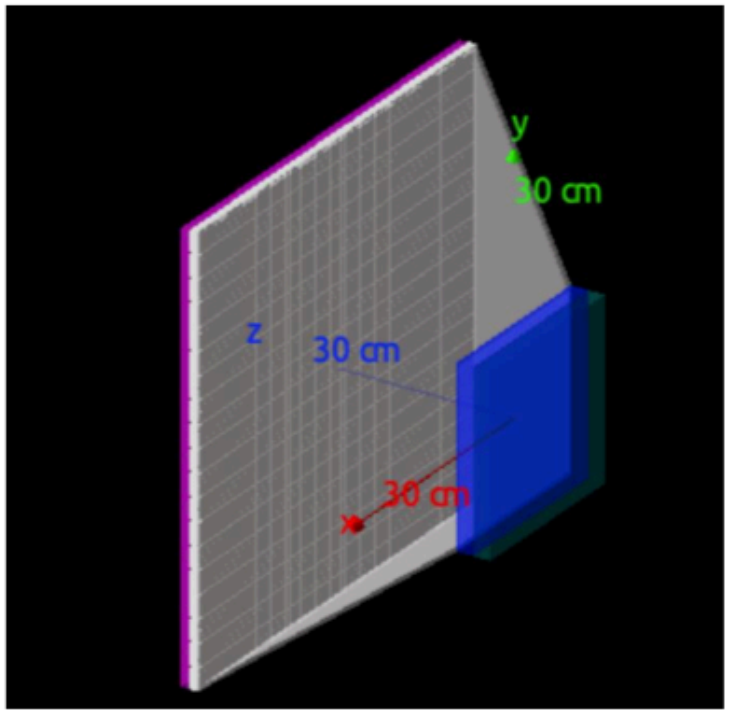
Assume 12 bits/edge, 0.5 hits/channel, minimal overhead
~ 8 kB/event

Top data rate: 30 kHz x 4 s, 10 μs between events
120K evts/spill (one spill each minute)
960 MB/spill (mostly dark hits)
for 10 cards, $\sim$ 1.6 MB/s/card data transfer rate
$\sim$ 1.4 TB/day data to keep

LIGHT TIGHT BOX

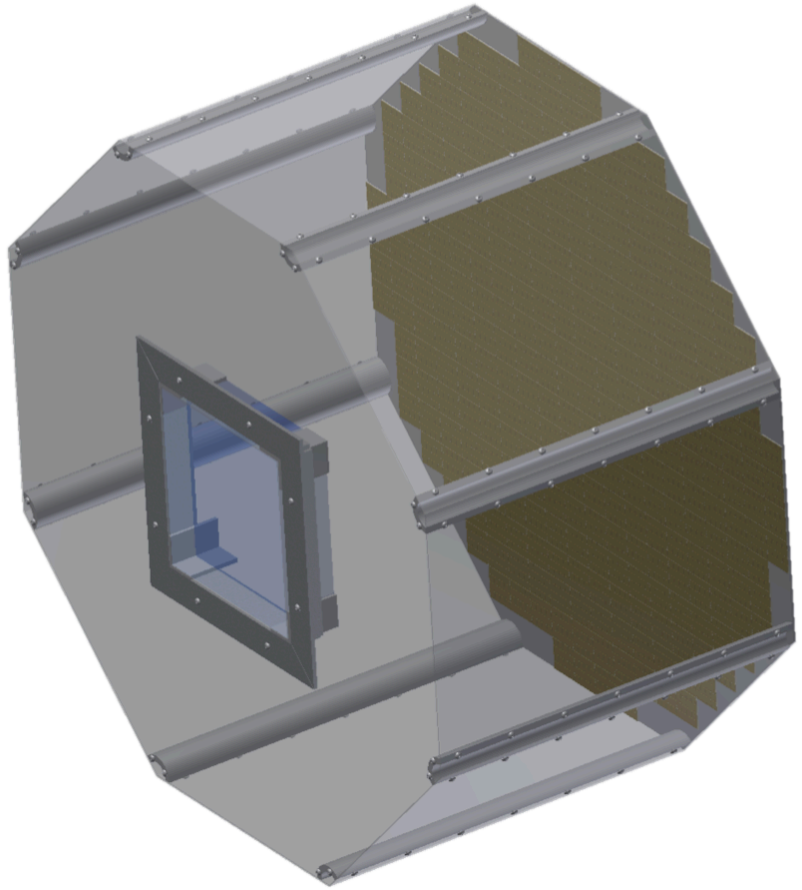


Rectilinear box is simplest
and current preference



Increase reflected light
if mirrors are used.

Shape adopted by HELIX.



Reflection in corners improved
More azimuthally symmetric/uniform.

Rear box would still be rectilinear
for electronics cards.

Plan for gas tight front volume for potential RICH upgrade

SCHEDULE

Design, procurement underway for small prototype:

64 channels:

- Four SIPM (one 2x2 unit cell)
- Four CITIROC (build 1 extra readout card for studies)
- One FPGA (not selected yet)
- Benchtop power (but one A7585 to get experience with)

Schedule: (see project document for finer detail)

February – May 2021: Prototype work
June – September 2021: Preproduction, procurement
October – December 2021: Production
Ambitious goal: Pack and ship before holiday shutdown of university efforts
Early 2022 – Commission
Late spring, early summer 2022 – Operate in Phase 2

COST

Item	Description	Quantity	Unit cost	Total Cost
SiPM module	2x2 SiPM array on PCB with connectors	81 + 4 spare	$1245 + $200 NRE	$106K
Backplane Module	PCB with connectors	2	$2930 + $500 NRE	$6.4K
Readout Module	PCB with 18 CITIROC and FPGAs for 9 SIPM modules	10 + 2 spare	$8711 + $1120 NRE	$105K
Bias Voltage	Not yet designed			
				$218K
		Developing bottoms up estimate for electronics M&S		
Design and cost estimation of cooling plate, light tight box, and electronics frame is under development but should not drive overall schedule for ARICH.				