Announcements & Electronics

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Announcements I: IPR

- I spent the last week in the DOE Independent Project Review (missing much of the ND-GAr workshop, which made me sad)
  - You heard Stefan's summary Friday
  - In my view, TMS did well.
    - Biggest identified problem was a double-counting of effort at installation time. A good catch. (That's why we have reviews)
    - Asked us to simulate performance at 2.4 MW (see next slide)
  - Committee showed substantial interest in ND-GAr, which is not part of the project
  - I gave the committee several opportunities to comment on certain cost-saving aspects (no spares, no LED flashers, etc.). The did not.
  - There was a non-TMS-specific comment about "optimism bias" – **I am taking this seriously**
  - We expect to be in "constant review" mode for at least the next ~18 months
    - As Stefan says, we haven't worked all this out, but if you just write down what needs to happen, that's how long it takes

The Issue at 2.4 MW

- Pileup is qualititatively different at 1.2 MW and 2.4 MW
- At 1.2 MW
  - We have one or sometimes two muon candidates in ND-LAr (light timing tells us that)
  - …pointing to one or sometimes two muon candidates in TMS
- At 2.4 MW
  - We have maybe 3 or 4muon candidates in ND-LAr …
  - …pointing at maybe three muon candidates in TMS
  - Many-to-many match
- The stereo design has relatively weak pattern recognition
- On the other hand, we have some advantages – e.g. typically the second muon is far away, especially in z (the LAr muons are in the front but the iron is in the back)
- We need to simulate to really understand this
  - Ideally, the simulation includes energy “blobs” (NCs, Michels, etc.) as well as tracks

Announcements II

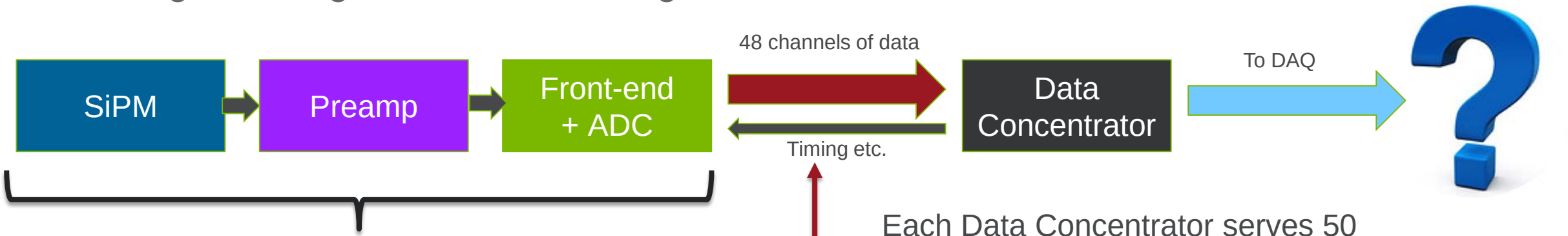
- Long-term, this project will have Five Level 3 managers
  - Steel, infrastructure and magnets
  - Electronics
  - Site assembly at each of the three sites

- Today, our goal is to *get to* the point where we are building panels
  - Mat Muether and Hugh Gallagher have graciously agreed to be Level 3s today as we work towards this goal
  - Exact responsibilities will evolve over time with the project status

- If this were an in-person meeting, I would have brought donuts

Electronics Changes

- Our original design looked something like this



Together form the “On Panel Board” (OPB)
There are 400 of them, each serving 3 SiPMs (i.e. 48 channels)

Each Data Concentrator serves 50 OPBs. It’s probably FPGA-based and it’s job is to mate this to the DAQ.

The DAQ is even less defined than what we are discussing today.

This data run is a few (2-3) meters

Electronics – Back From The Engineers

- As reported last week, I spent one week of engineering on this, to get a Bill-Of-Materials level estimate. I asked them not to redesign, but let us know if anything was stupid

- The FPGA plan fell into that category
  - The Data Concentrator FPGAs needed to be big to handle all the inputs
  - But there wasn't much work for them to do, so a lot of the chip was unused → uneconomical

- The new concept is to split this into two parts
  - A Xilinx Altrix-7 FPGA on the Panel
    - Does zero suppression on the Panel
    - Panel communications are serial over DisplayPort rather than parallel
  - A Xilinx Zynq-7 FPGA on the Data Concentrator
    - FPGA with a built in ARM Cortex-A9 CPU
      - This chip is powerful enough to run Linux

Electronics – Back From The Engineers Part II

- Not everyone was enthusiastic about the AFE5807 front-end chip, but everyone thought it would work
  - Single-ended input with no common mode rejection – potential for noise
  - We should keep this in mind when the time comes
  - Also, when the time comes there will likely be a version that can run at 106 MHz (Main Injector frequency is 53 MHz)

- The estimate was not clear about what goes on which boards, but it appears that the low voltage is generated at the DCs and sent to the OPBs. The DisplayPort cable can't handle all these volatges
  - A separate cable is needed, probably with DIN or DSUB connectors (never use the same connector twice on the same unit!)

DIN

D-SUB

These are in the dollar to few dollar range. Both are commodities – can easily get from Newark, Mouser, etc.

Electronics – Back From The Engineers Part III

- They included a custom optical link to the DAQ
  - This is unnecessary, because the system is powered by Power-Over-Ethernet. One port is our uplink to the DAQ.
    - Reminder – the “DAQ” doesn’t do any actual data acquisition. We do. The DAQ does event building and writing to permanent storage.

- The Data Concentrator boards are now Data Concentrator crates (or 19” racks, if we can swing it)
  - 8 crates, 10 boards per crate, 5 panels (240 channels) per board
  - The “5” is just a guess

- The largest and most uncertain element was PCB manufacture and stuffing: $400,000
  - As we go forward, we should keep the boards modest and standard-sized