ASIC Design and Development

Paul Rubinov

2021 All Engineers Retreat

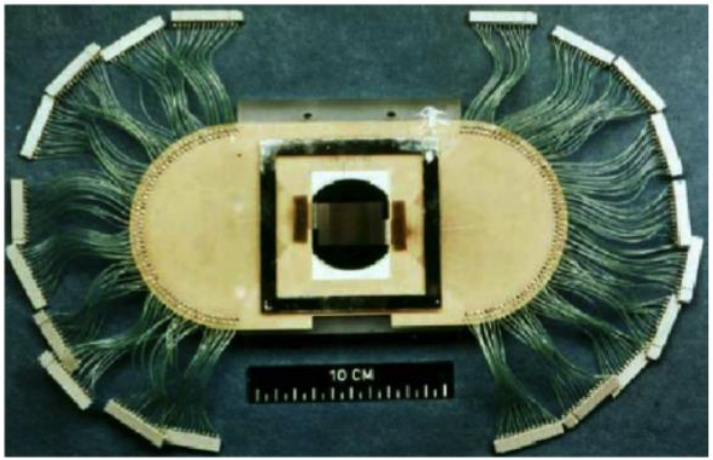
24 Feb

ASIC
Fermilab

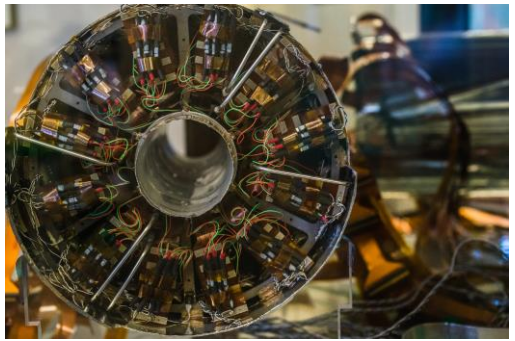
The Fermilab ASIC Group

Application **S**pecific **I**ntegrated **C**ircuits

The history of ASIC design for HEP is tied to the development of Si strip detectors.
The first Fermilab ASIC : QPA02 (Quad Preamp), bipolar, semi-custom



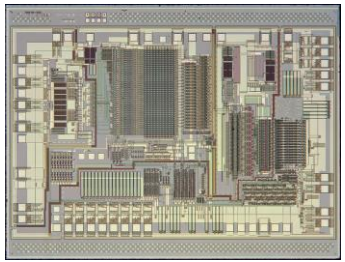
First Si strip detector at CERN
NA11 (1981)
60um readout pitch, 400 chan
Readout > 1 sq meter



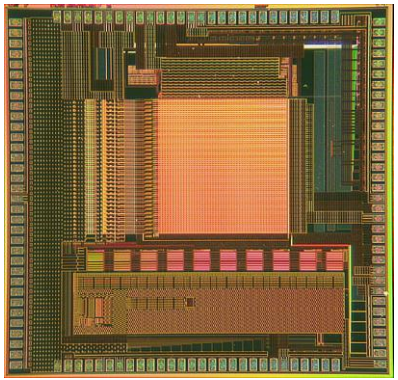
R. Yarema, "ASIC Design at Fermilab", FERMILAB-Conf-91/170

Need for collider detectors drives full custom design in CMOS

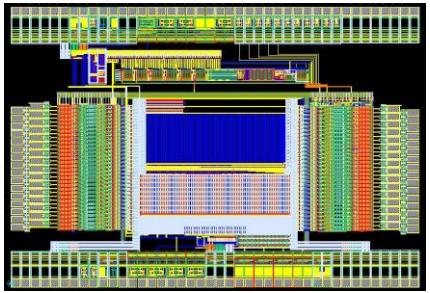
- By **2005**, Fermilab ASIC group is BUSY
  - 5 (!) ASIC engineers + Analog and Digital + Test engineers
  - Many projects, most in TSMC 0.25um (250nm)



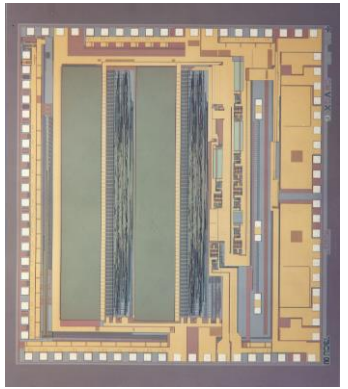
QIE9



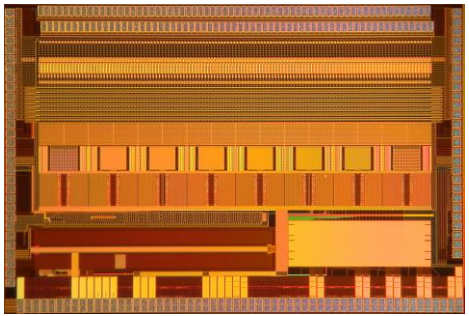
TriP-t



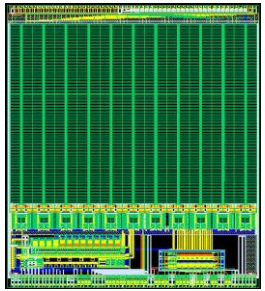
DCAL



RMCC



FSSR



FPIX2

+SVX4
+MASDA(X)
+APD RO (NOvA)
Going to 130nm

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Today

J. Hoff
- **C. Gingu**
- **A. Shenai**
- **C. Syal**
- **R. Wickwire**
- **(M. Hammer)**

S. Li
- **T. England**
- **H. Sun**
- **X. Wang**

G. Drake
- **D. Braga**
- **Q. Sun**
- **T. Zimmerman**

F. Fahim
Deputy Head
Quantum Science
Program, FQI

- + Test engineers, IT support, firmware support etc.

The power of Integrated Circuits

- Moore and friends – digital scaling

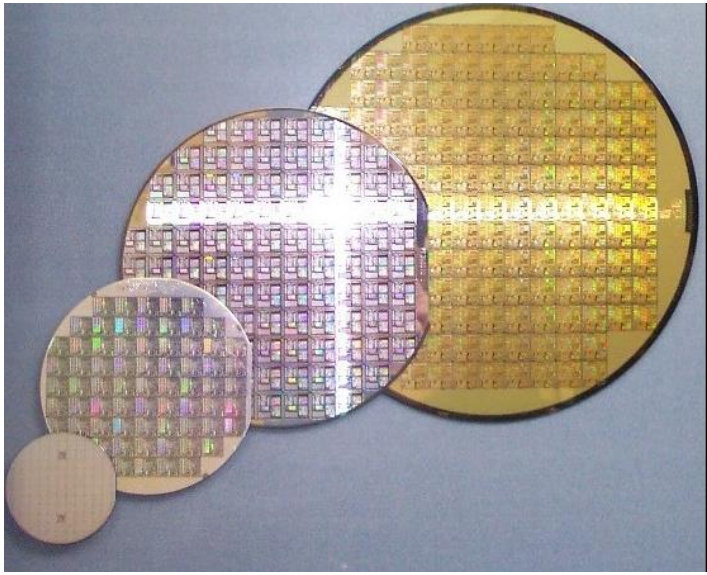
Scaled Parameters	Constant field Scaling
t_{OX}, L, W, X_j, W_d	$1/\kappa$
N_a, N_d $(ions/cm^3)$	κ
Power supply: (V_{dd})	$1/\kappa$
Electric field in device: (E)	1
Capacitance: (C)	$1/\kappa$
Inversion charge density (Q)	1
Circuit delay time: τ CV/I	$1/\kappa$
Power dissipation: (P)	$1/\kappa^2$
Power density $(\sim P/A)$	1
Circuit density	κ^2
Chip Area (A)	$1/\kappa^2$

MOSFET scaling (process nodes)

- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1981
- 1 µm – 1984
- 800 nm – 1987
- 600 nm – 1990
- 350 nm – 1993
- 250 nm – 1996
- 180 nm – 1999
- 130 nm – 2001
- 90 nm – 2003
- 65 nm – 2005
- 45 nm – 2007
- 32 nm – 2009
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm - 2018
- 5 nm - 2020

Future

- 3 nm ~ 2022
- 2 nm ~ 2024



4in wafer → 300mm wafer

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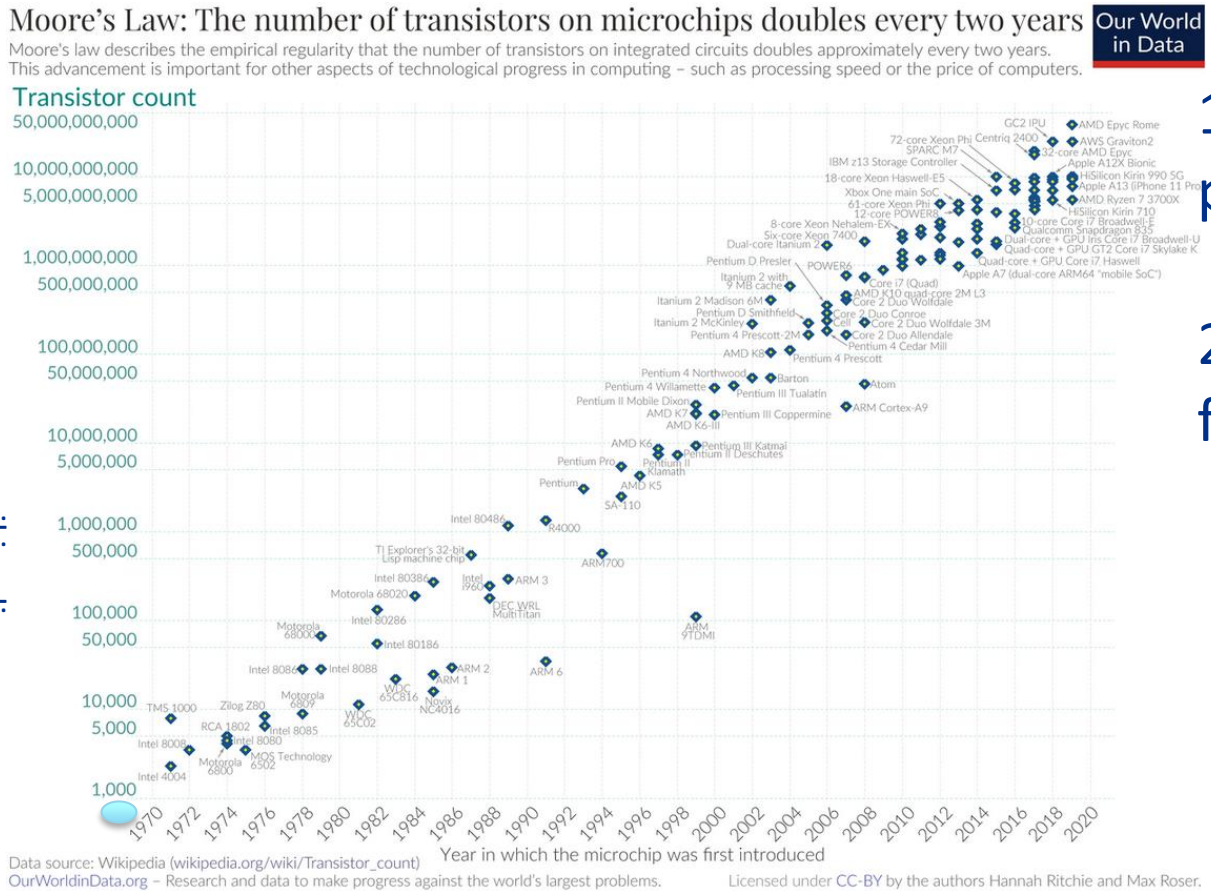
Moore's law cont.



wikipedia

1990: $25K for prototype run

2020: $40K for 55nm GF for 9mm^2 (50 chips)

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Analog scaling

P. O'Connor and G. De Geronimo
Prospects for charge sensitive amplifiers in scaled CMOS
NIM A 480 (2002) 713-725 Written exactly 20 yrs ago

Table 2
System parameters for ENC scaling simulation

System	C_{det}	t_s	P	I_{leak}	Detector	Typical application
a	30	75	10	0.001	Wire chamber	Tracking, imaging
b	15	25	0.2	10	Si Strip	Tracking
c	0.3	25	0.02	1	Si Pixel	Tracking
d	3	2500–500[a]	10	0.01	Semiconductor	Spectroscopy
UNITS	pF	ns	mW	nA	—	—

[a] For this system, the shaping time was varied at each L_g to optimize the overall noise (i.e., to make the white series noise and parallel noise equal).

Analog scaling cont.

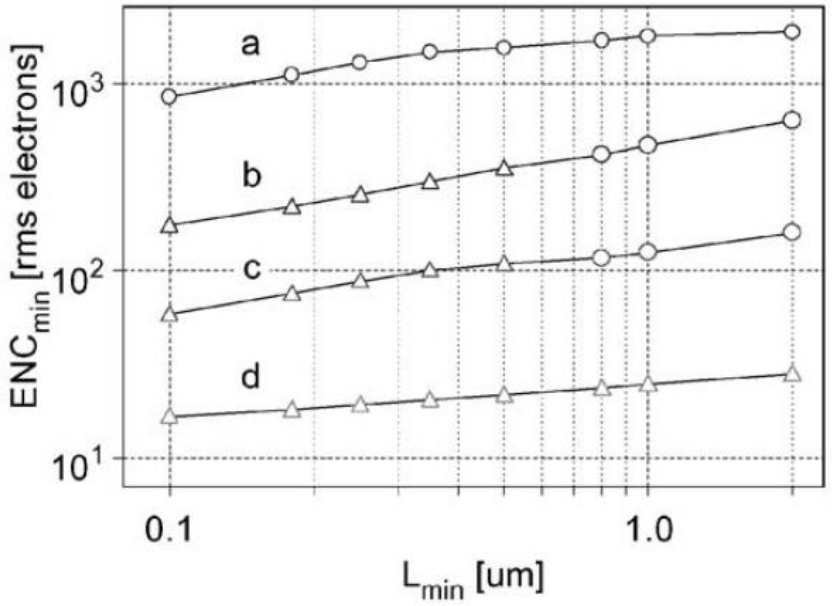


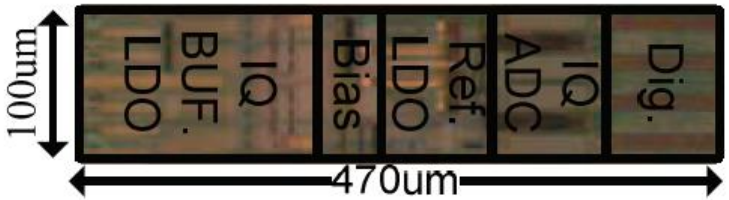
Fig. 6. Optimum total ENC as a function of the minimum gate length. Curves (a–d) refer to the system parameters given in Table 2. Circles = NMOS, triangles = PMOS.

ADC scaling

~10 to 14 bit, 100MSPS

FOM= Power/(2^ENOB *freq)

Technology	Year	Area (sq mm)	FOM (fJ/step)
250nm	2010	4.5	344
180nm	2012	0.5	89
130nm	2012	0.24	31
65nm	2012	0.19	46
28nm	2015	0.047	13



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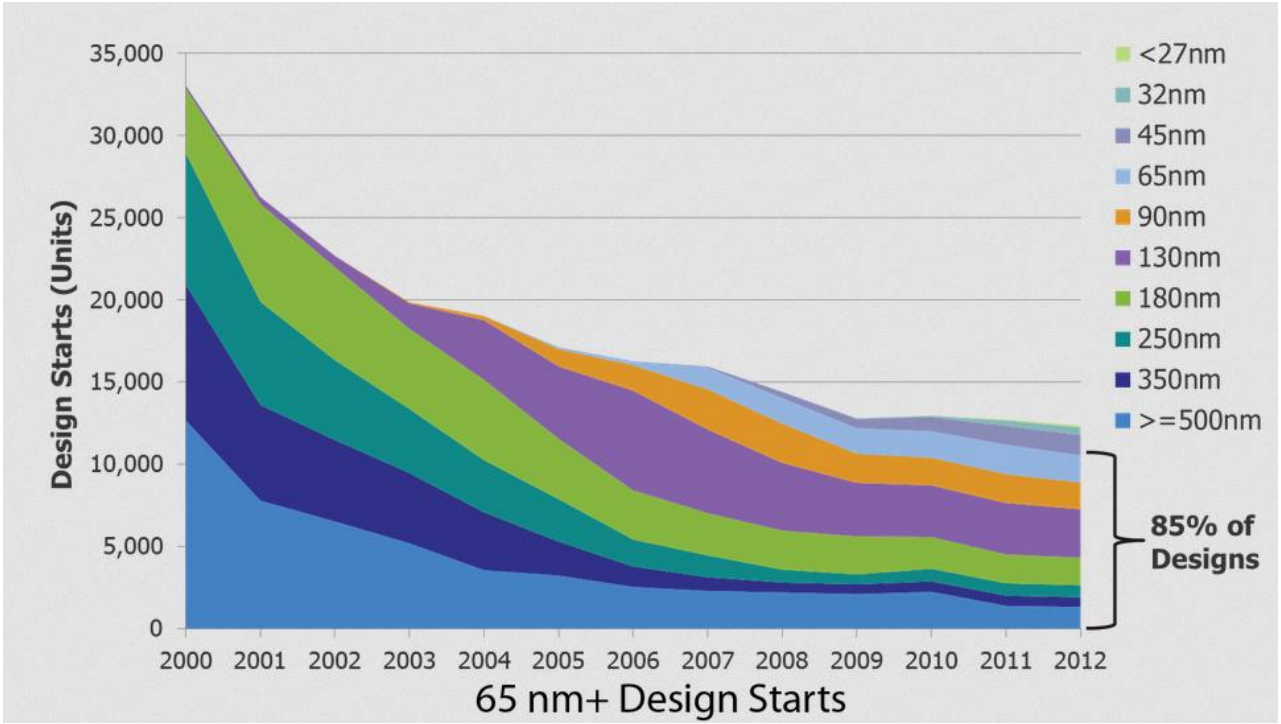
The power of Application Specific

- Moore's law does not drive design decisions



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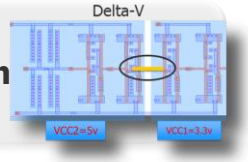
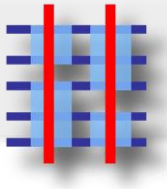
Functionality

28nm

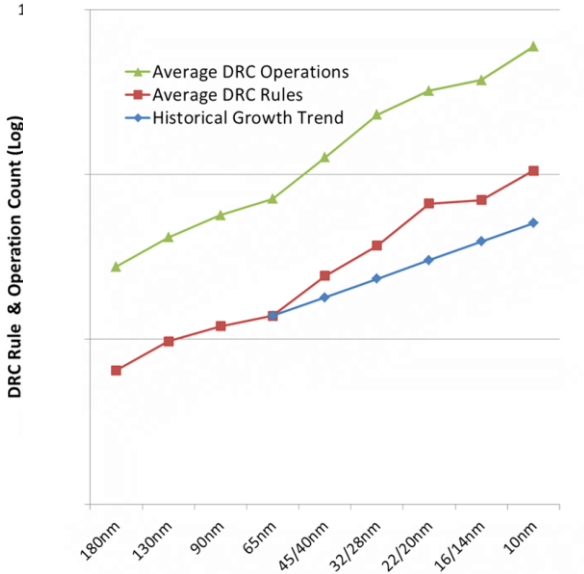
22/20nm

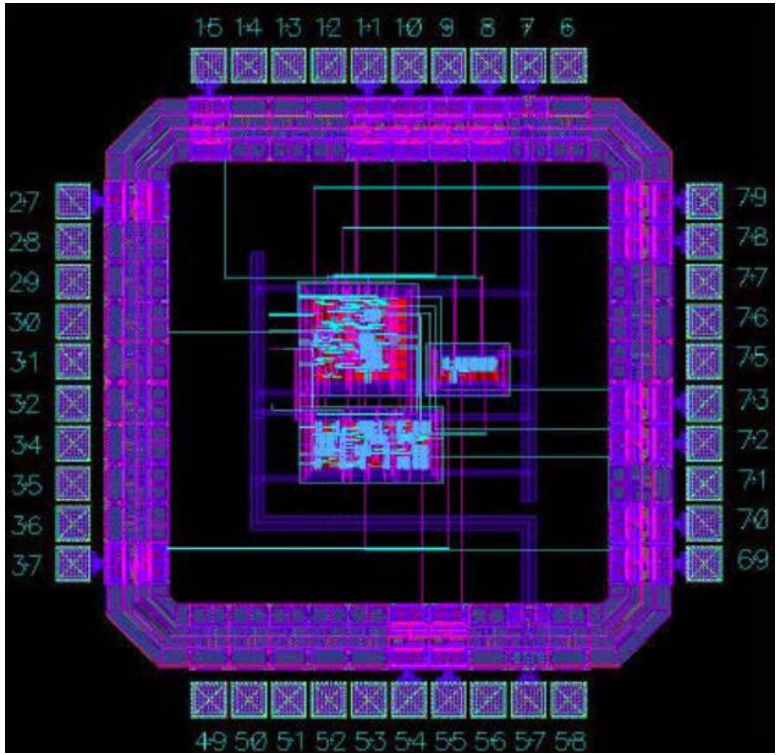


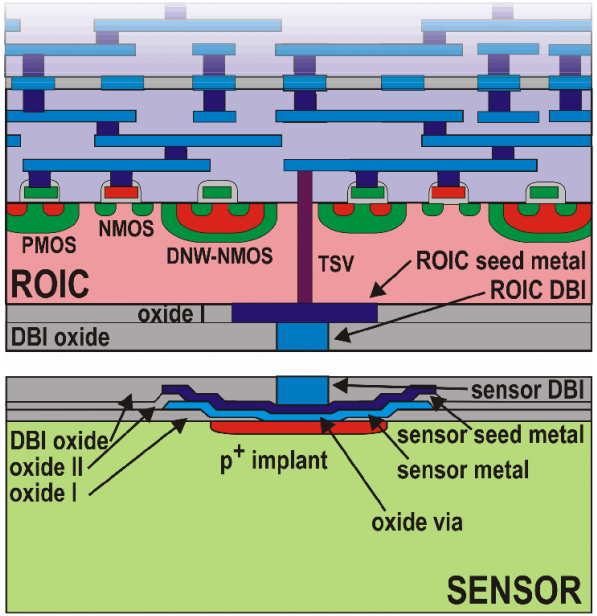
16/14nm



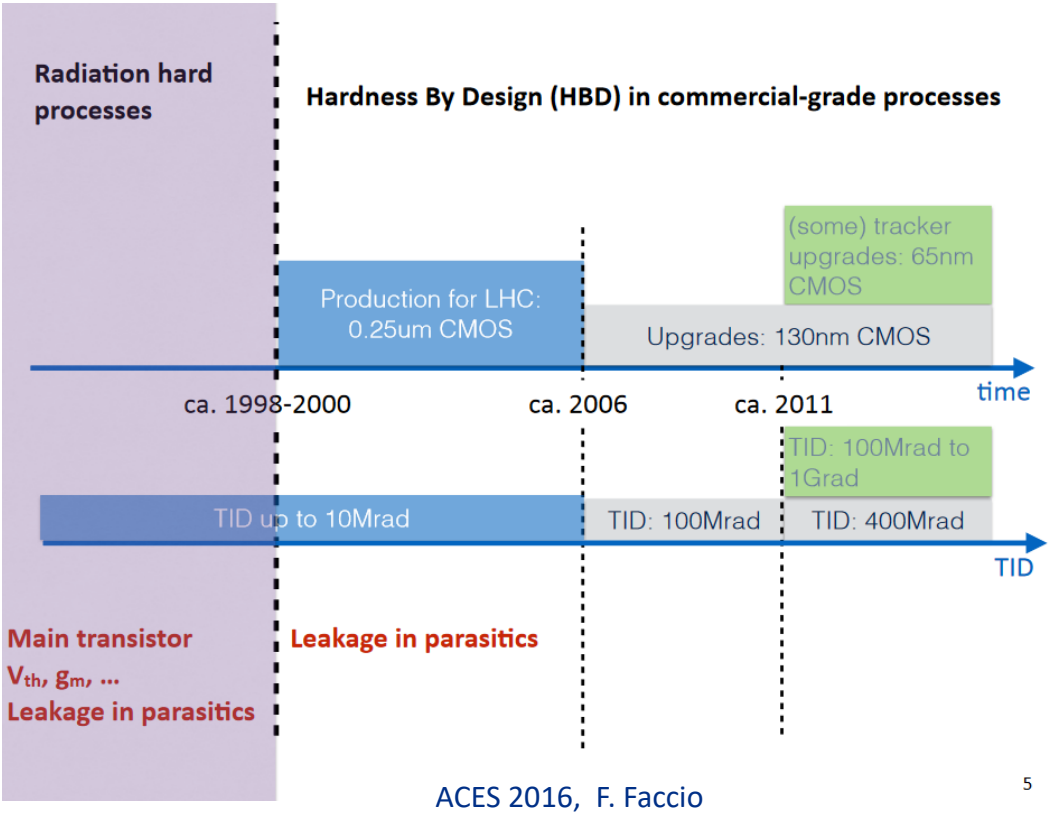
Complexity

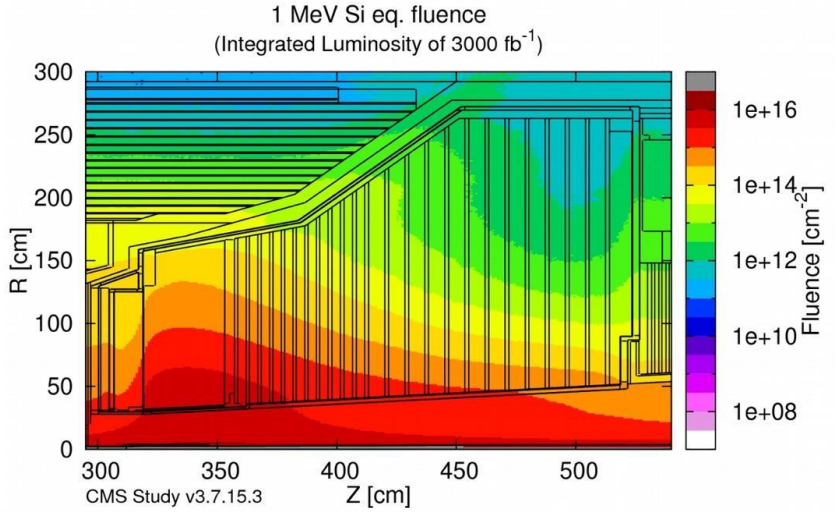


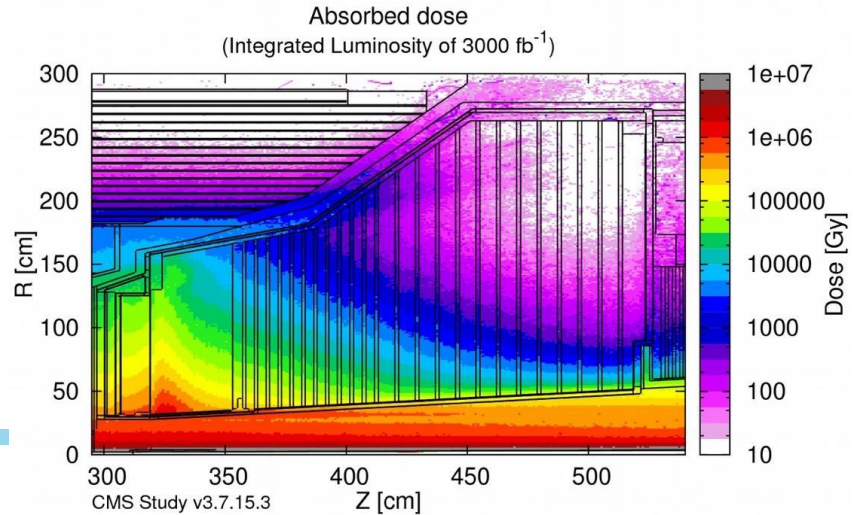

15 14 13 12 11 10 9 8 7 6
27 28 29 30 31 32 34 35 36 37
79 78 77 76 75 73 72 71 70 69
49 50 51 52 53 54 55 56 57 58


PMOS
NMOS
DNW-NMOS
TSV
ROIC seed metal
ROIC DBI
ROIC
oxide I
DBI oxide
sensor DBI
DBI oxide
oxide II
oxide I
p+ implant
sensor seed metal
sensor metal
oxide via
SENSOR

Need for Extreme Environments

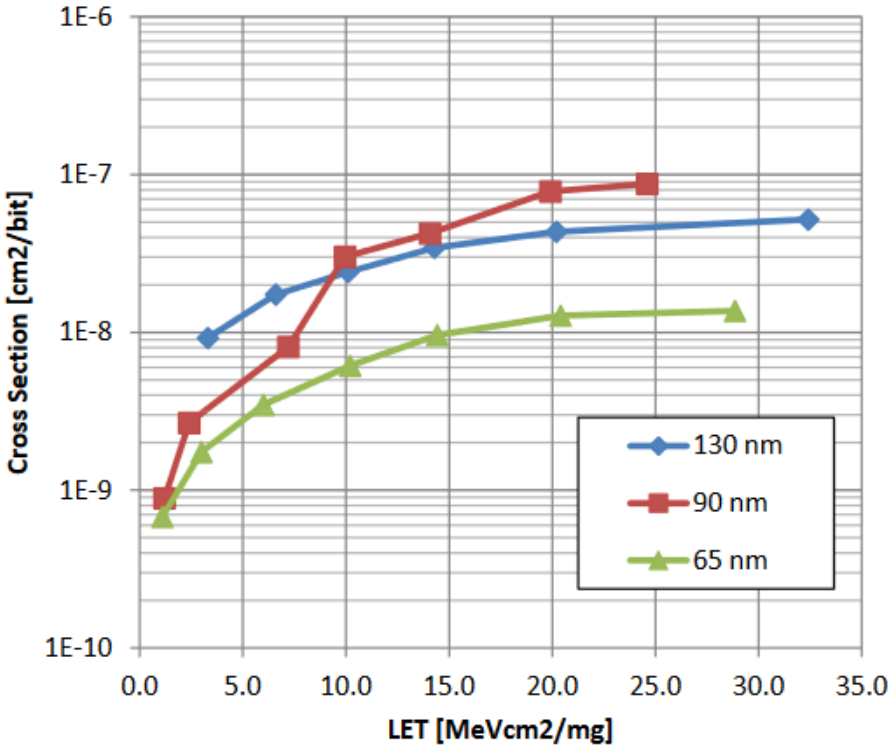


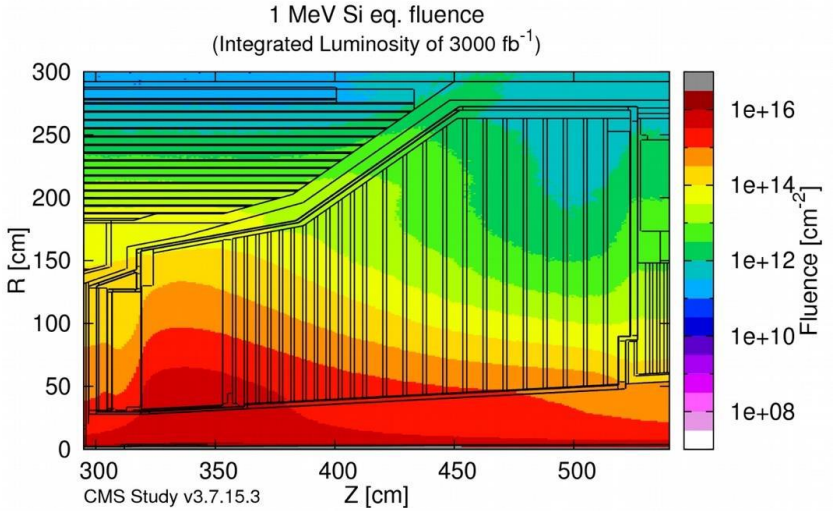


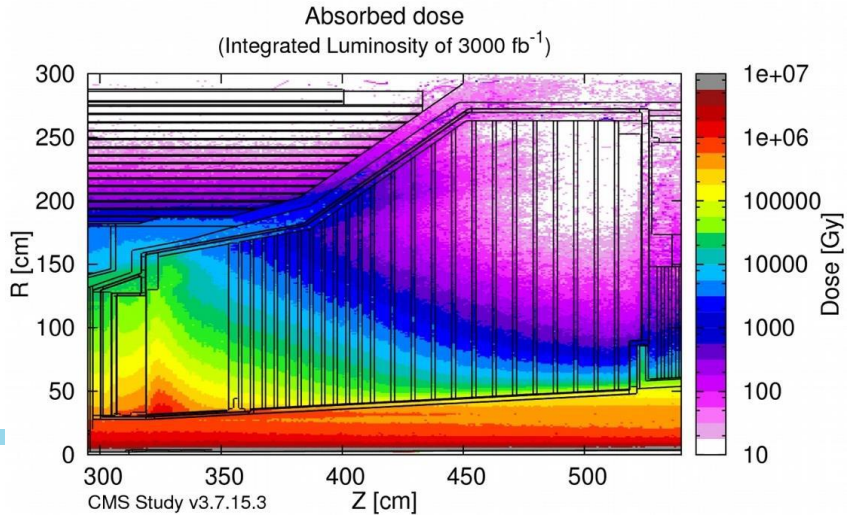


ACES 2016, F. Faccio
https://indico.cern.ch/event/468486

Need for Extreme Environments







Need for Extreme Environments

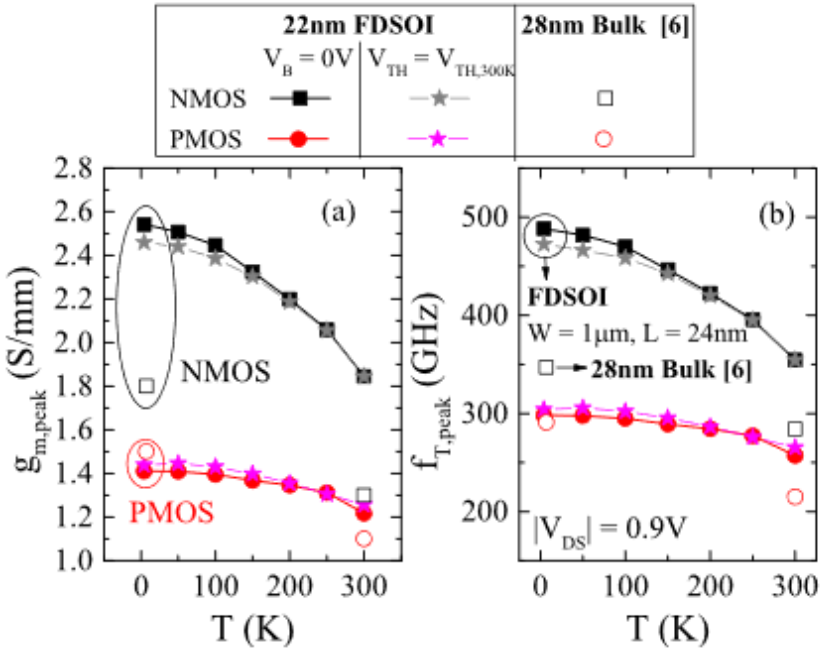


Fig. 5. (a) $g_{m,peak}$ versus T and (b) $f_{T,peak}$ versus T for nMOS and pMOS, at $V_B = 0$ V and at V_B needed to keep V_{TH} constant $= V_{TH,300K}$. $|V_{DS}| = 0.9$ V.

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 67, NO. 11, NOVEMBER 2020 4563

Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications

Bruna Cardoso Paz, Mikaël Cassé, *Member, IEEE*, Christoforos Theodorou, Gérard Ghibaudo, *Fellow, IEEE*, Thorsten Kammler, Luca Pirro, Maud Vinet, *Senior Member, IEEE*, Silvano de Franceschi, Tristan Meunier, and Fred Gaillard

(Invited Paper)

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Projects within the ASIC group (current, recent and near future)

CMS Upgrades

ECON-T and ECON-D: data concentrators for trigger and DAQ paths of HGCAL

ETROC: precision timing for MIPs in the forward region using LGADs

DUNE Cold electronics

COLDADC: (with LBNL and BNL) 16ch, 12 bit, 2 MSPS ADC

COLDATA: “Digital-on-Top” leveraging FNAL cold models. <1E-15 BER @25m and1.28gbps

65nm

GLOBALFOUNDRIES®

22nm FD SOI

Projects within the ASIC group (current, recent and near future)

Quantum projects

MIDNA: readout of Skipper CCDs to allow large number of channels

SNSPD: readout of Superconducting Nanowire Single Photon Detector (part of QuantISED)

ACC1: Atomic Clock Control – shrinking Atomic Clocks to be chip sized (part of QuantISED)

CITC1: Cryo-electronics Ion Trap control for Qubits and other quantum applications

CryoADC: Collaboration with Microsoft, component for quantum computing

Skipper in CMOS (R&D) : extending Skipper technology to CMOS sensors

SiSeRO (R&D) : Joint development with MIT LL to extend Skipper technology to MIT-LL process

Other:

FALCON: High speed Xray camera for APS upgrade at ANL

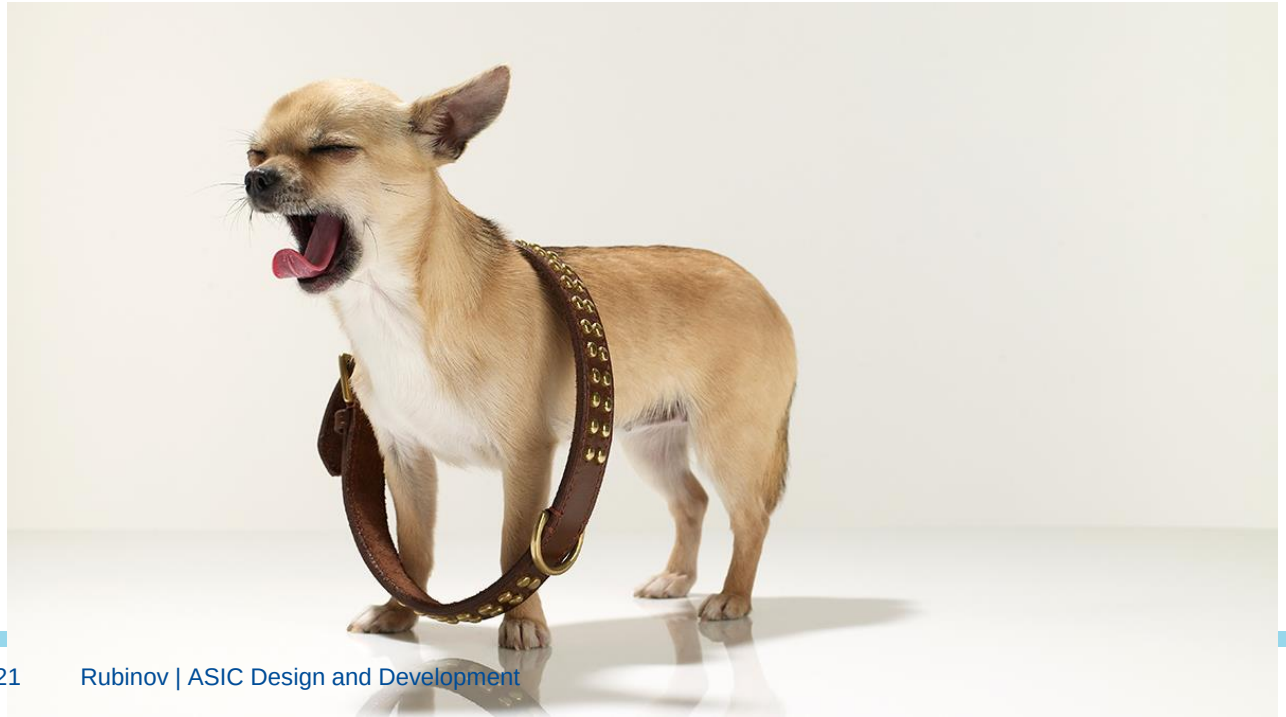
VIPRAM (130nm): 3D CAM (Vertically Integrated Pattern Recognition Associative Memory)

Take Home Message

One Size does NOT fit all.

Fermilab ASIC group is here to do apply expertise in

Integrated Circuits to our **Specific Applications**



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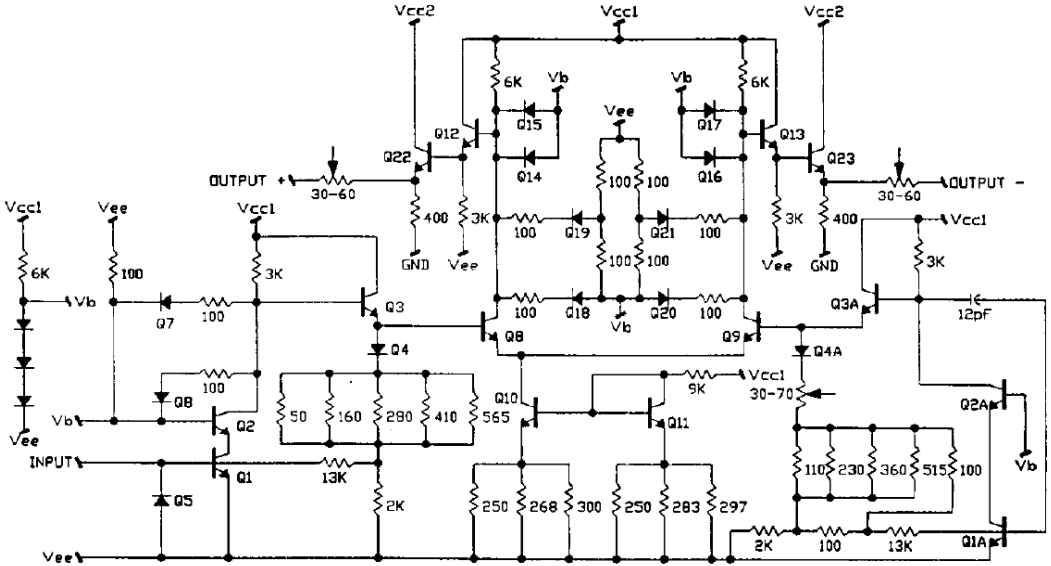
BACKUP

Backup: MPW prices from Europractice

GLOBALFOUNDRIES

Technology	Standard EUR / mm^2	Discounted EUR / mm^2
GLOBALFOUNDRIES SiGe 8HP	3,800 [1]	3,600 [1]
GLOBALFOUNDRIES 130 nm BCDlite	1,500 [2]	1,400 [2]
GLOBALFOUNDRIES 130 nm LP	1,500 [2]	1,400 [2]
GLOBALFOUNDRIES 90WG Silicon Photonics	5,250 [1]	5,000 [1]
GLOBALFOUNDRIES 55 nm LPx-NVM/LPx-RF	4,000 [2]	3,800 [2]
GLOBALFOUNDRIES 55 nm LPe	4,000 [2]	3,800 [2]
GLOBALFOUNDRIES 45RFSOI	7,350 [2]	7,000 [2]
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	5,000 [2]	4,700 [2]
GLOBALFOUNDRIES 28 nm SLP/SLP-RF	10,200 [2]	9,700 [2]
GLOBALFOUNDRIES 22 nm FDSOI	14,000 [2]	13,200 [2]

BACKUP: QPA02



QPA02 Schematic Diagram

4 chan
Gain = 17mv/fC
ENC = 1600e @ 20pF
Rise = 6 ns
Falltime = 12ns
Power = 42 mw/channel

R. Yarema, “ASIC Design at Fermilab”, FERMILAB-Conf-91/170