Trigger Primitive (TP) Readout

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Upstream DAQ Software

Outline

- Upstream DAQ PD-II WBS v0
  - Readout/TPG Firmware
    - 3. Finalise TP FLX output format - ongoing, need to get OK from SW POV
  - Readout/TPG Software
    - 2.a.v. TPLinkReader - not started -> TP Fake Reader
    - 2.b. Design and implementation of latency buffer - fixed (done), dynamic (design underway)
    - 2.e. Implement DAQ module for TP readout/publication - not started
    - 5.b. Implement TPG overlay
    - 6.b. TP Control

- Update on ongoing work
  - TP FLX dataformats
  - ‘readout’ repository in DUNEDAQ v2.2.0 Release - MiniDAQArising
  - Next steps

FLX Output Dataformat for TP Packets

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	
0xABCD (start of block symbol)	Seq. number, E-Link ID	FLX block header
0x3C	0x0	SOP/SOF CR (removed by FLX card ?)
flags	wire ID, fibre, crate	TP header
timestamp	timestamp	..
timestamp	timestamp	..
hit stop	hit start	TP hit frame
hit peak time	hit peak adc	..
flags, hit continues	hit sum	..
hit stop	hit start	TP hit frame
hit peak time	hit peak adc	..
flags, hit continues	hit sum	..
accumulator	median	TP pedestal information
0xFOOD	0xFEED	..
0xBEEF	0xDEAD	..
0xDC	0x0	EOP/EOF CR (removed by FLX card ?)
Type(3), T(1), E(1), C(1), (sub-)packet size(10)	0x0	FLX trailer
...	...	
...	...	
...	...	
...	...	
...	...	
Type(3), T(1), E(1), C(1), (sub-)packet size(10)	0x0	FLX block (1 KB)
0xABCD (start of block symbol)	Seq. number, E-Link ID	FLX block header
...	...	

-- No need to add new "magic" words ?

-- CR's SOP/EOP word removed by FLX ? - OK

-- FLX block 1 KB

-- FLX header and trailer

TP BR output format to DS not discussed here

FLX Output Dataformat for TP Packets

- Comments
  - TP packets traverse several firmware components before reaching the Felix card
    - TPG core, Arbitrator, Compression, Central Router (CR), Wupper, Felix card (FLX)
    - Data words can be stripped or added
    - Firmware formats mostly fixed
  - We are interested in the output format from the Felix card
    - These data will be read out by the TPLinkReader
    - A fixed format or several versions of the FLX output format ?
  - TPG core pedestal information frame is optional
    - Magic words used also for padding to 3 32-bit words
    - Will the pedestal information frame format change in PD-II ?
  - Selection of FLX output format can be controlled via run configuration
  - The FLX output format should allow to interpret the TP information correctly and easily
- Conclusion
  - No need to for major changes to the existing formats (used in PD-I)
  - Next revision after first implementation of TP FLX output format in ‘dataformats’ repository

Trigger Primitive (TP) Fake Card Reader

- Development in latest DUNE DAQ release - DUNEDAQ v2.2.0 Release - MiniDAQArising
  - Setup software release work area and environment
  - Clone 'readout' repository from github
    - Modify, compile, build, run code
  - First implementation of 'TP' inside FakeCardReader module
    - plugins/FakeCardReader.cpp
    - plugins/FakeCardReader.hpp
    - src/CreateLatencyBuffer.hpp
    - src/CreateRawDataProcessor.hpp
    - src/CreateRequestHandler.hpp
  - Configuration
    - test/fakereadout-tp-commands.json (enables TP links only)
    - test/fakereadout-wib-and-tp-commands.json (enables WIB and TP links)
- Run Control commands
  - init, conf, start, stop
  - Both WIB and TP fake card readers running

Produced Packet rate: 166.003 [kHz]
Produced Packet rate: 166.003 [kHz]
Consumed Packet rate: 166.003 [kHz]
Consumed Packet rate: 166.003 [kHz]

Next Steps

- Discuss/review current implementation (software ‘sprints’)
  - Current ‘TP’ fake card reader a placeholder for the TP fake card reader
    - Internal TP implementation same as for WIB
    - Implement TP FLX output format in ‘dataformats’ repository
    - Create TP frame.bin input file containing TP frames
    - Use binary data captures from protoDune-I taken in summer 2020
    - Add TP in configuration generations scripts (Python, jsonnet)
  - Enforce correct TP link numbering, e.g.

Super Logic Region (SLR)	WIB links	TP links
card0	0, 1, 2, 3, 4	5, (6, 7, 8, 9)
card1	6, 7, 8, 9, 10	11

  - Implement TP latency buffer
  - Discuss whether TP fake card reader can/shall evolve as a separate appfwk module
- Changes in forked repository
  - https://github.com/hristovaivana/readout/tree/hristova/tp_fakereadout