# System design

- Number of feedthroughs on pressure vessel will be limiting and we want to limit the analogue signal path length
  - Therefore must digitize and zero-suppress inside vessel before sending out of vessel
- Design underway of aggregator cards in UK and of ASIC host cards in USA
- Timing information will also need passing in to aggregator cards

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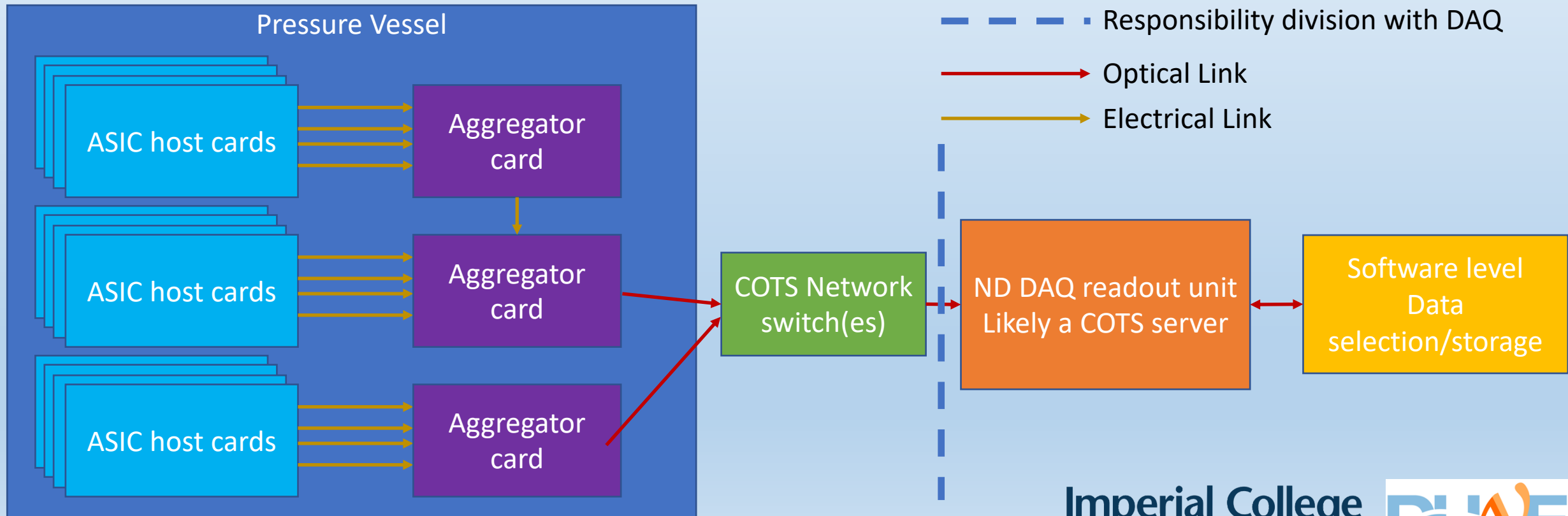
Calibration

- Systems involving reading data from above system seem fine
  - i.e. zero suppressed pre-digitised
- Discussion of access to raw waveforms, seems LArPix can do this for single channel at a time. Would likely do as a special run. Do we need more than this?

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Longitudinal single sample resolution

- Choice of digitizer ASIC must have sufficient sampling frequency

- Argon gas has drift velocities O(10cm/us)

| Required resolution	Implied Sampling Frequency
1cm	10 MHz
1mm	100 MHz
100um	1 GHz

- Donna gets similar numbers (3mm resolution for 150 MHz) based

- Does not take into account longitudinal diffusion

- However, these are single sample resolutions so significant improvement from fitting multiple adjacent pixels **SIMULATION GROUP OVERLAP**

  - ALICE achieve 1300um precision with 5-10 MHz sampling

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Digitiser ASIC options

- LArPix is front runner, but here are some other options for comparison

- Need to consider magnetic tolerance, resolution and gain too **(see slides from Alysia with gain simulations)**

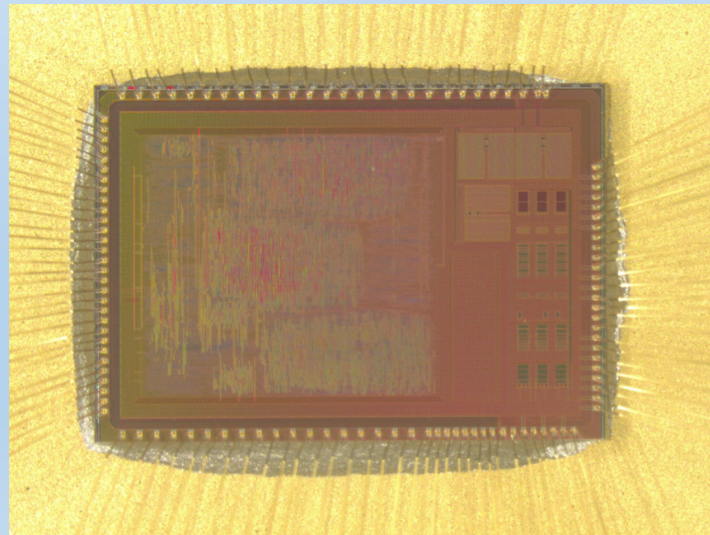- Host and aggregator boards will also contribute to thermal budget

LArPix v2 chip

- 64 channels at 500kHz (but can be upgraded (interest in doing this in Rutgers, FNAL, UC Santa Barbara
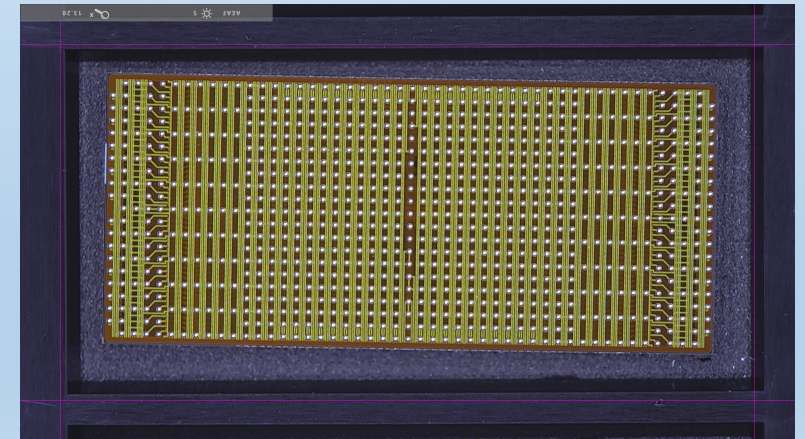
- ~100 uW/channel (will go up with speed increase)
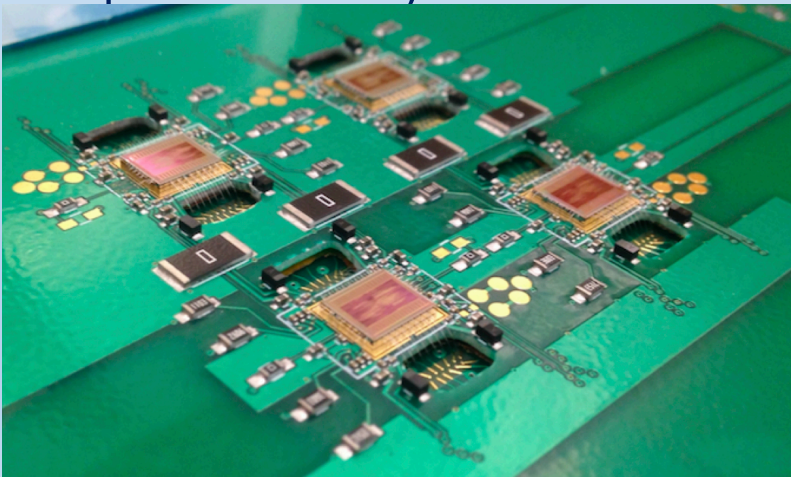
SAMPA chip develop for ALICE TPC upgrade

- 32 channels at 5 or 10 MHz

- ~35 mW/channel

HGROC chip developed for CMS HGCAL

- 72 channels at 40 MHz

- ~15 mW/channel

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ASIC host cards

- Input is analogue electrical signals from detector
  - Each one will be positioned in a block of 3 ALICE ROC slots using an edge connector as 64 channels matches number channels a single LArPix v2 can read: implies ~11,000 of these cards
- Primary role is digitization of signals and zero-suppression
- Version with LArPix v1 has been designed by Pittsburgh and will be tested using GOAT
  - LArPix v2 will be easier as signal inversion can be done on LArPix with v2

Analogue
Electrical
Signals

ASIC host card

Digitiser
ASIC

Digital
Electrical
signals

Aggregator
card

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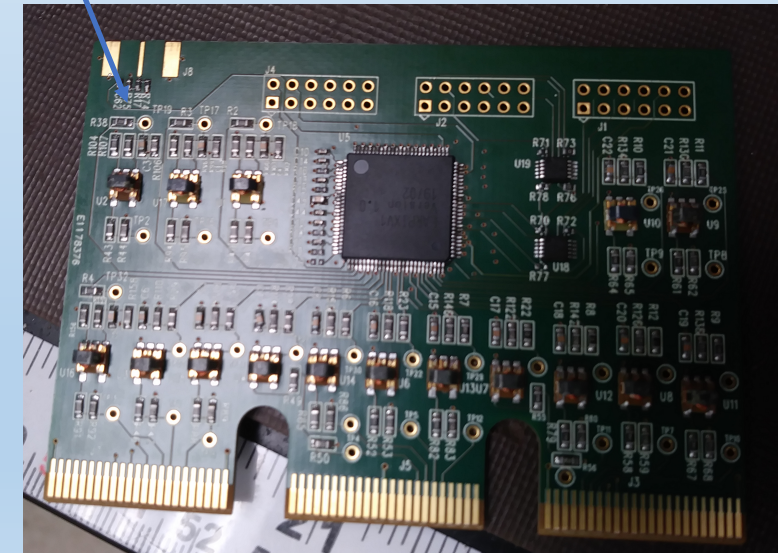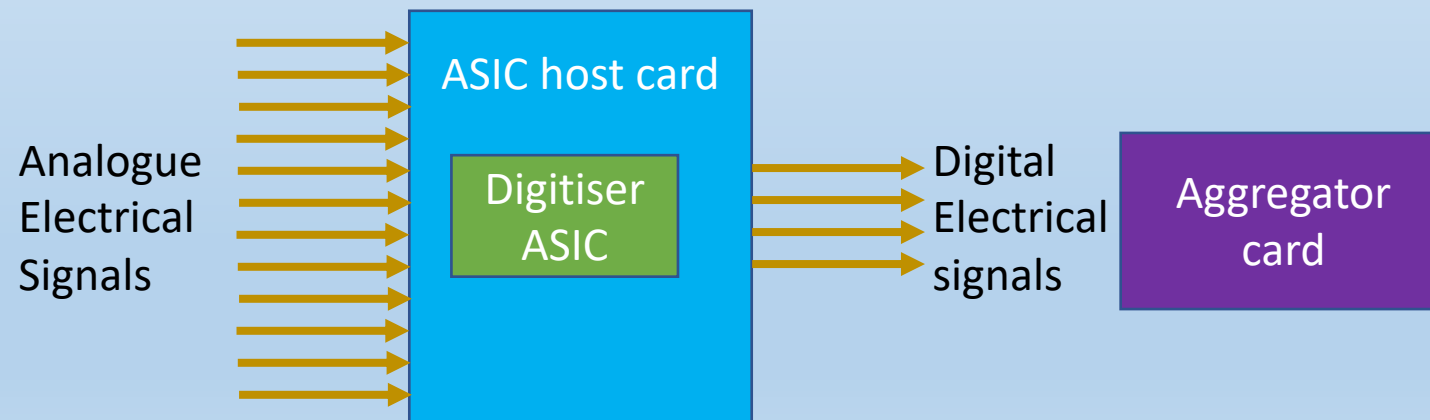
Aggregator cards

- Input is digitized electrical signals from ASIC cards
- Primary roles are controlling ASIC cards, electrical to optical change and consolidation into fewer links
  - Inter-card communication can reduce number of links further as limit seems unlikely to be throughput of FPGA but number of LArPixs that a single FPGA can be interfaced with
  - Can also buffer to even out data rate and do necessary low-level processing
- Connecting ~100 LArPix to each FPGA implies ~110 of these cards
  - Could reduce with inter-LArPix communication

Digital Electrical Signals

Aggregator card

FPGA

Aggregator card

FPGA

Pressure vessel

Digital Optical signals

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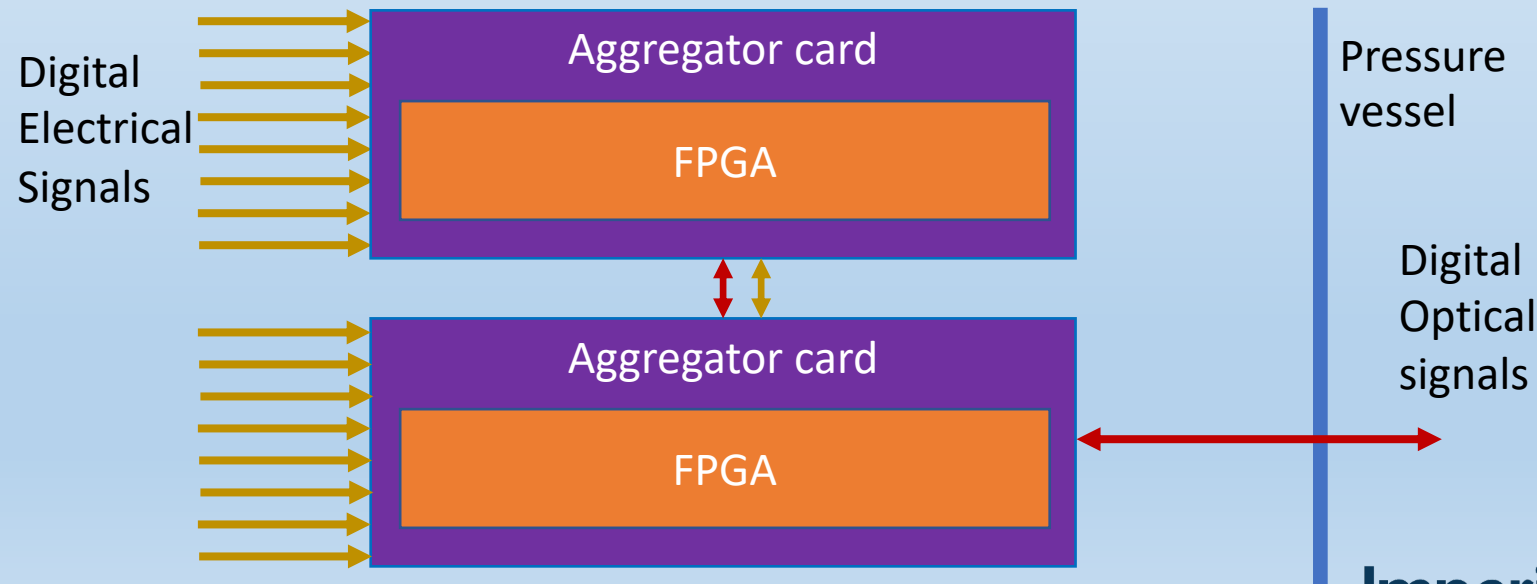
Heat

- Very rough numbers:
  - 110 HPgTPC aggregators: FPGAs (5-8 W per aggregator), 1W 10 Gb/s, extra for powering. Todo for IC to get more accurate numbers
  - 11,000 HPgTPC ASIC host cards: LArPix v2 <150uW/ch, will go up when we increase sampling frequency. V1 prototype board is ~2mW for one board, estimate ~12.4mW per ASIC for LArPix v2

- Looks like ECAL may dominate. In any case looking at O(kW) from HPgTPC

- **Interaction with mechanical group: what does cooling this look like?**

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How many optical link feedthroughs do we need? Back of the envelope numbers

- How much data will we be generating?
  - 700,000 channels means ~11,000 uprated LArPix chips
  - Maximum data rate of a 500kHz LArPix v2 is 5Mb/s so assume a maximum of 50 Mb/s for 5MHz
  - This gives a maximum of 550 Gb/s if LArPix stream out at max rate but this is not likely
  - Pessimistically assuming 135 Hz of cosmics at 10% occupancy plus 100% occupancy beam data gives 47 Gb/s
  - Early numbers from Tom Junk give 130,000 hits per event implying less than 1 Gb/s
- How much data can we put out per link? NB 1 link equals two fibers
  - Special high pressure tolerant fiber SFPs can support ~4 Gb/s, standard FPGAs can support 6.25 or 10 Gb/s so let's use 4 Gb/s as an illustrative number
  - Assume 10% for framing, error correction etc. so 3.6 Gb/s per link
- This gives an absolute maximum of ~150 links, a pessimistic ~16, and maybe even 1
- In the latter two cases connections between boards and routing inside pressure vessel likely to be the limit. E.g. 1 link not practical for reading out both ends of detector
- Above does not including timing distribution

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Timing

- Details of ND DAQ timing system not finalized including where line of responsibility is
- Potentially could send timing information to network switch and distribute via PTP over existing links to aggregator cards if accuracy of this method is good enough
- If need to send timing endpoints directly to aggregators this would increase number of links
  - Likely not an extra link per card as aggregators could distribute timing between each other
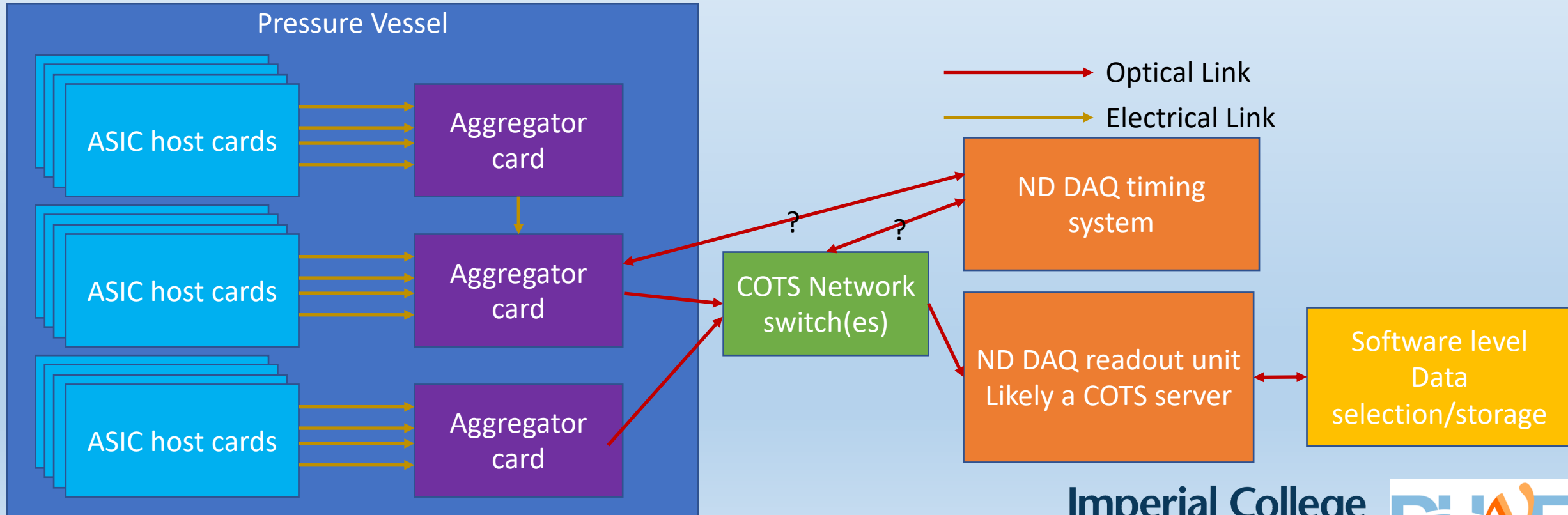
Slow control (SC) and Control, Configuration & nearline Monitoring (CCM)

- CCM envisaged to take place through system described so far
  - Homework: Follow up with FD to see how advanced their system is
  - Lots of questions on how to deal with temporary and longer term board failure.
  - Need to specify conditions detector must keep running in and where it's ok for run to crash
  - Also questions on special runs for calibration etc.
- Slow control will probably be mostly a different system. Recorded items will probably mostly be from mechanical group discussions plus board temp etc.
  - Drift HV, ROC HV, pressures, gas composition monitoring, temperatures, control of filling system, control of cooling system. Electronics voltages LV. Also current monitoring to check for sparks
  - Do we send straight to ND DAQ SC solution or do we need any on detector processing, ND DAQ solution also not extant yet

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Testing (slices etc.)

- GOAT and UK pressure vessel have an IROC and OROC respectively
- Aiming to build up full slice test up to DAQ boundary as components are ready
  - Start with ASIC host card (spares of v1 exist so should be able to have one in London too) controlled by miniZ or similar then add aggregator and more up to date host card as we can
- Also at some point will want a full chain all the way to offline including ND DAQ
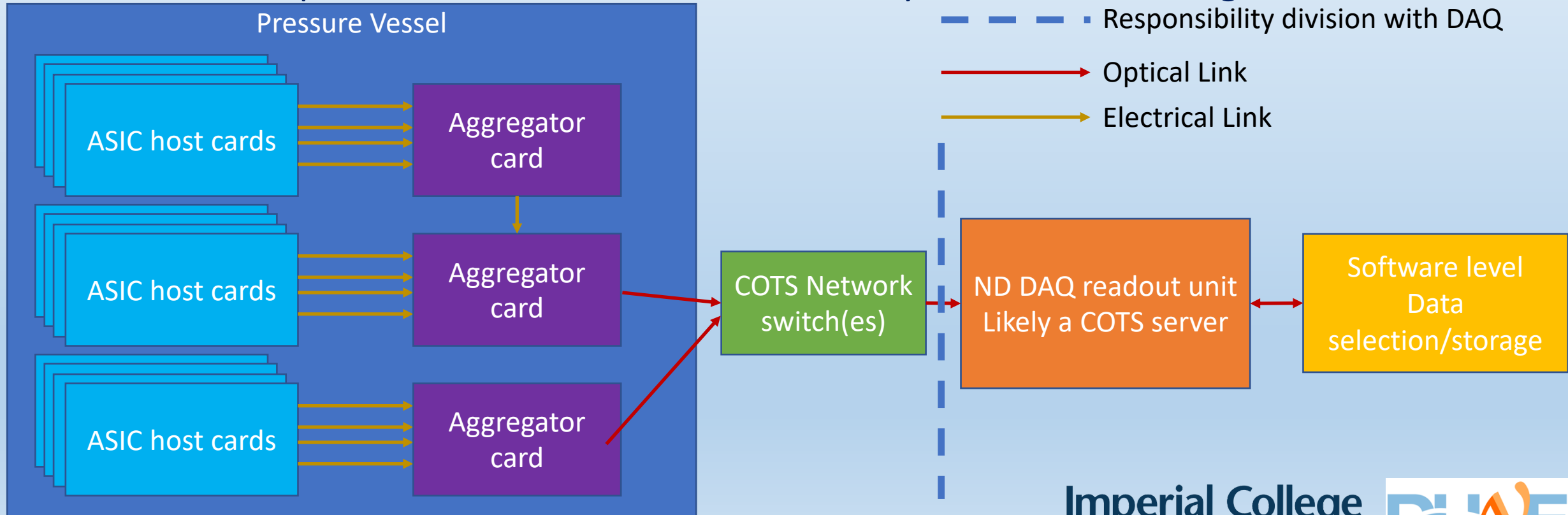
Summary

- Design of HPgTPC readout electronics is underway with some early prototypes starting to be available for some components

- Details of occupancy from simulation efforts will be essential for optimising system design

- Timing system needs have not been included in estimates of numbers of links

- Thermal budget will also be necessary to estimate and set requirements on so we can spec cooling

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