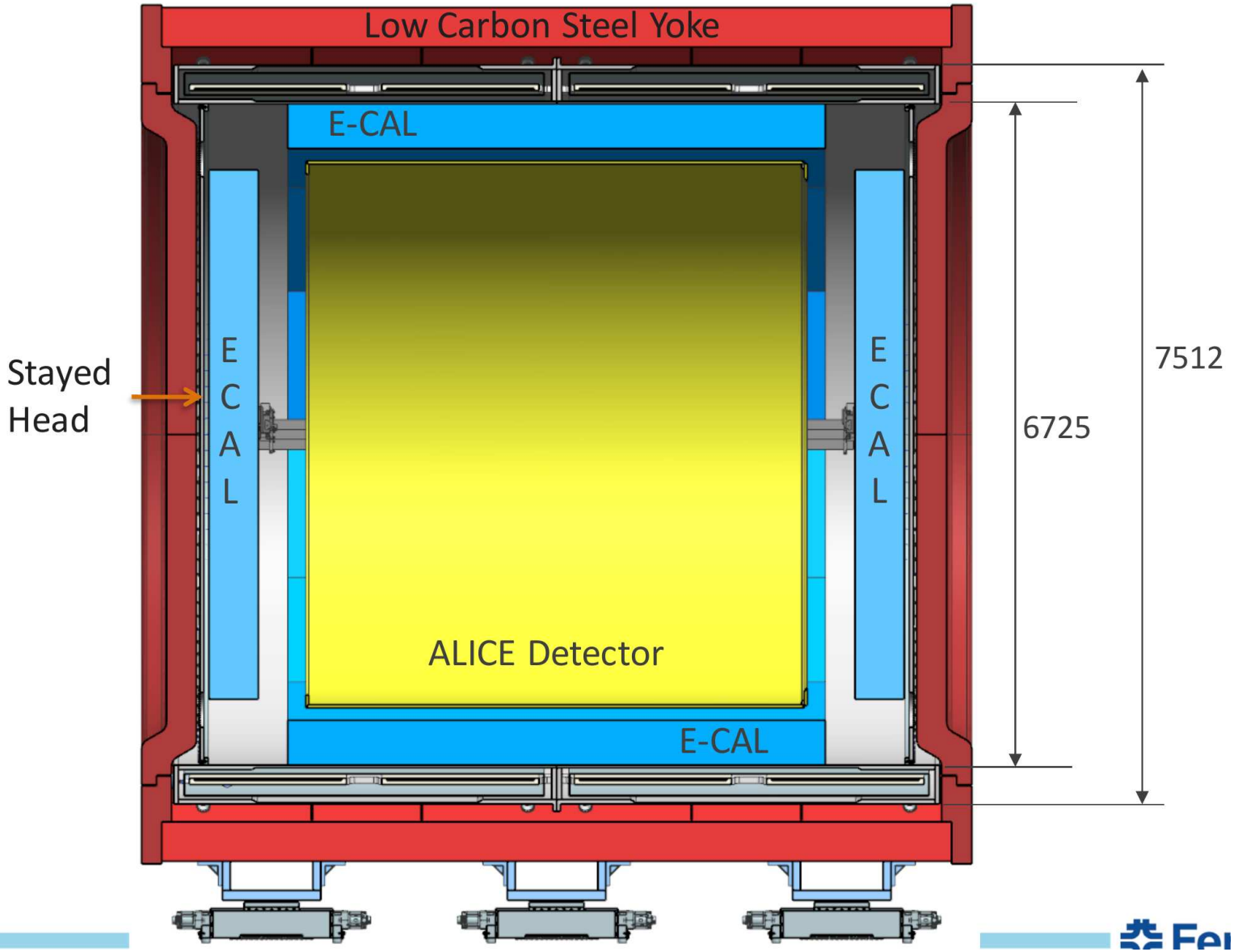
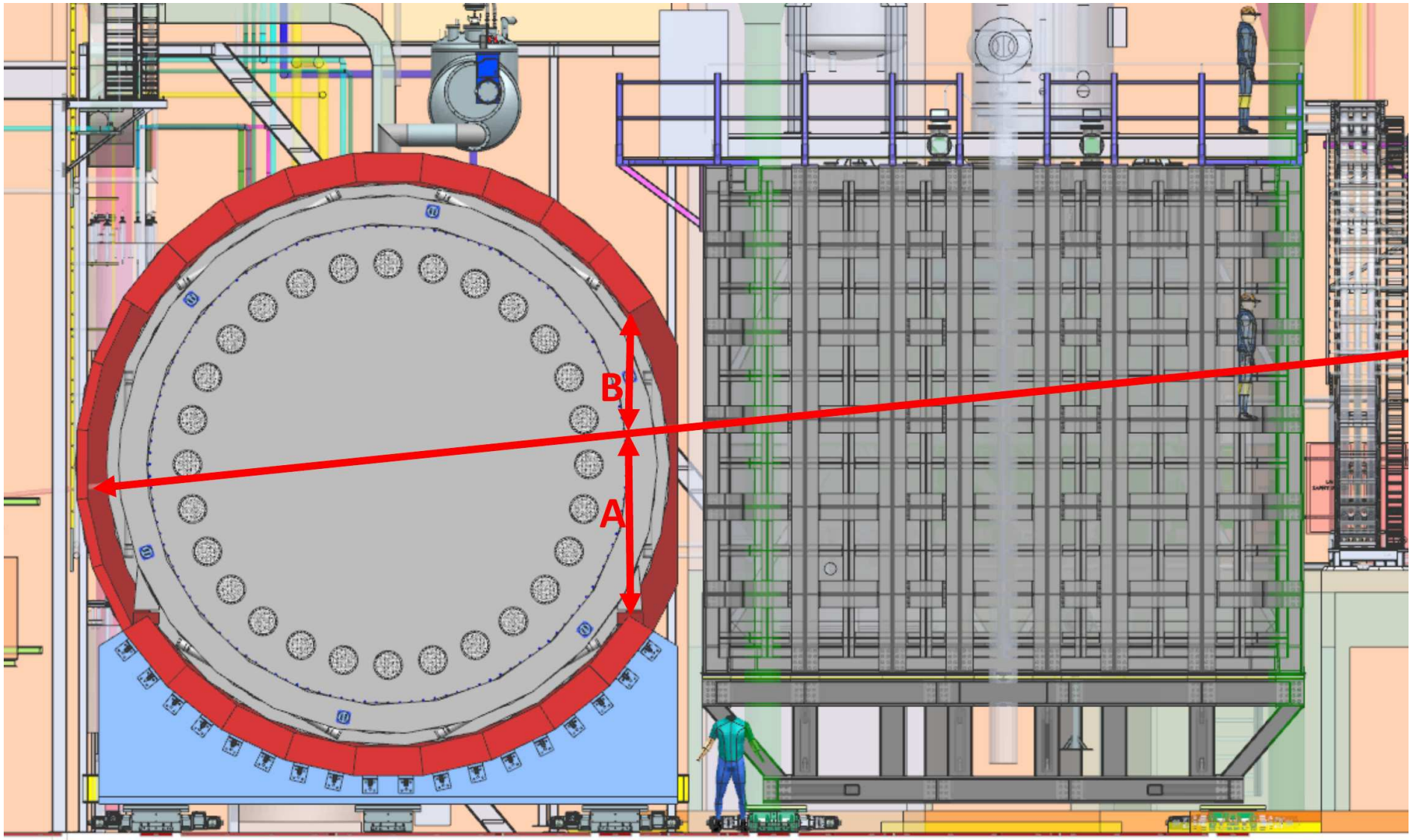
Choice of FPGA

- LArPix signals (1.8V CMOS):
  - MOSI: Individual per LArPix (to maximize bandwidth)
  - MISO: Some potential for sharing between chips of we're clever with RST_SYNC, otherwise individual per chip
  - CLK: can possibly be shared between a small number of chips
  - RST_SYNC: Can be shared between chips.
  - Setup/hold-time limitations on fanout? Layout presented below may require 45cm cables.
  - EXTERN_TRIG: probably not needed?
  - 1.8V power: 6.9 mA@100 MHz, 10x at 100 MHz?
- XCKU035-1FBVA676C: Modern, relatively inexpensive via CERN, 312 IOs, 19Mbit blockram last time we were worried about a possibly hermetically sealed heat spreader. This was unwarranted, this device doesn't have a spreader.
- XC7A75T-1FGG676C: Single-unit price less than half of KCU, 300 IOs, 3.9Mbit blockram. EOL 2030, price may increase when/if it becomes mature.
- XC7A200T-1FBG676C: Single-unit price comparable to KCU volume, 400 IOs, 13Mbit blockram.

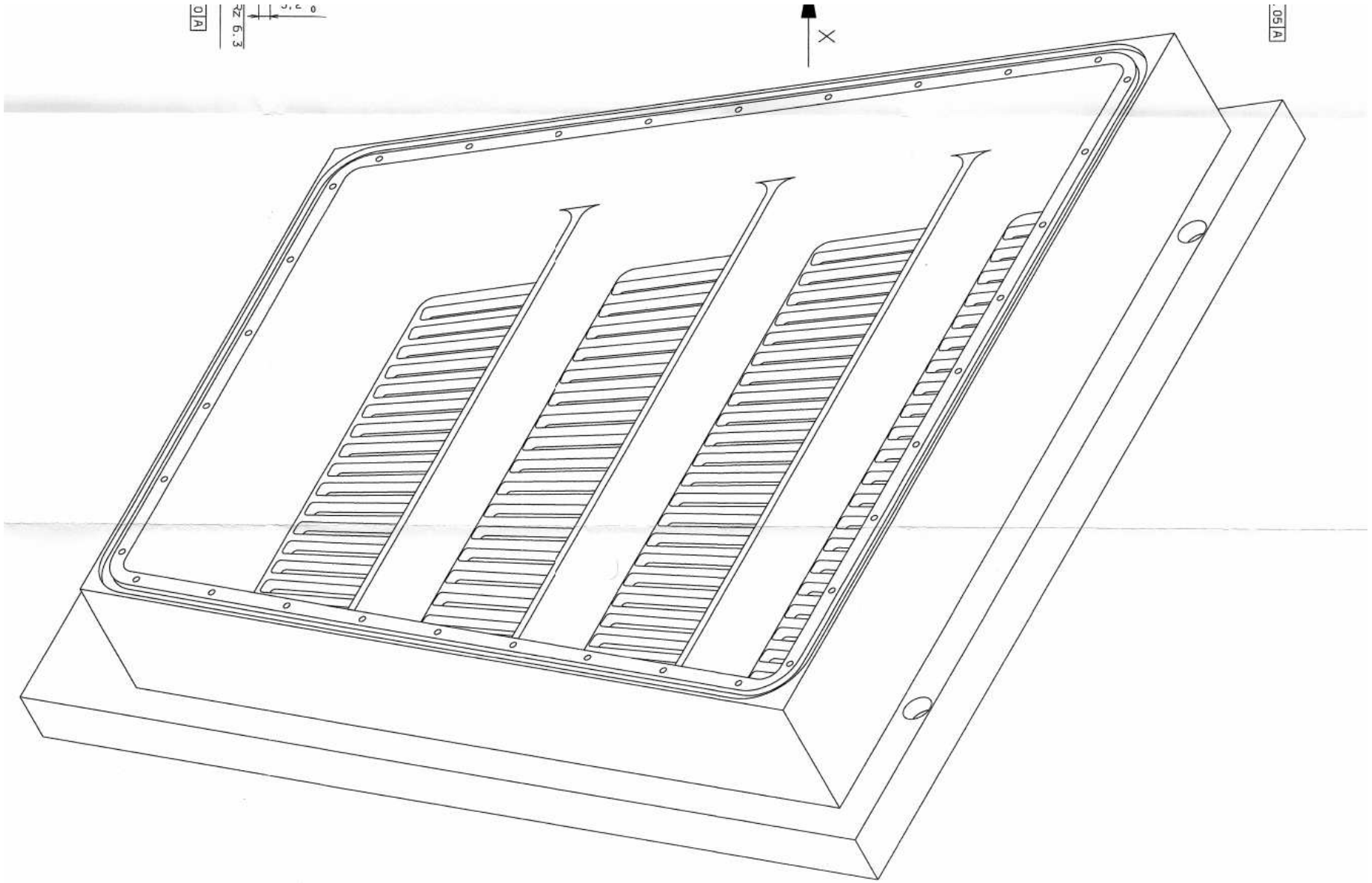
Detector geometry



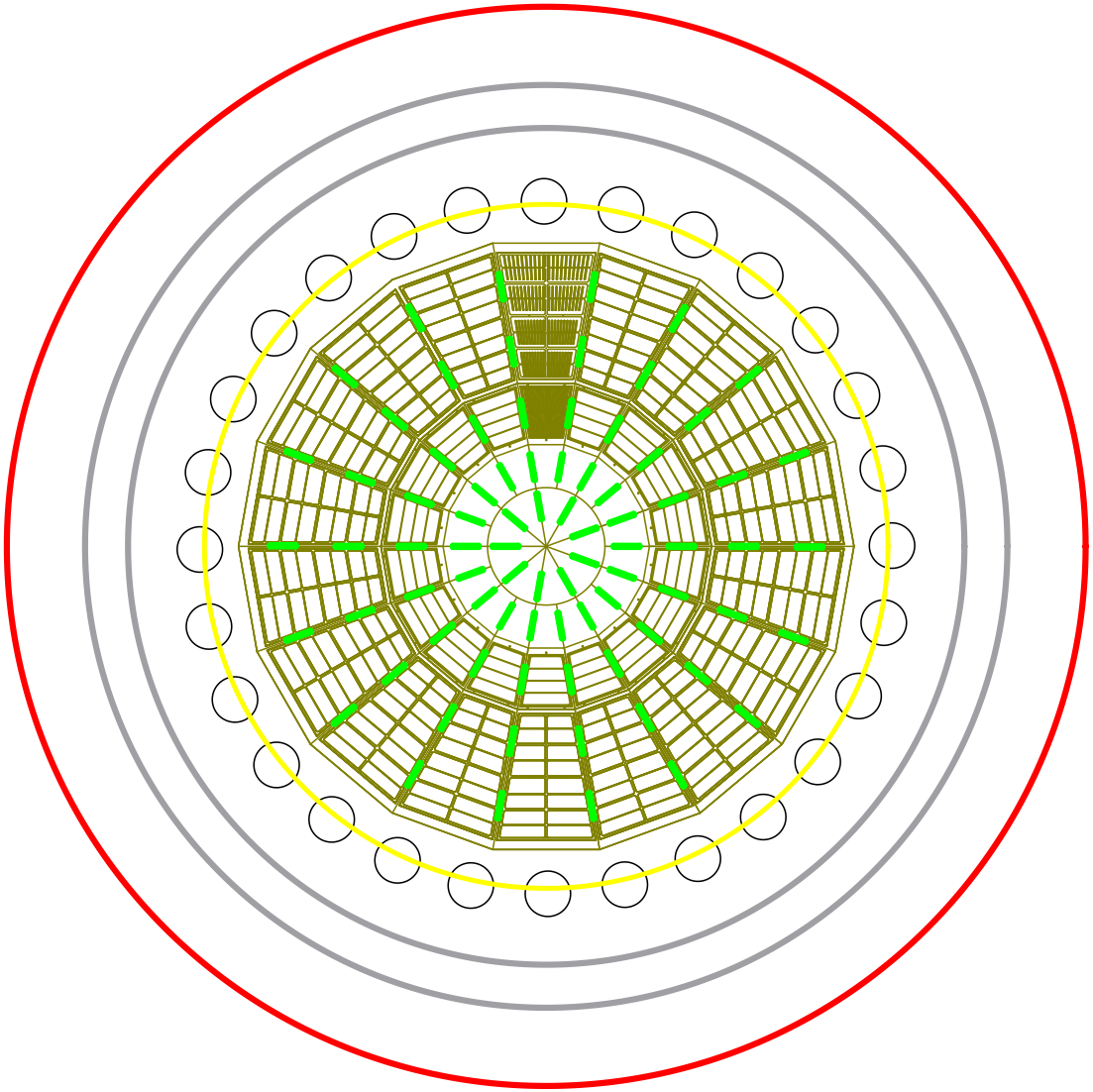
Detector geometry



Detector geometry

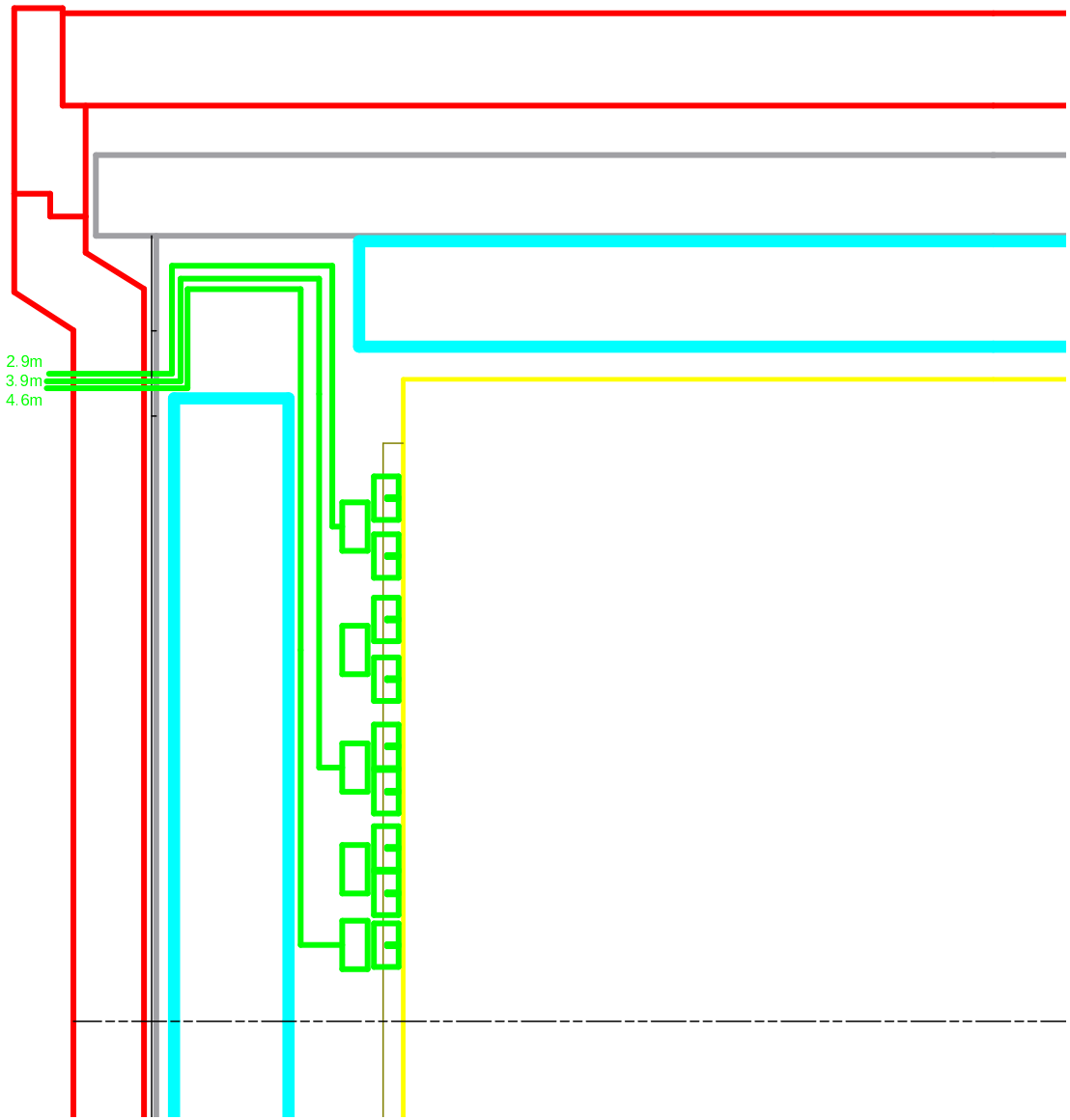


Concentrator layout



- Each slot represents one 64ch frontend (LAr
- 156 in the outer module (use 2 concentrators
- 90 in the inner module
- In this sketch: core channel density 2.3x inne density.
- 81 concentrators per end, conveniently divide into 9 feedthrough flanges.
- Use one KCU035 board outside of each f for data concentration, clock distribution and p control?

Data cables



- 2.9m/3.9m/4.6m cable length including some slack.
- GTH at 1.25Gbit/s over 15m CAT6 works fine.
- 5m mDP cable tested to 2.5Gbit.
- Would be interesting to try some better cables (but using consumer cable makes procurement easy).
- Other options: 1000Base-T1 or Coaxpress, not required for this distance but would reduce conductor count.
- We might get away with just using LVDS from normal IOs (untested).
- DB25/DB37/DB62 or NA62-style potted PCB feedthrough?
- Try to group frontend board in groups of 4-5 to reduce number of cable harnesses?

Architecture sketch