ETROC Risks

RI-ID RT-402-8-55-D
Title ETL - Schedule delay in submitting ETROC2

Summary

If a ETROC2 design takes longer than originally anticipated due to additional work, then the resultant delay in ETROC2 availability will delay module prototyping work. Delays may occur due to worse than expected performance of ETROC1, such as its timing resolution, power consumption, or radiation tolerance, or due to unexpected design difficulties of the large-size ASIC.

The dates should be adjusted.

Risk mitigation: The impact to the rest of system will be minimized as the new ETROC2 emulator will allow the system test to continue.

Labor cost: Should be adjusted. Could assume 0.5 – 1 – 1.5 FTE, 2 – 4 – 6 months

ETROC Risks

RI-ID RT-402-8-01-D
Title ETL - Additional FE ASIC prototype cycle is required

Summary

This risk can have multiple causes.
1) If the necessary performance (precision vs power consumption) is not achieved during the last prototype cycle, an additional prototype cycle may be necessary causing a delay and incurring a cost increase.
2) ASIC specification has changed due to external reasons, such as lpGBT clock distribution does not meet specifications.

This risk needs to be modified. The ETROC2 size is full size, thus the numbers should be adjusted. The starting/expiration dates should be changed

Risk mitigations: All critical design blocks have been prototyped and will be extensively tested. The system interfaces and main digital blocks will be prototyped in firmware in the ETROC2 emulator and will be tested with the backend system via the readout board. Extensive ETROC2 design verifications is in the plan.

Labor Cost: Should be 3-pt triangular: 0.75 – 1.5 – 2.0 FTE

ETROC Risks

RI-ID RT-402-8-54-D
Title ETL - Schedule delay in submitting ETROC3

Summary
If ETROC3 design takes longer than originally anticipated due to additional work, then the resultant delay in ETROC3 availability will delay module pre-production work. Delays may occur due to worse than expected performance of ETROC2, such as its timing resolution, power consumption, or radiation tolerance, or additional design work required to modify ETROC2.

Delay 2 – 4 – 6 months,
Labor Cost: 0.5 – 1.0 – 1.5 FTE

RI-ID RT-402-8-03-D
Title ETL - FE ASIC does not meet specs - needs another pre-prod run

Summary
If the preproduction Front End ASIC does not meet specifications after the masks are produced then an additional set of masks will need to be produced and additional engineering effort is required to adjust the design so that the ASIC meets specification.

The labor estimate is too low. Any change to the full size ETROC design will require extensive design verification.

Labor Cost: Should be a 3-pt triangular PDF: 0.5 – 0.75 – 1.0 FTE.

ETROC – Additional Risks

Delay of the ETROC1 testing due to the availability of the testing facilities (TID, SEU, beam tests);

Delay of the ETROC2 testing due to the availability of the testing facilities (TID, SEU, beam tests);

Delay due to unexpected technical difficulties to fully evaluate ETROC2 (such as system level issue, good example is clock distribution)

Delay due to the needed system component not available or not ready to fully test ETROC2 at system level (this has a high probability)....

Delay of ETROC2 due to the delay of bump bonding study

Unable to hire PhDs

Lost of key engineers (this is covered in the overall general risks?)
This now might have a higher probability due to COVID