Wire-Cell TPC simulation for VD update

Previous works:

- Initial Field Response simulation for 50L
- 2-view geometry ported to Wire-Cell format
- initial configuration for standalone Wire-Cell

Ref:

- Brett's talk https://indico.fnal.gov/event/47321/contributions/206217/
- Andrea's talk https://indico.fnal.gov/event/46502/contributions/206716/

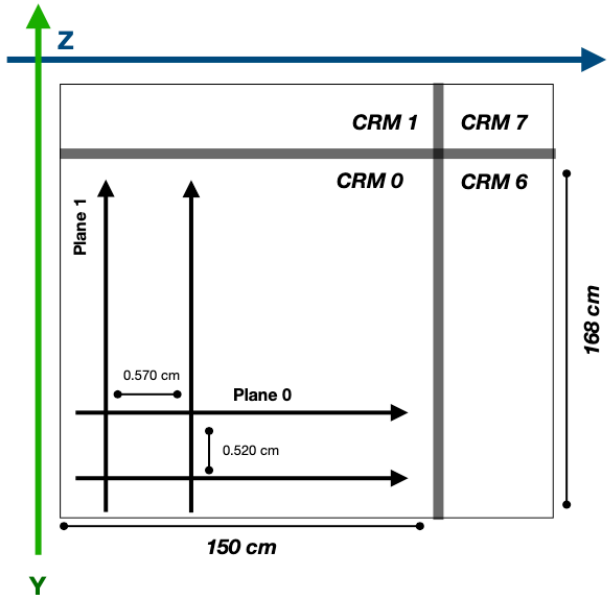
Update: LArSoft integration

- currently focusing on making the full chain work
  - more tuning/debugging/enhancing later
- status: initial integration done for sim-SP chain
  - https://github.com/HaiwangYu/wire-cell-toolkit/blob/dune-vd/cfg/pgrapher/experiment/dune-vd/

Initial check of the TPC simulation

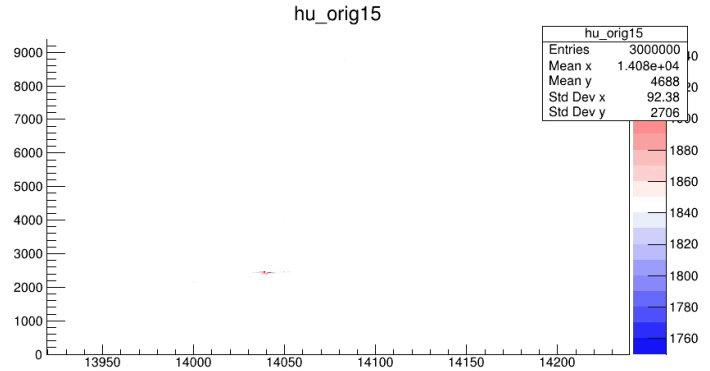
- For now, use sim::SimEnergyDeposit from dune10kt-1x2x6 (HD)
  - Will try V. Galymov's simulation for VD later.

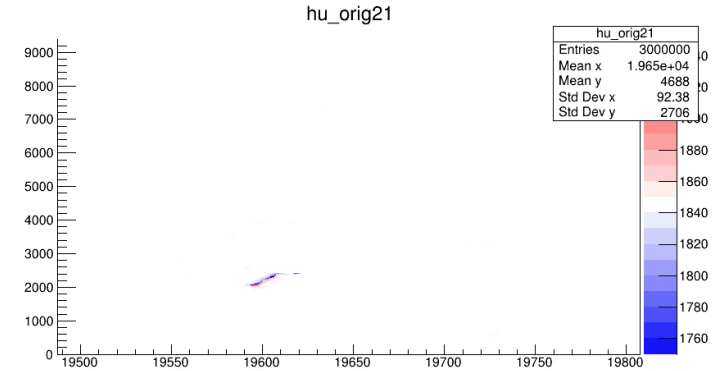
- geom: https://github.com/WireCell/wire-cell-data/blob/master/dunevd-wires-twoplanes.json.bz2
- field resp.: https://www.phy.bnl.gov/~bviren/tmp/pcbro/pcbro-response-latest.tar
- fcl: https://github.com/HaiwangYu/wire-cell-toolkit/blob/dune-vd/cfg/pgrapher/experiment/dune-vd/wcls-sim-drift-simchannel.fcl



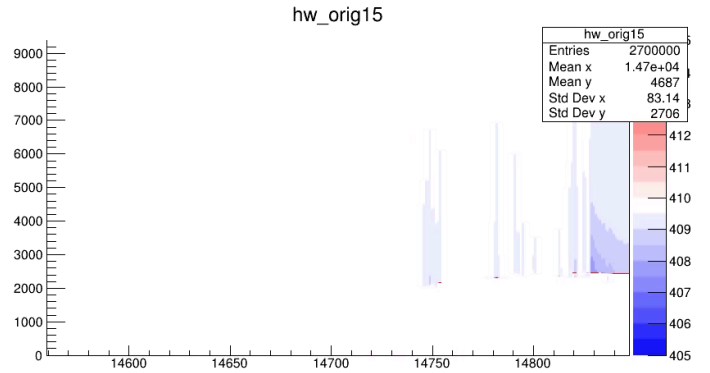
mu- simulated from the HD

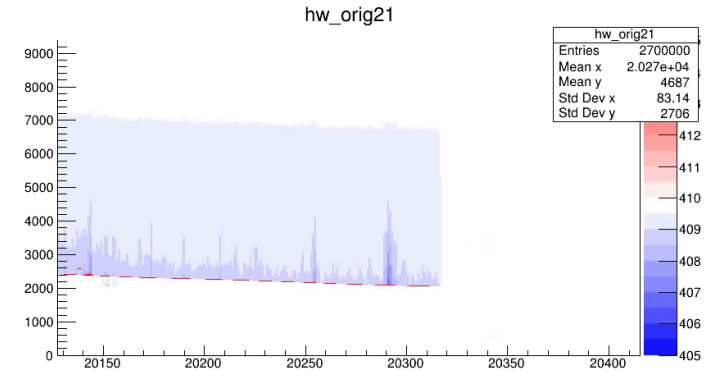
induction





collection

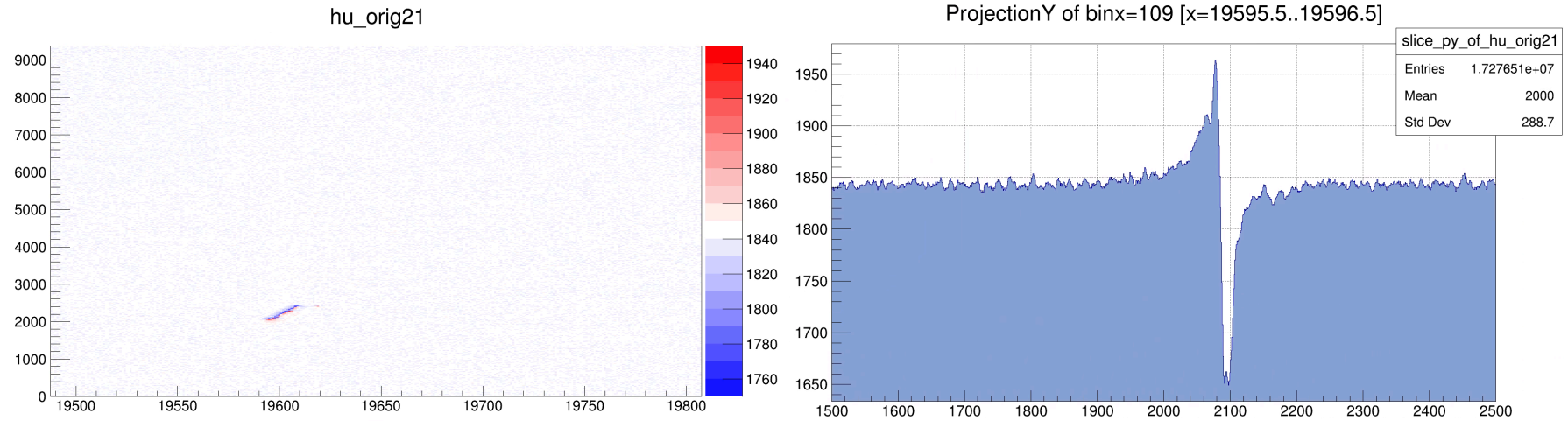




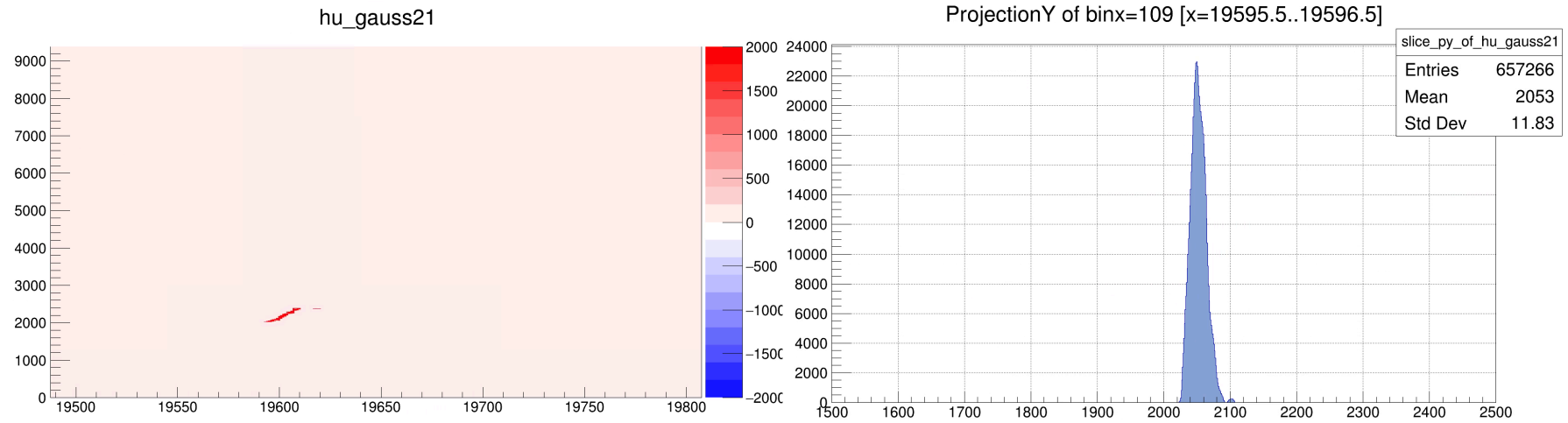
Initial check of the Signal Processing

- noise model from ProtoDUNE-SP
  - working with B. Yu on new model for VD
- filters and other tunings are also from ProtoDUNE-SP
- initial check, more tuning undergoing

sim



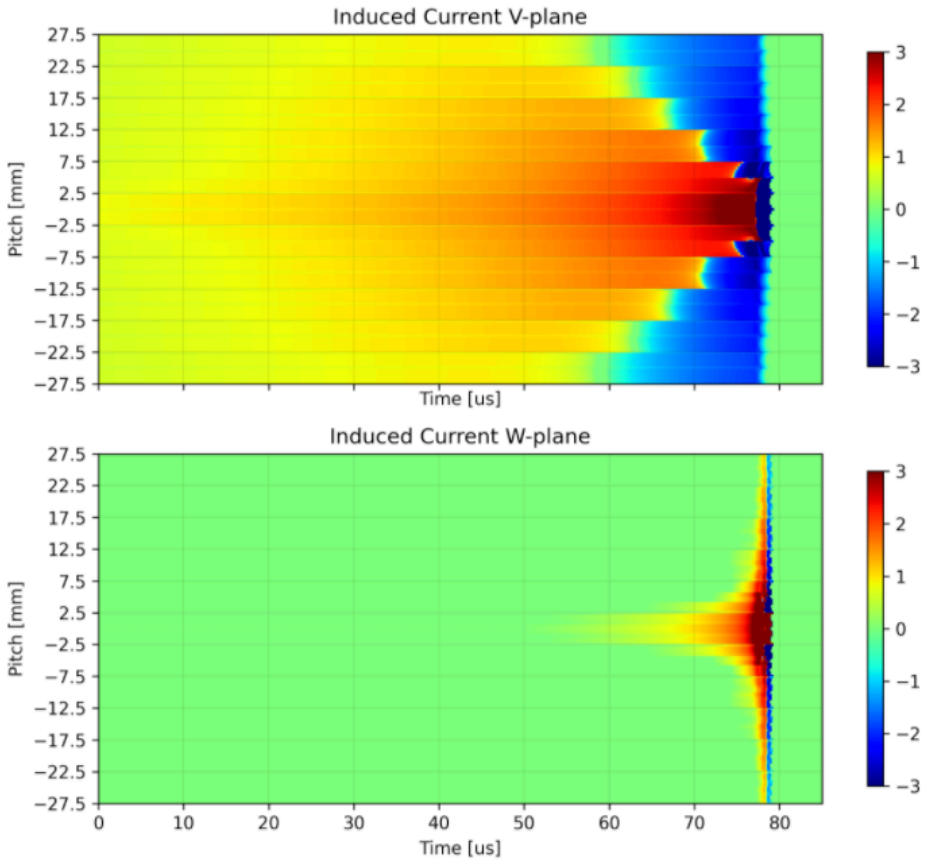
signal processing



Field Response

- Currently using the one calculated for the 50L Prototype using the “2.5D” method by Y. Li and B. Viren
  - using this as placeholder
  - more in B. Viren’s talk in last FD sim/reco meeting

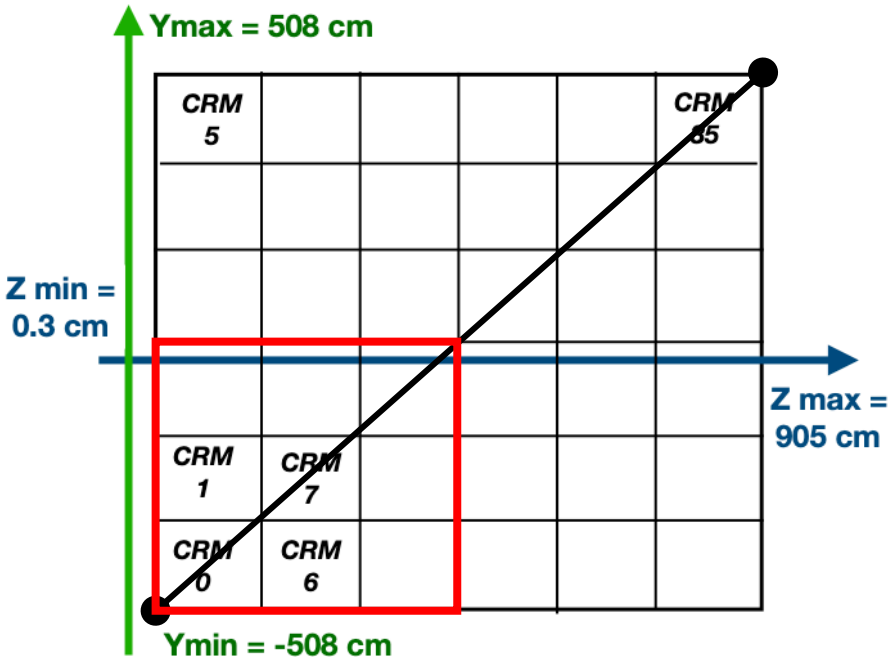
- F. Pietropaolo and B. Viren are working on new procedures and for FD

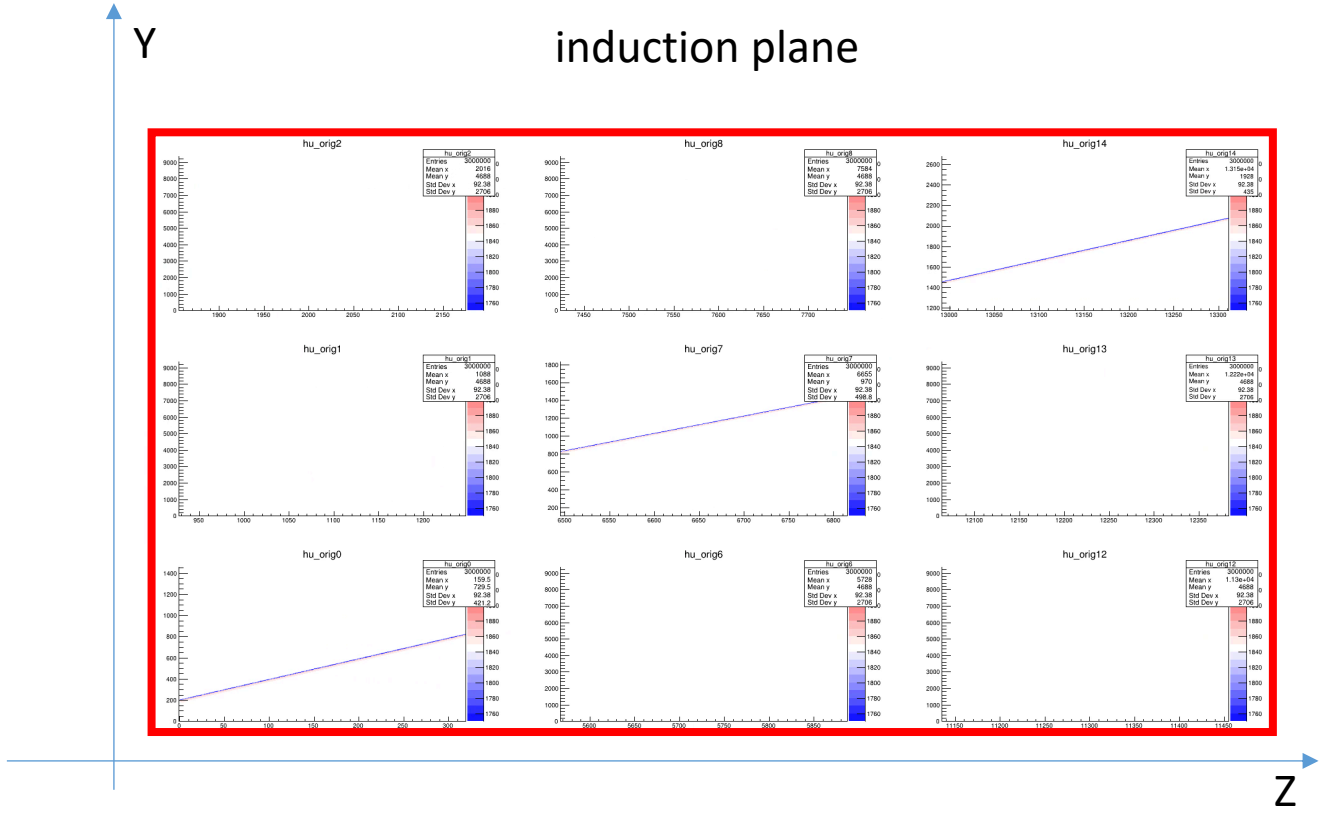


Geometry

- Currently using 2-view version ported using the gdml from V. Galymov
  - Work from A. Scarpelli

- Working on porting V. Galymov's 3-view geometry

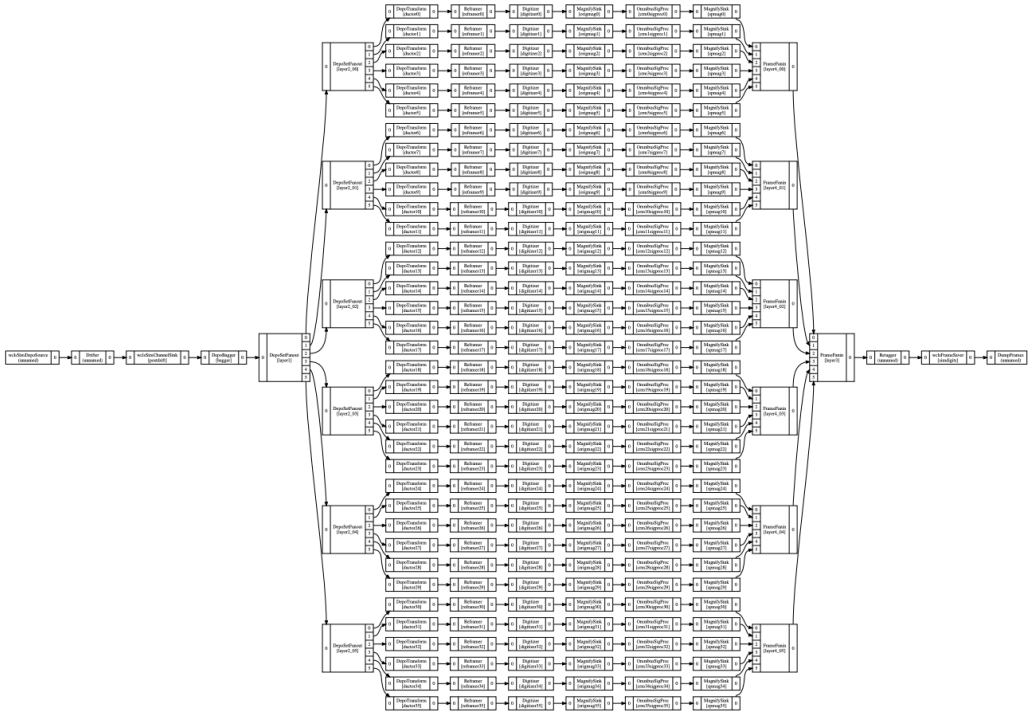




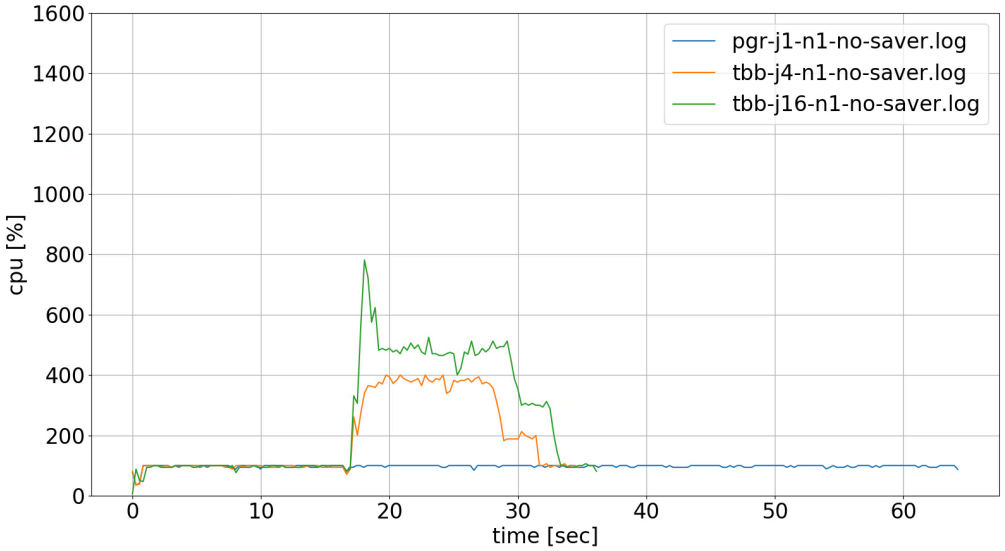
Wire-Cell Graph and Multi-threading

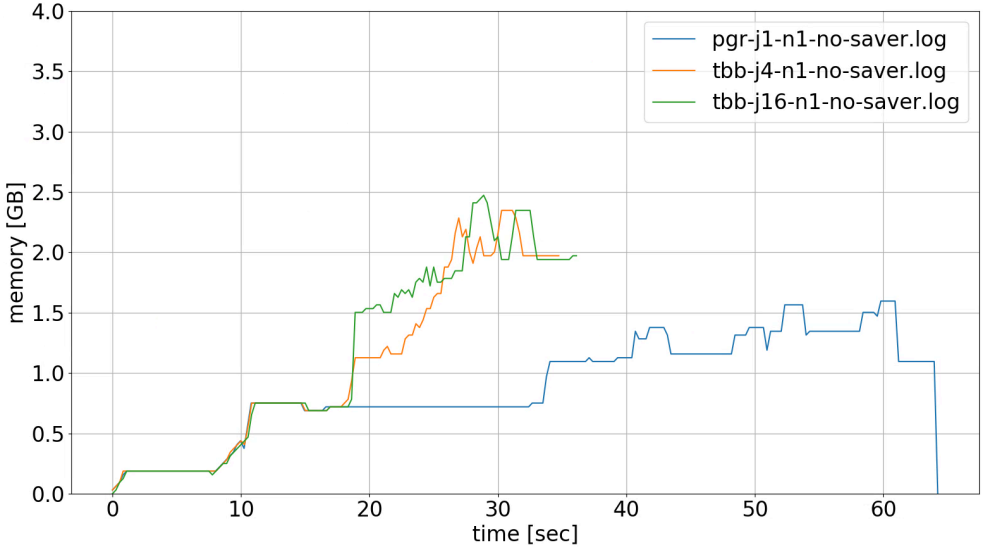
- Task level multi-threading using TBB
  - like LArSoft
  - Memory-CPU load balancing

WC Graph for FD VD simulation



ICARUS simulation





Summary

Initial integration with LArSoft done

- TPC sim + signal processing
- https://github.com/HaiwangYu/wire-cell-toolkit/tree/dune-vd/cfg/pgrapher/experiment/dune-vd

Will gradually update the placeholders:

- Field Response
- 3-view geometry
- Noise model

Validations:

- geometry
- sim::SimChannel
- raw::RawDigit

Further tunings and optimizations

DUNE 10kt 1x2x6 workspace

Work form Wenqiang Gu:

- full gen-g4-tpcsim chain working with dune v09_10_00
  - seems to have issues with latest v09_16_00, working on it
- validation from the collaboration is very welcome

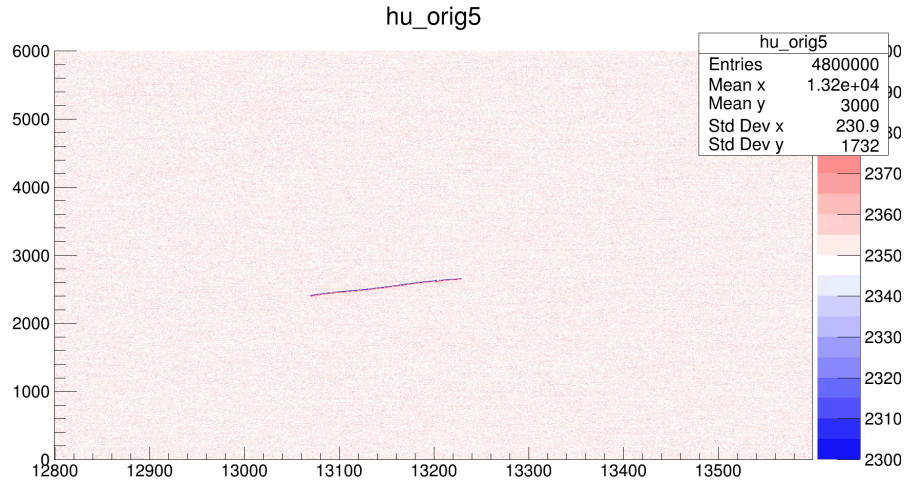
gen: prod_muminus_0.1-5.0GeV_isotropic_dune10kt_1x2x6.fcl

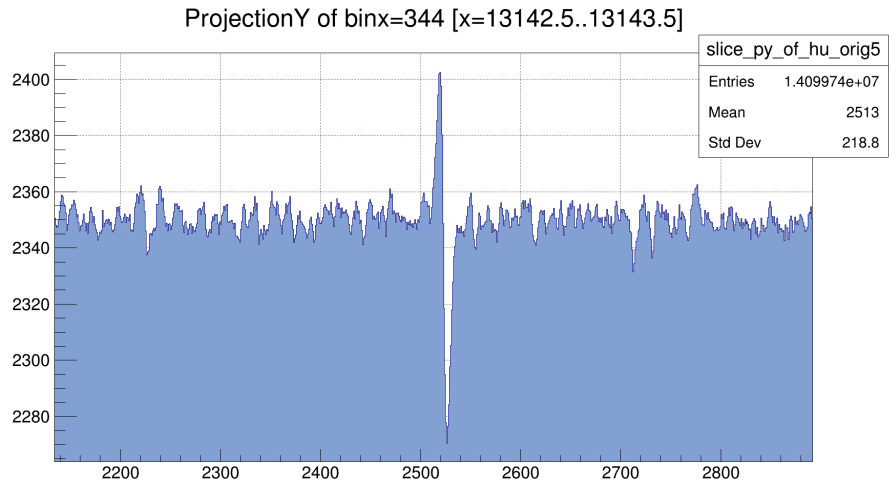
g4: supernova_g4_refactored_dune10kt_1x2x6.fcl

- /dune/app/users/wgu/larsoft/v09_12_00/srcs/dunetpc/fcl/dunefd/g4/standard_g4_refactored_dune10kt.fcl

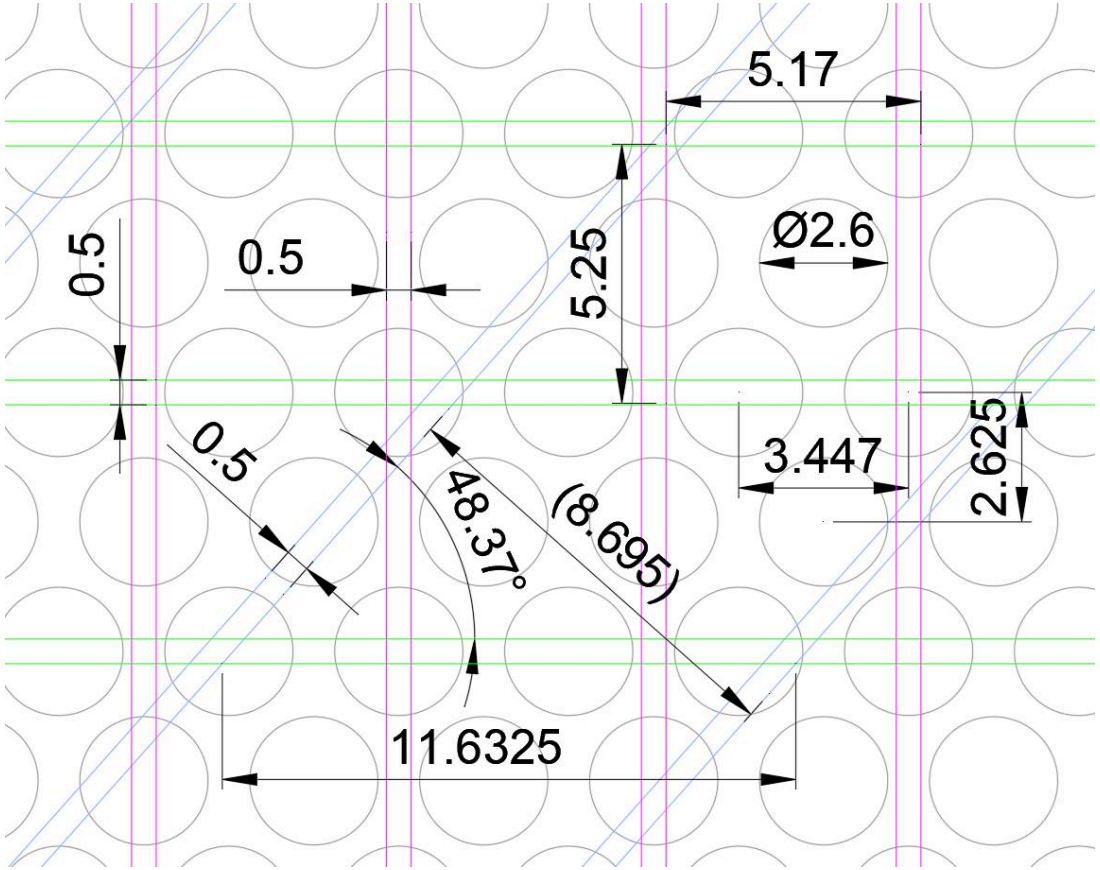
TPC Sim: opdet_multidetsim_refactored_dune10kt_1x2x6.fcl

- wire-cell-cfg/pgrapher/experiment/dune10kt-1x2x6/wcls-sim-drift-simchannel.jsonnet



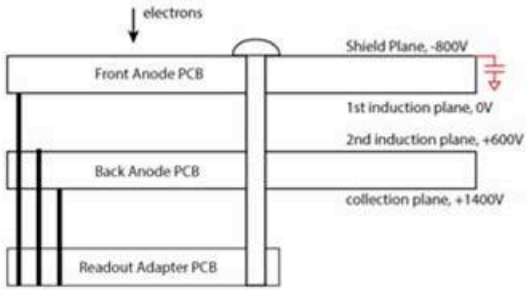


Backup

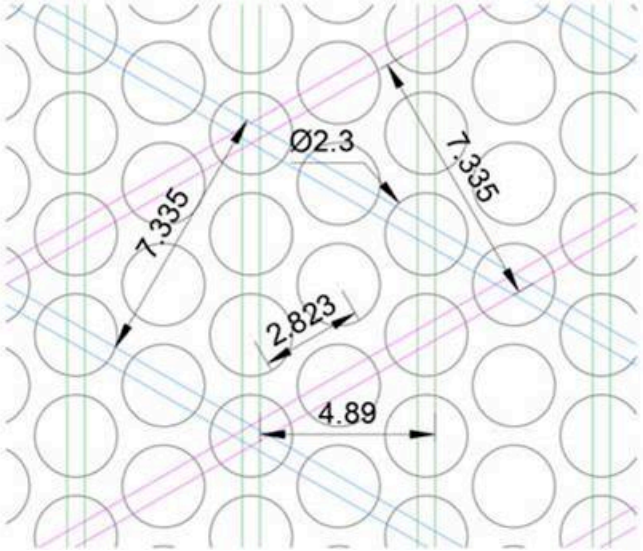

5.17
0.5
0.5
5.25
Ø2.6
0.5
48.37°
(8.695)
3.447
2.625
11.6325

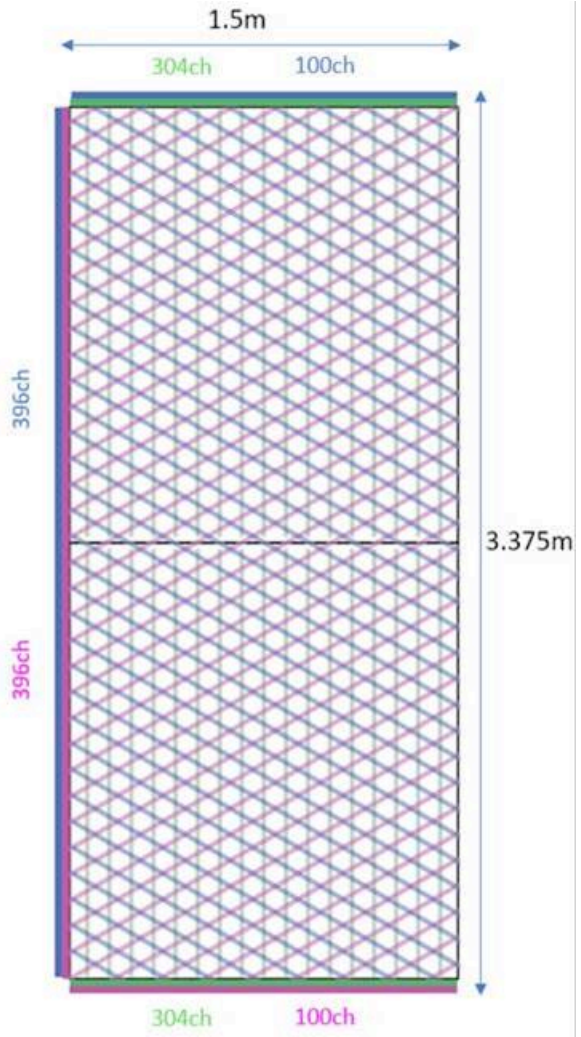
New 3V Reference Design(?)

- The layout shown here has a total channel count of 3200. The holes are 2.823mm apart on an equilateral triangular pattern. Hole size is 2.3mm (0.5mm min wall thickness).
- The collection strips are perpendicular to the beam @ 4.89mm pitch. The two induction plane strips are ±30° w.r.t. the beam @ 7.335mm pitch.
- The nominal gap width is 0.5mm, always splitting a row of holes in equal halves.
- If we implement a shield layer as the first plane facing the cathode, both anode PCBs will be perforated with the same pattern (60% open), with the holes aligned.
- The shield efficiency could be up to 95%.



3-view with a shield plane





```
================================================================================================================

!! The following modules have been misconfigured: !!

----------------------------------------------------------------------------------------------------------------


Module label: PDFastSim
module_type : PDFastSimPAR

Any parameters prefaced with '#' are optional.
Missing parameters:

 -    DoReflectedLight: <bool>

 -    IncludePropTime: <bool>

 -    UseLitePhotons: <bool>

 -    OpaqueCathode: <bool>

 -    OnlyOneCryostat: <bool>

 -    VUVHits: << delegated >>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