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U.S. DEPARTMENT OF ENERGY

LArPix-v2 channel thresholding optimization

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DUNE Pixel Readout Meeting

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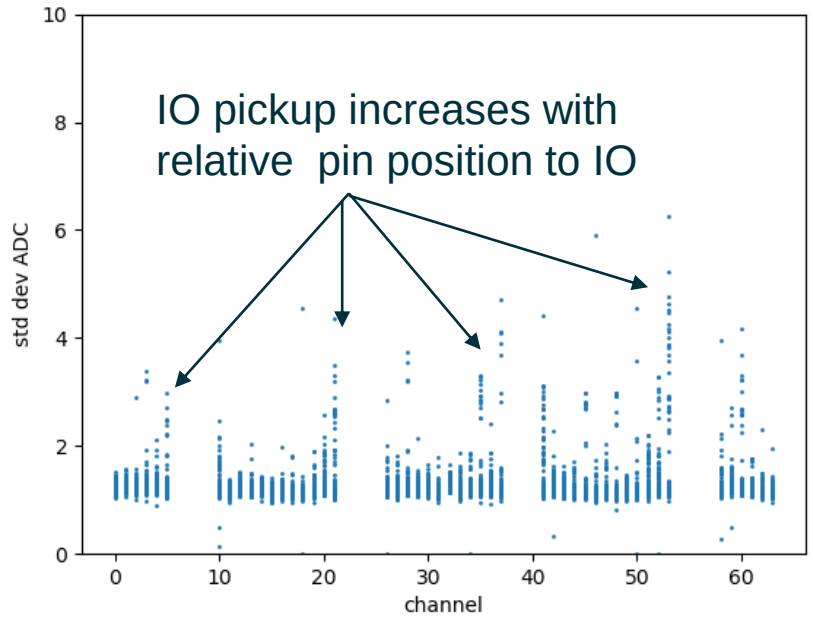
PACMAN v1rev3 final checkout

- Can drive 8 tiles if
  - Modify to bypass one of the 2 A regulators
  - Lower digital power 1.5-1.6 V (at tile)
- Noise comparable to unmodified PACMAN



8-tile warm enclosure

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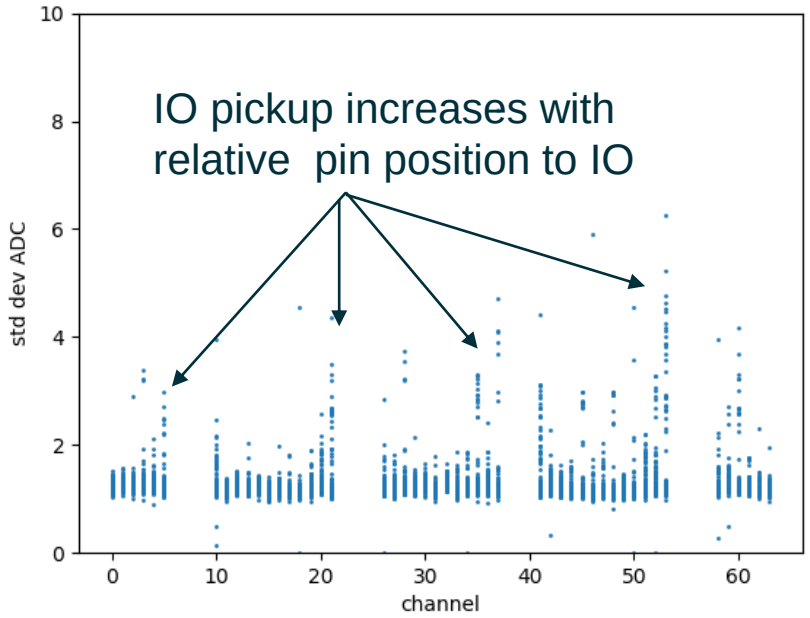
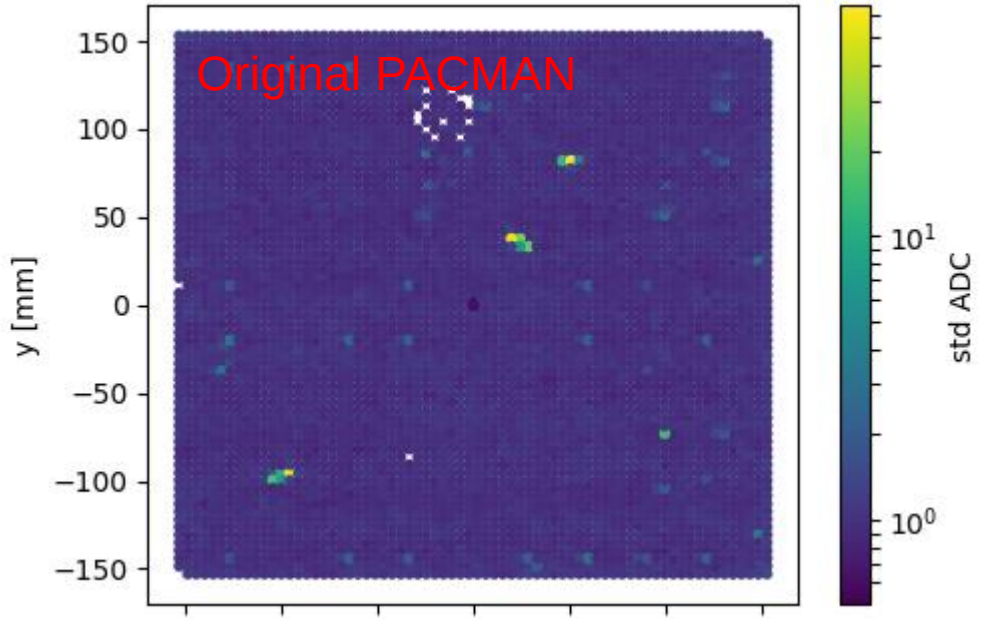
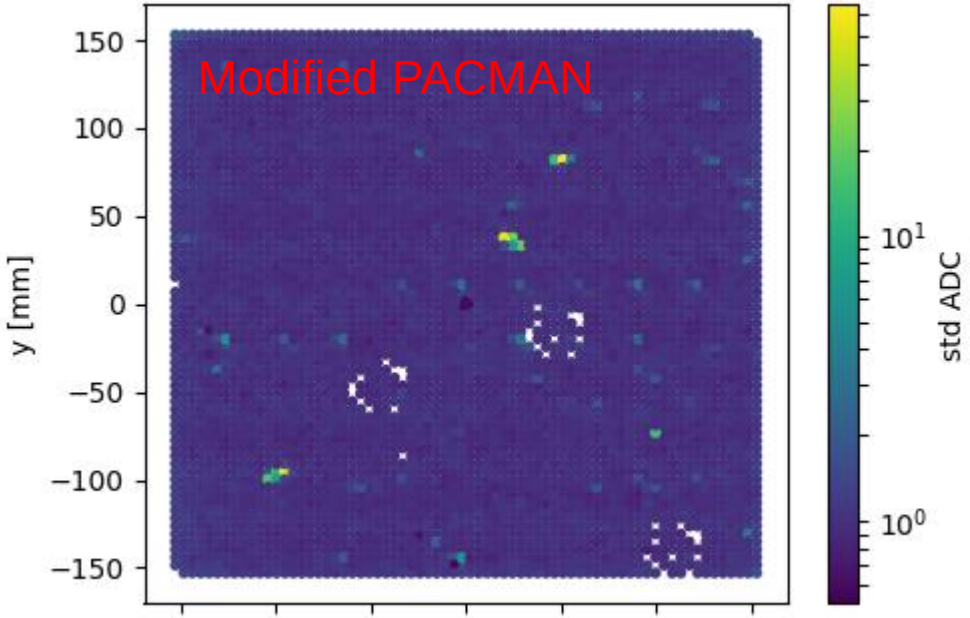
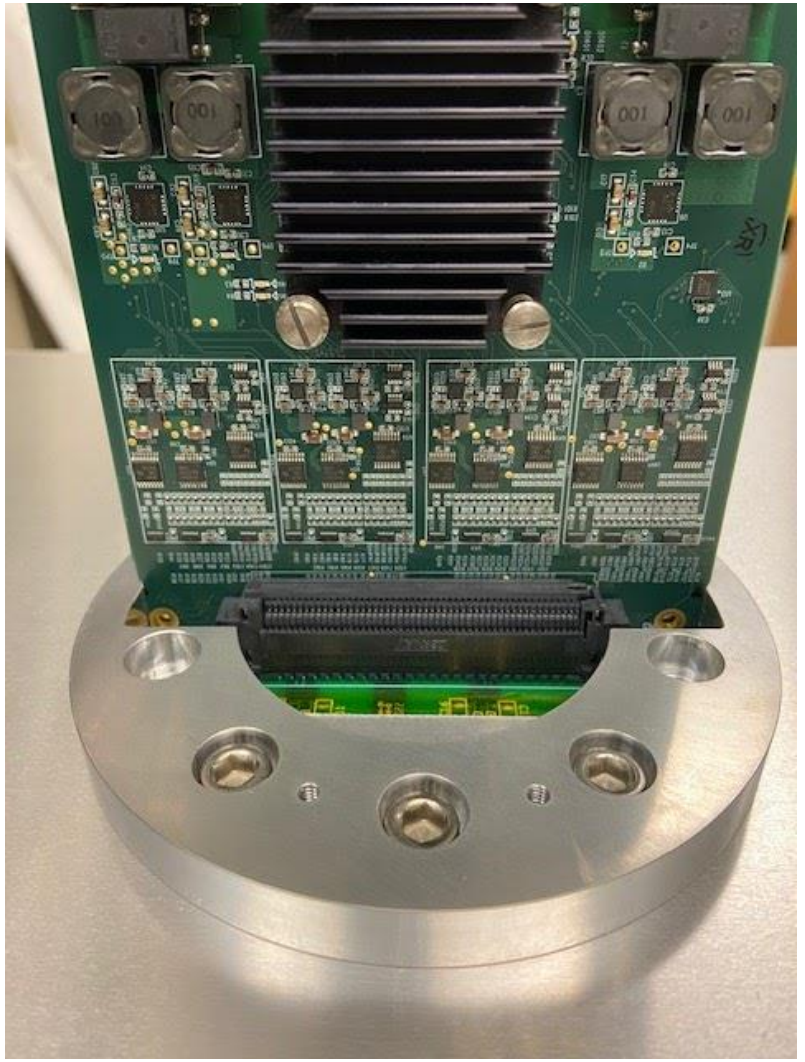






UARTs from PACMAN 300-pin connector

- 32 UARTs to serve 32 “root” ASICs on 8 tiles
- No IO on some UARTs (5-10% of UARTs)
  - Defective UARTs changes from board to board
  - ASIC networking risks
  - Identified as assembly issue → too low reflow temperature during solder
- For Module 0
  - Single board with all UARTs
  - Fixed board with 31 of 32 UARTs

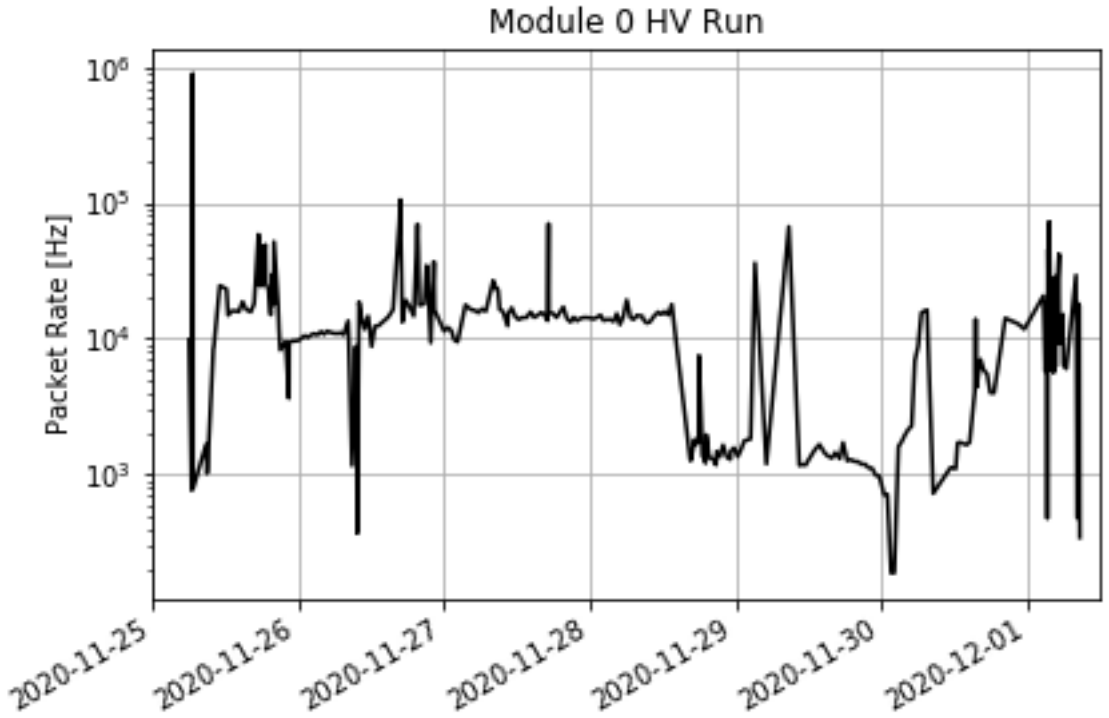


PACMAN v1rerv3
(~1.4 A current draw at supply)

LArPix-v2 channel thresholding

To date we have been using a specified self-trigger rate to configure channel thresholds

- “Walk down” global and trim thresholds until noise floor is reached then back off
- Can be a lengthy procedure to converge especially if noisy channels not identified before hand; doesn’t scale will
- Maximizes charge sensitivity at the expense of anode stability



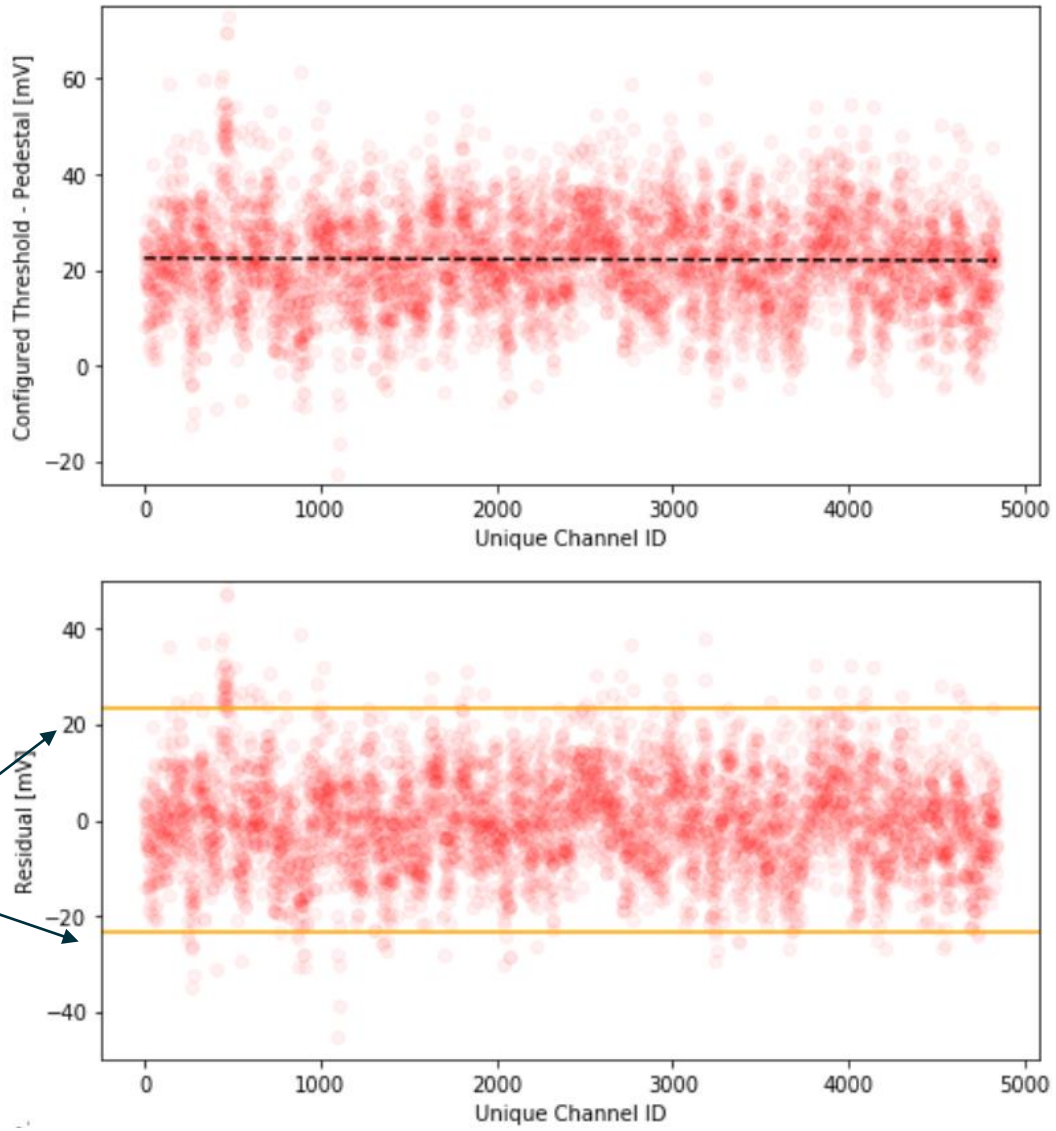
Self-triggered data also invaluable for validating system stability - identifying noise sources, grounding issues

Predictive power of pedestal

Fairly reliable to seed threshold with prediction from pedestal data

Variation of thresholds relative to pedestal fairly stable between chips

Potentially significant speedup in channel configuration process



Threshold trim

Chip-level demonstration

Seed threshold with prediction from pedestal data

Algorithm

(1) *Global_DAC = X*(Pedestal_Std. Dev.) + Pedestal_Mean*

(2) *With trim thresholds maxed out, check rate with null pulse → disable high rate channels*

(3) *Walk down trim thresholds until → if sensitivity check if at noise floor*

Thresholds set to be sensitive to ¼ MIP