Reference clock oscillators

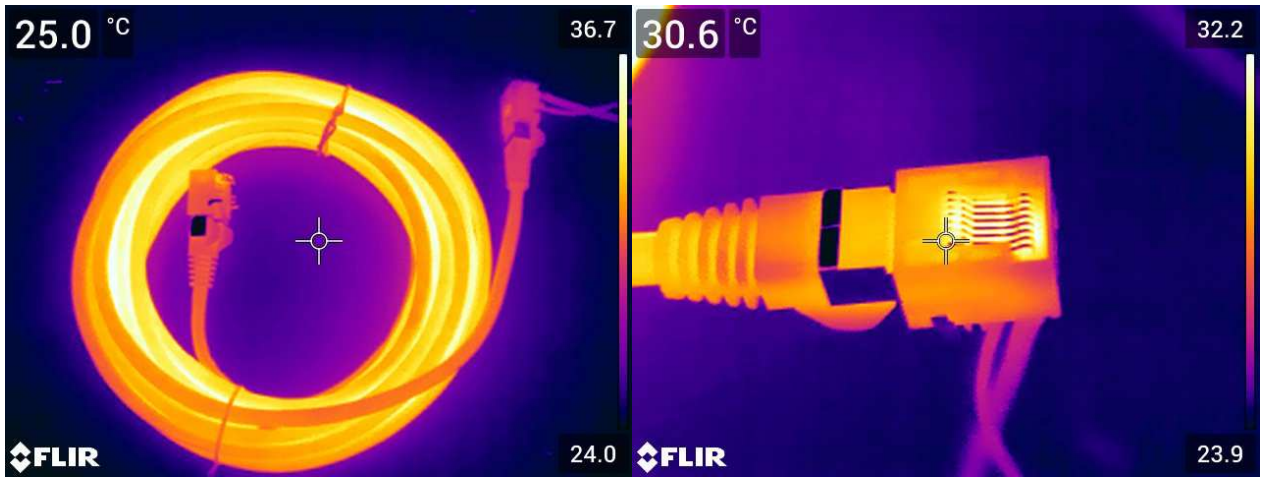
- Required for the gigabit tranceivers
- Allowable refclk vs data rate offset: +-1250pppm (at $<$6Gbit/s)
- SI500DSAB-ACF: “Quartz-free”, “MEMS-free” all silicon, 150ppm worst case.
- SI570 I2C programmable oscillator which we’ve used in various designs, permits filtering of the recovered clock if desired.
- SI511 a cheaper and lower-power I2C programmable oscillator, higher jitter (but probably fine).
- Hermetic ceramic packages: leak rate better than 5*10^{-8} atm*cm^3/s, 158cm^3 per 10y at 10Bar
- Leak rate generally assumed to scale with square root of molecule mass
  Helium 2.65 times faster than Nitrogen, Helium 2.1 times faster than Argon.

Oscillator pressure dependence

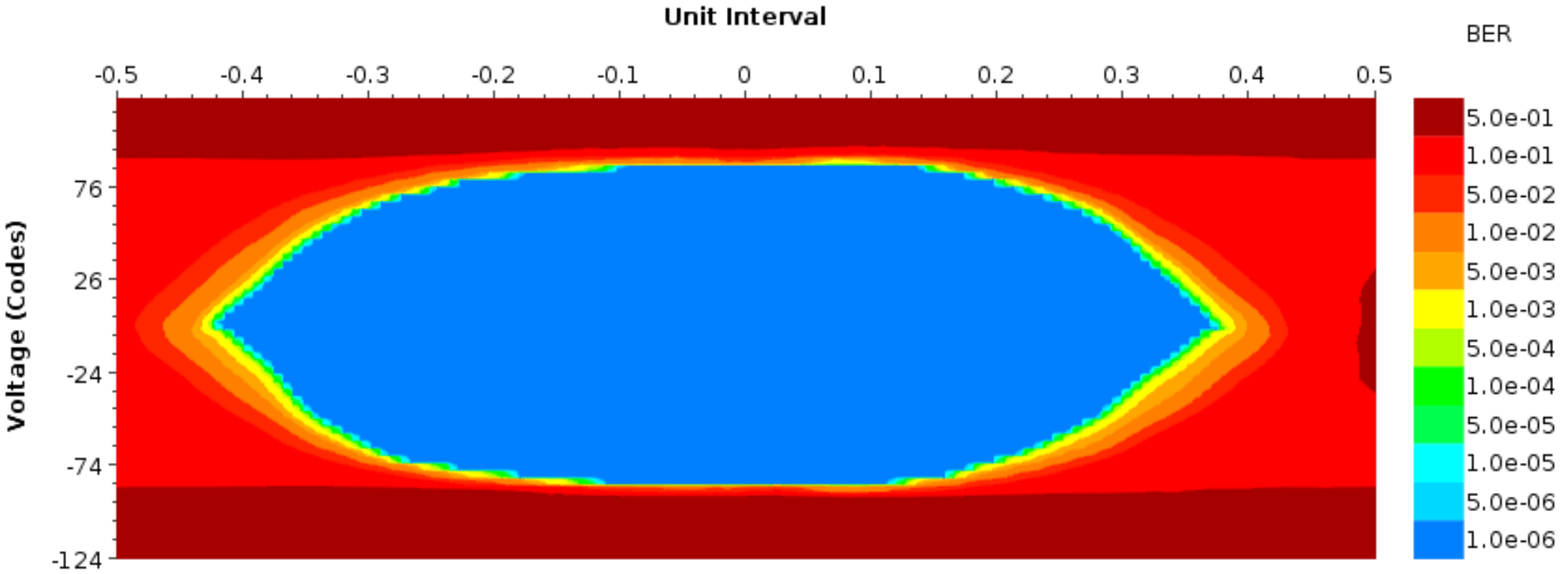
- MEMS oscillators has been shown to be quite sensitive to Helium gas.
- There is some confusion about the pressure sensitivity of crystal oscillators in the litterature:
  - Various works quote 10^{-7} per Pascal, which would be very bad.
  - However, the original work from 1966 actually states 1.35 * 10^{-9} per torr or about 10^{-6} per bar.
  - A quick test seems to more or less confirm this: When pressurizing an opened 40 MHz oscillator in air to 8 Bar a frequency shift of about 400 Hz resulted.

Phantom power over the data lines

- Power inejction/extraction requires non-saturating inductive components (can't use standard POE parts).
- Practical inductor sizes: 200-1000nH (balance between LF attenuation and HF dispersion due to resonance).
- Some further experimentation will be required to fine tune.
- If Ethernet cables are used all 4 pairs of an ethernet cable is used (enables redundant data link, reduces current per wire)
- At least 1 A per wire seems OK in practice.
- For an estimated 20W per board 5V power would in principle be possible.
  However, higher is probably preferable to reduce losses (trade-off with DC-DC efficiency).

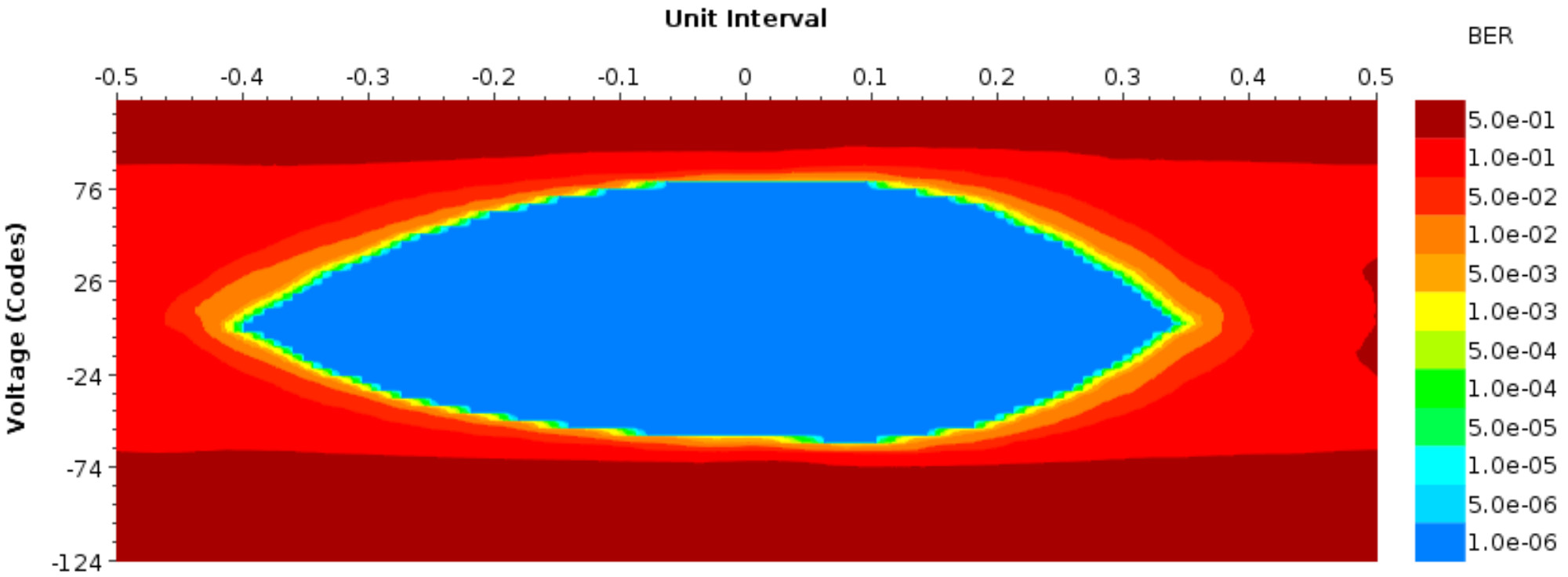


1.25G over 7m CAT6A



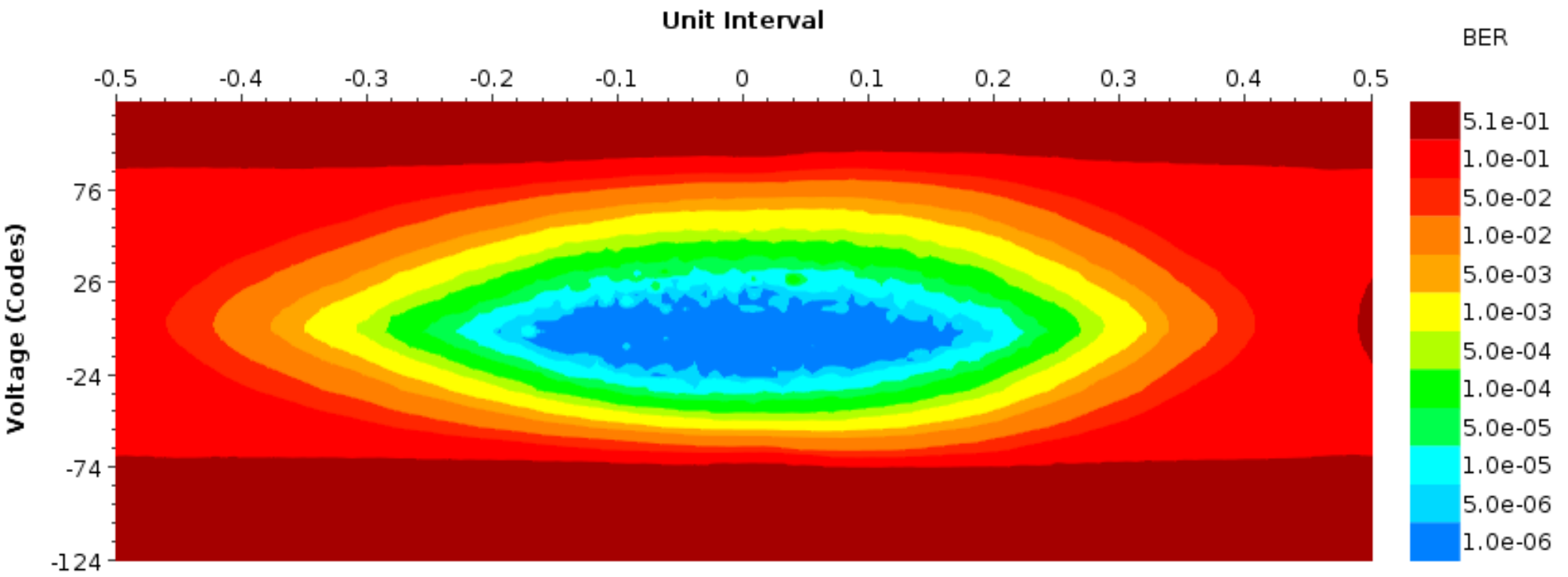
PRBS7

1.25G over 7m CAT6A



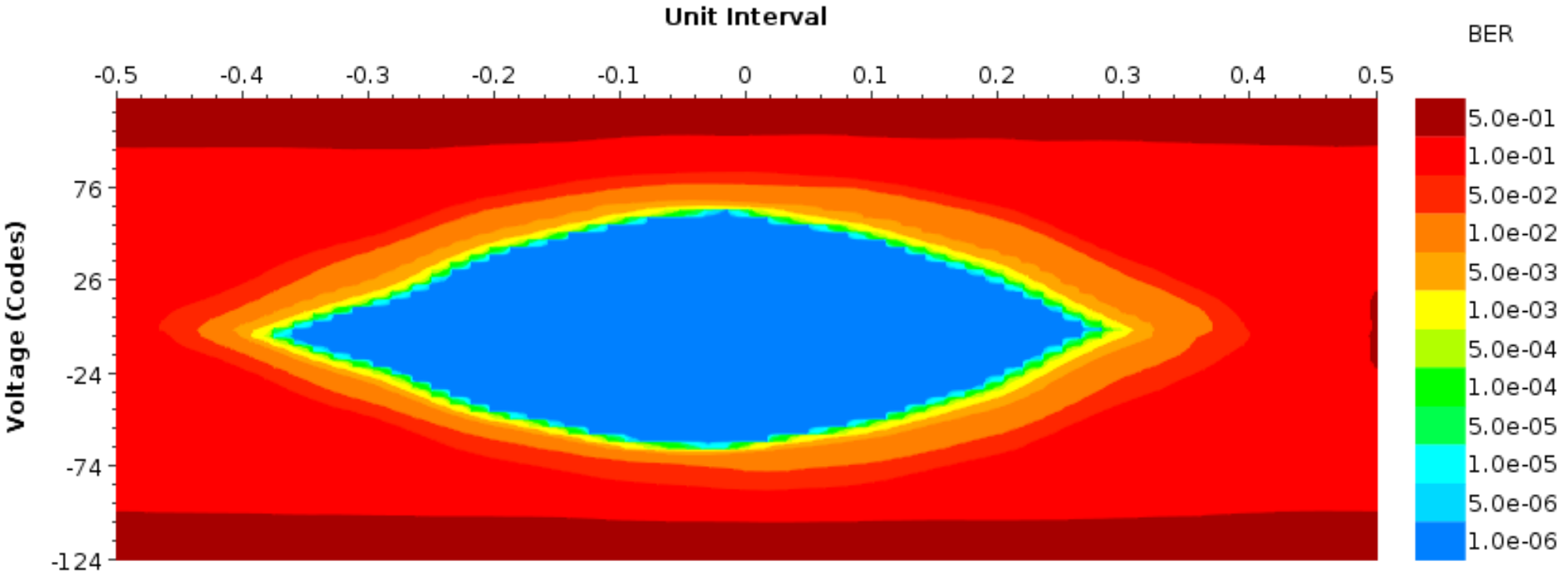
PBRS7, with 2x2x400nH inductors for power injection/extraction

1.25G over 7m CAT6A

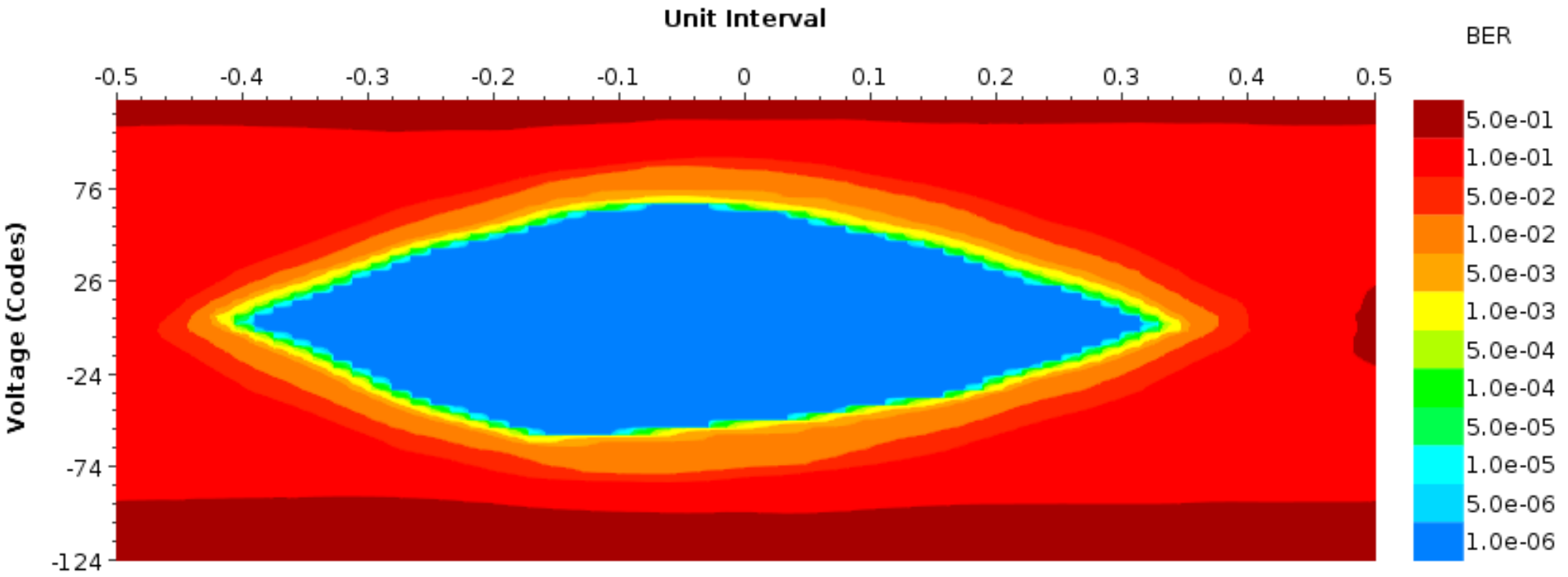


PBRS31, with 2x2x400nH inductors for power injection/extraction

2.5G over 7m CAT6A

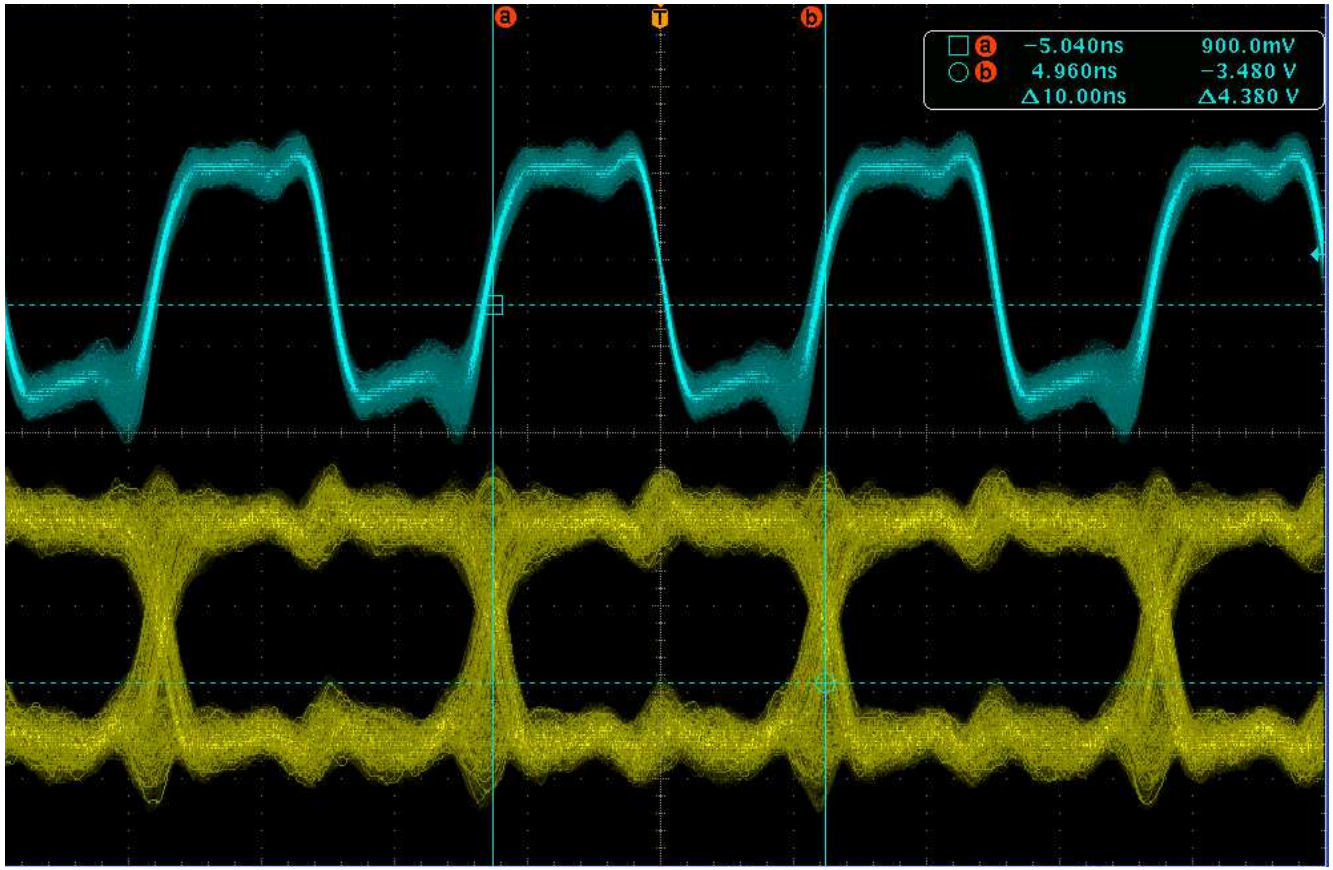


2.5G over 7m CAT6A



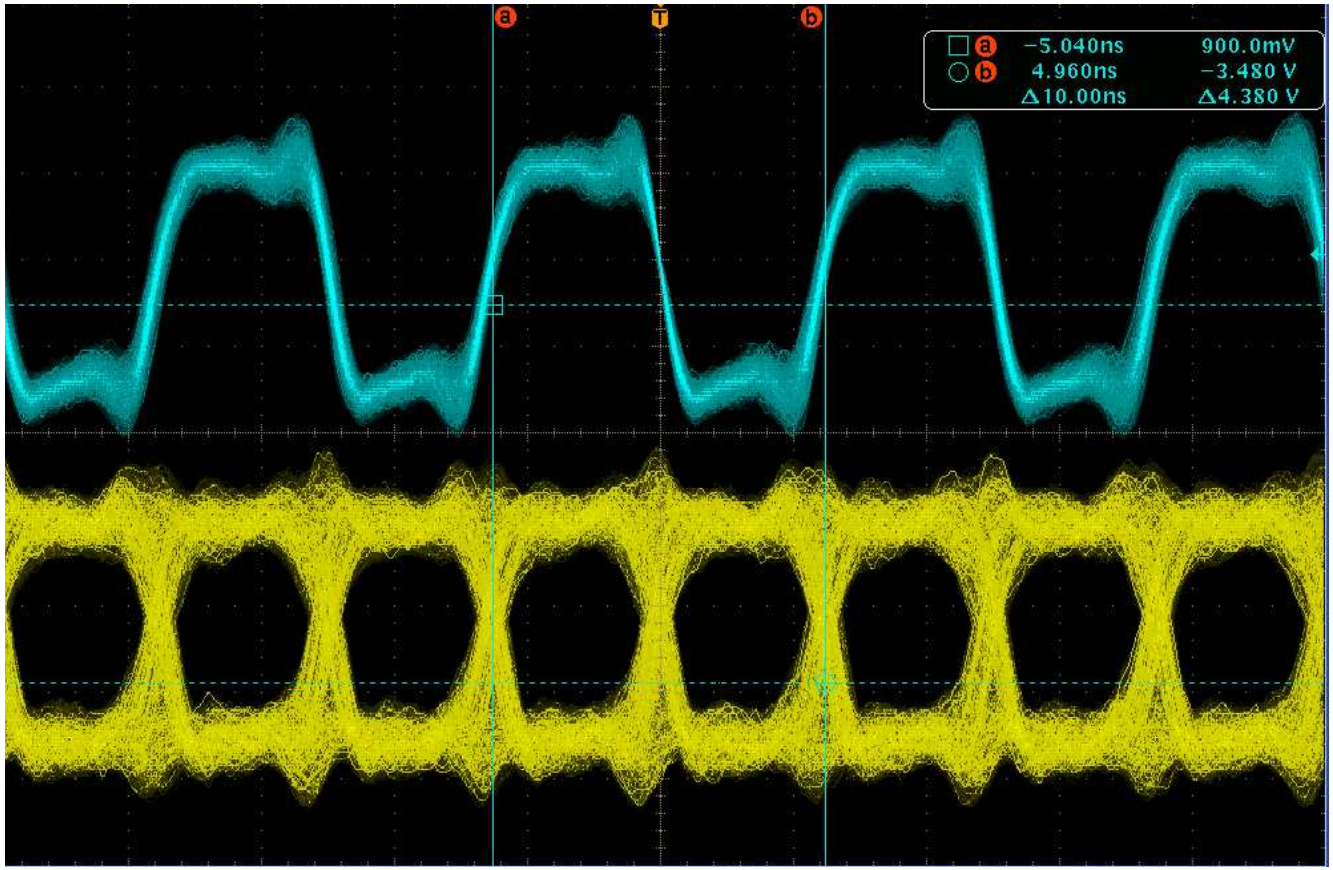
PBRS7, with 2x2x400nH inductors for power injection/extraction

CMOS data over ribbon cable to Larpix



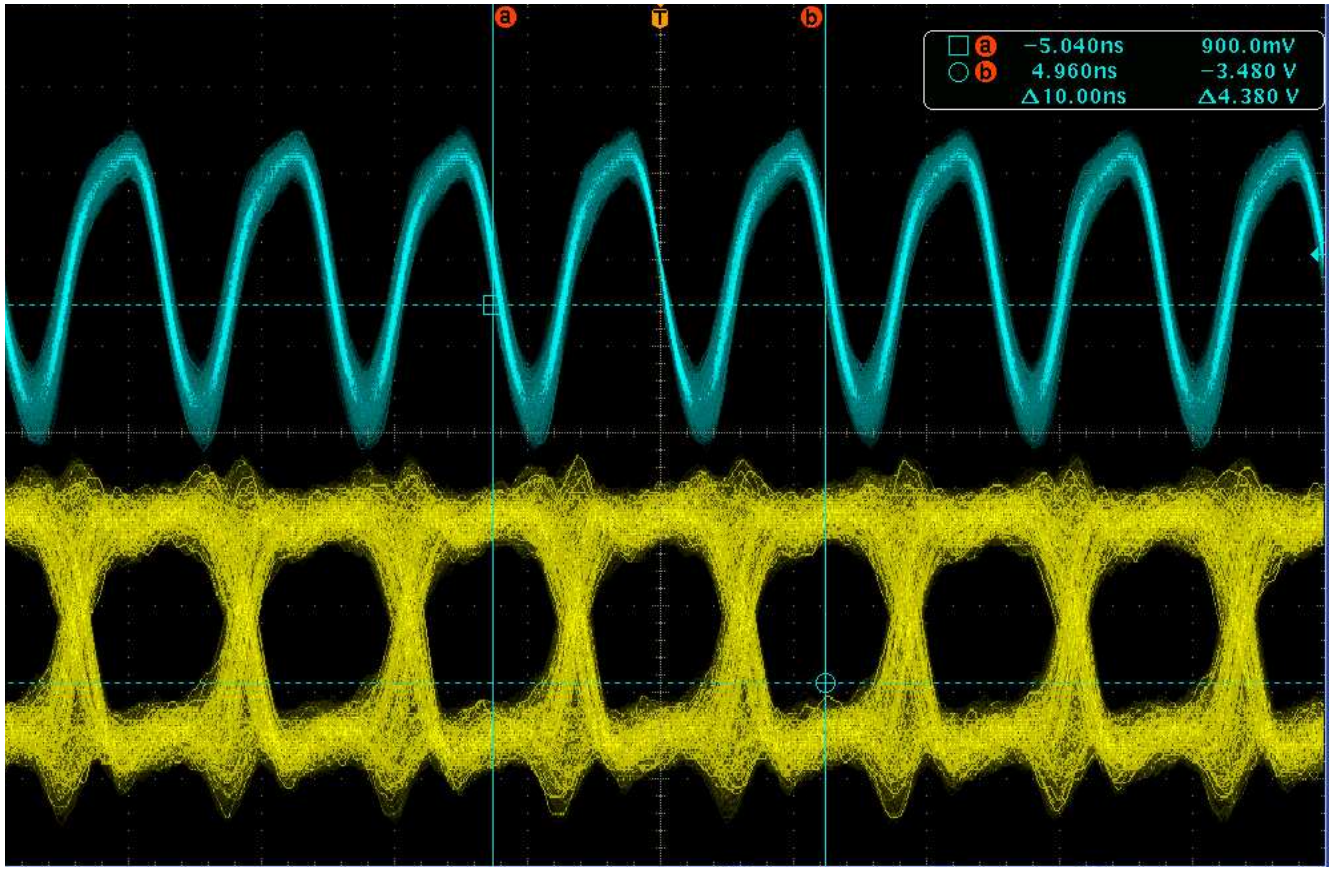
1m, 0.05" pitch, 100MHz clock, 100MHz data.

CMOS data over ribbon cable to Larpix



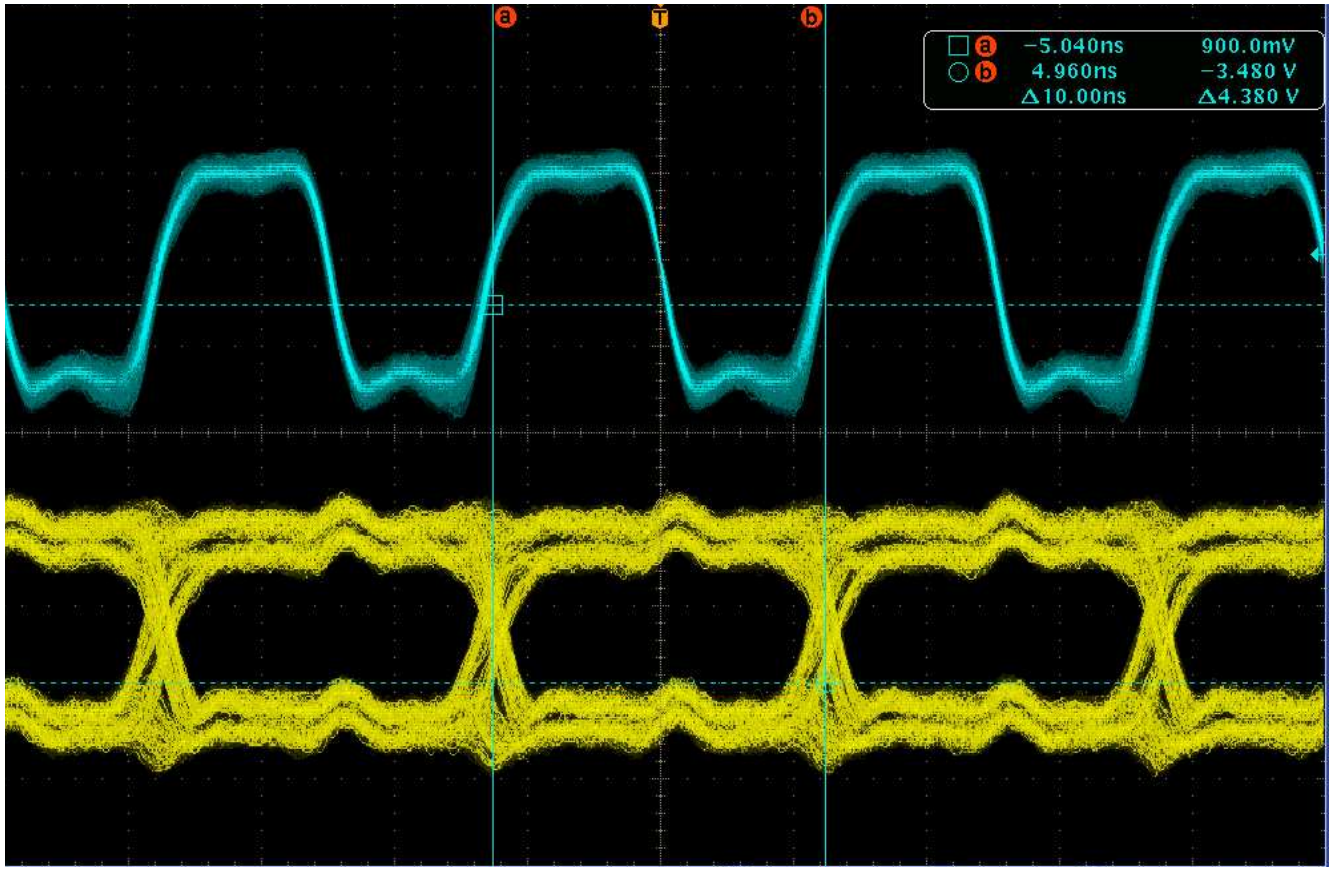
1m, 0.05" pitch, 100MHz clock, 200MHz data.

CMOS data over ribbon cable to Larpix



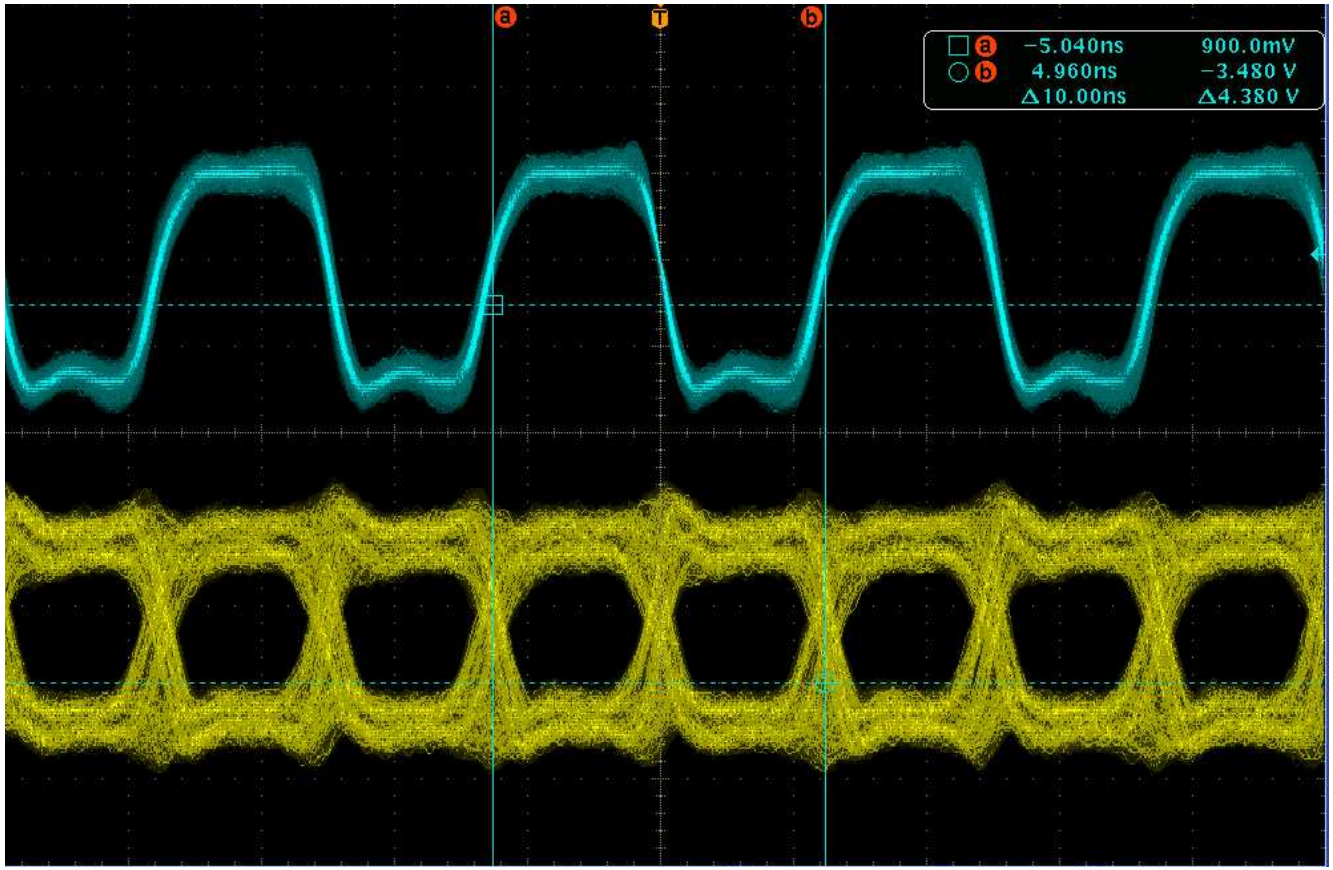
1m, 0.05" pitch, 200MHz clock, 200MHz data.

CMOS data over ribbon cable to Larpix



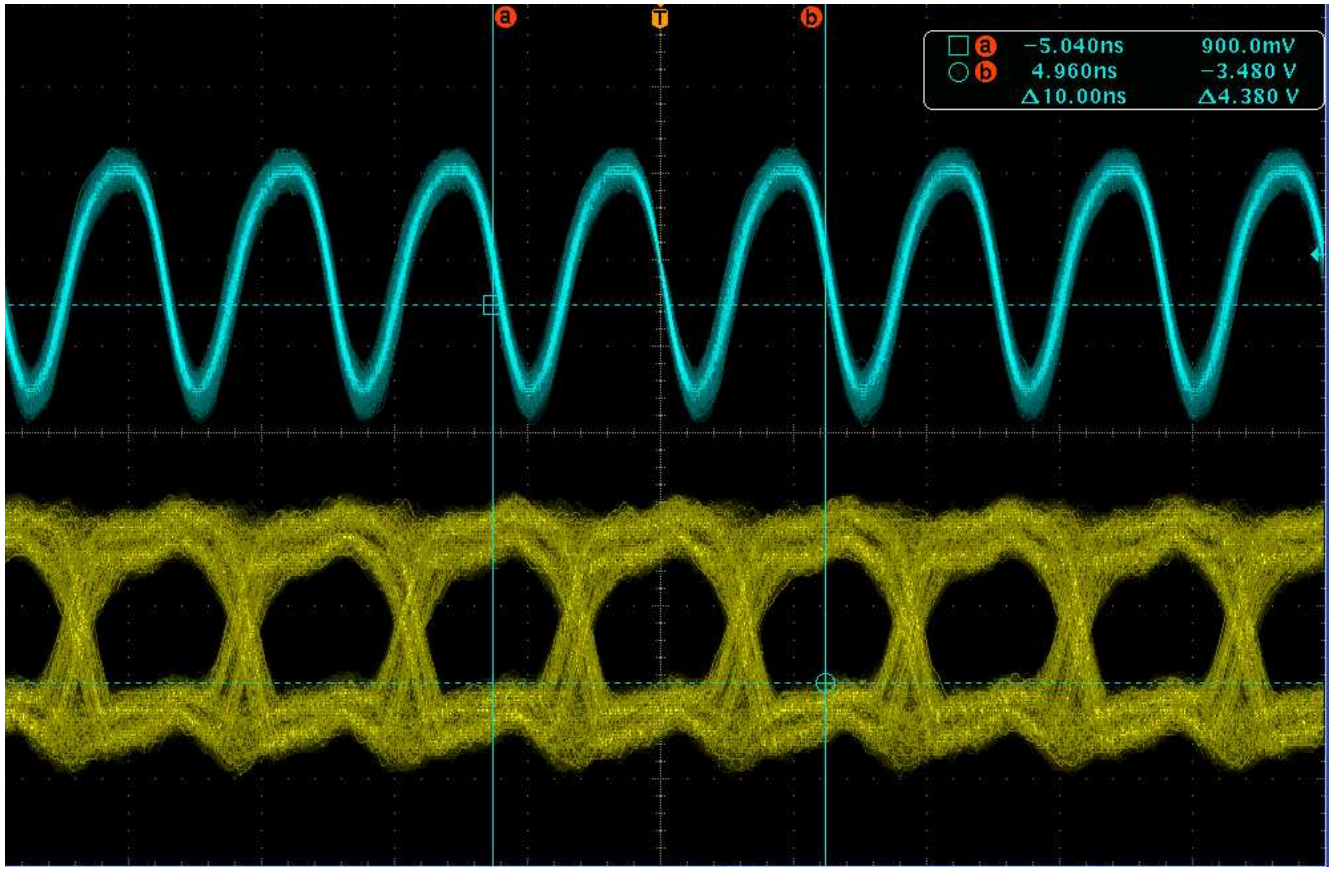
1m, 0.025" pitch, 100MHz clock, 100MHz data.

CMOS data over ribbon cable to Larpix



1m, 0.025" pitch, 100MHz clock, 200MHz data.

CMOS data over ribbon cable to Larpix



1m, 0.025" pitch, 200MHz clock, 200MHz data.

Reconfiguration over high speed links

- QSPI flash for firmware storage assumed.
- Kintex Ultrascale (probably most other modern families as well) support initiating firmware reload from firmware, with programmable start address
- Allows a “Golden” firmware to be stored at the start of the memory (optionally write-protected), and new images to be stored later in the image.
- Should a “new” firmware fail the power can simply be cycled to revert to the good image.
- Also possible to use a watchdog timer to trigger reverting to known good firmware.