VD PD CE - Meeting Mar. 3, 2021

- VD PD CE R&D effort Plan/Milestones & Resources(at FNAL and BNL) (in preparation) - *Ryan*
- Progress w/ PoF for CE - *Bill*
- SiPM Passive Ganging - *Dave*
- Progress w/ Digital Opto Transmitter tests - *Alan*
- Plans for Analog Opto Transmitter test - *Sabrina/Jaime*
- Progress w/ ADC selection and plans for tests at FNAL - *Gustavo*
- Plans for CE tests at BNL - *Hucheng*

If time allows:

- Power Budget (current estimates) - *Bill-Ryan*
- VD PhDet Requirements and Specs (in preparation) - *Flavio*

DoE is moving towards a plan for the US that puts a substantial part of the “cathode” mounting scheme in DUNE-US as the baseline plan.

This gives even more impetus towards executing the R&D phase productively

Consistent resources have been made available starting from February for the rest of current FY

Activity				Milestones/Deliverables	
Site	System	Subsystem or Task	Sub-SubSystem	Feb-May	June-Sept
FNAL	VD Photon Detector				
		xARAPUCA detector			
Mi-Bicocca UNICAMP CSU FNAL			- SiPMs - DichroicFilter - WLS plates - Mechanical Frame	Complete design optimization for xARAPUCA Tiles for Vertical Drift PDS - in collaboration with International and other US groups	Complete fabrication of TWO xARAPUCA Tiles (one 2-sided and one 1-sided) for Cold Box test at CERN - in collaboration with International and other US groups Deliver units to CERN
		PoF Power Transmission			
FNAL CERN			- LaserTransmitter - Fibre - (Cold) Receiver	Complete fabrication of two 60W PoF units (driver, receiver, fiber, feedthrough, regulator). Test at FNAL.	Deliver units to CERN and complete testing in 50L test facility. Prepare for Cold Box test.
		Cold Electronics			
FNAL UCSB BNL			- SiPM Passive Ganging (hybrid config.)	Complete design for SiPM passive ganging circuit at FNAL	Deliver passive ganging PCB’s with SiPMs surface mounted for TWO xARAPUCA Tiles - in collaboration with International and other US groups
Mi-Bicocca …			- Cold Active Sum - Amplif./Shaping		Integrate SiPM Cold Active Sum&Analog FE stage (delivered by other International groups) into CE layout
FNAL BNL			- Digital Conversion (Cold ADC)	Complete Cold ADC selection, test (demonstration of operation at LAr T)	Integrate Cold ADC stage into CE layout, start longevity validation test
FNAL BNL			- Cold Aggregator (FPGA)	Complete Cold Aggregator (FPGA) selection, test, validation	Integrate Cold FPGA stage into CE layout
			- External Clock Transmission		Integrate Clock and FPGA programming signal into CE layout
		Electro-Opto/RF Signal Transmission			
FNAL			- Cold Digital Optical Transceiver	Cold Fiber transmitter (Data Link) Search, Selection, bench Test in cold and characterization	Cold Fiber transmitter Validation Integrate Cold Fiber transmitter into CE layout
APC-Paris Mi-Bicocca (DS collab) FNAL			- Cold Analog Optical Transceiver		
			- Cold Digital RF Transceiver	Cold RF/WiFi transmitter Search, bench Test in cold and characterization (alternative option to Cold Fiber transmitter)	Cold RF/WiFi transmitter Validation (alternative to Fiber transmitter)
		Integrated CE Board Layout			
FNAL …			- Integrated CE Board	Design an integrated CE layout (Analog+Digital+Data Aggregation+Data Transmission) with PoF Supply and External Clock communication for the r/o of VD xARAPUCA Tile detectors	Deliver complete CE layout for TWO xARAPUCA Tiles including SiPM Active Sum&Analog FE stage from Int.l groups
FNAL		Resources and Schedule Management			
				electrical systems engineering coordination and management, liaison with DoE DUNE Project	electrical systems engineering coordination and management, liaison with DoE DUNE Project