SiPM board for PoF read out and power

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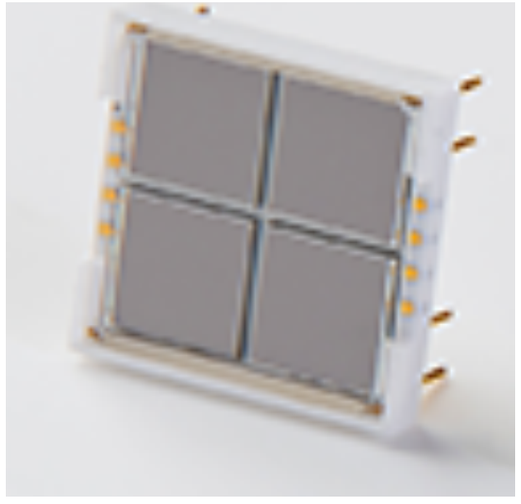
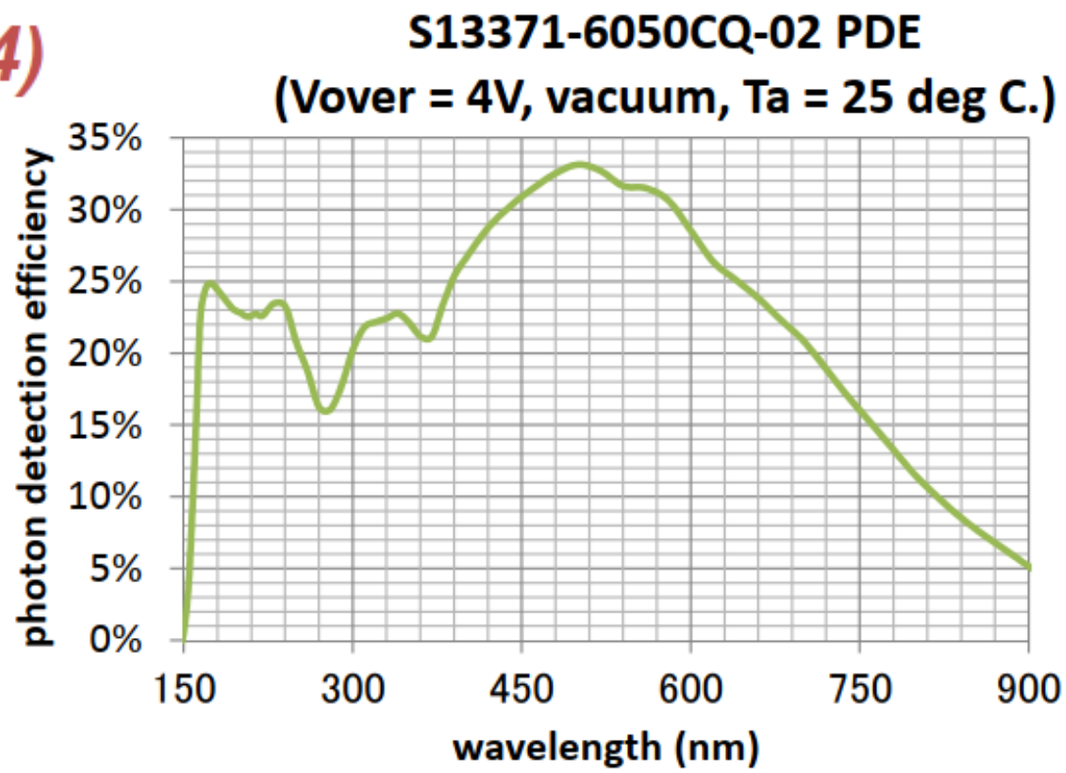
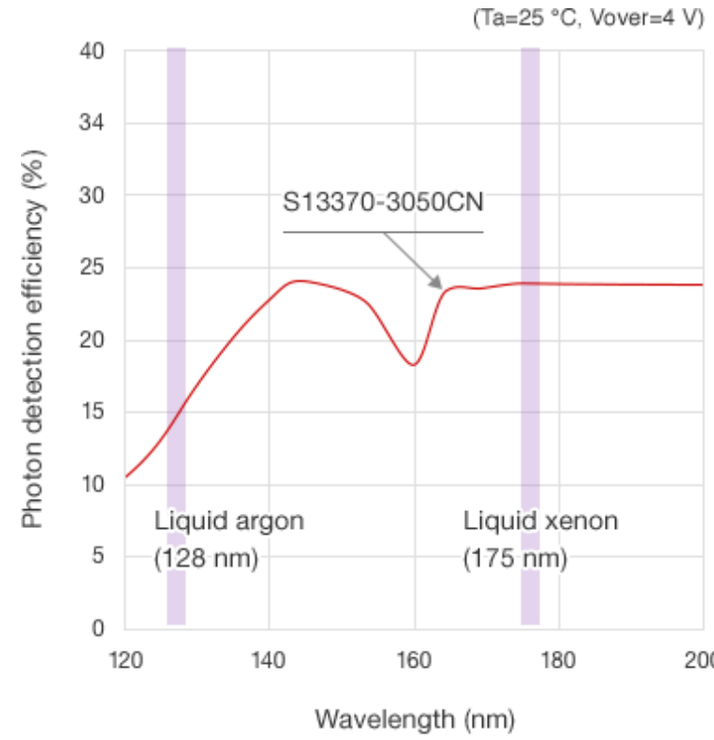
SiPMs for PoF tests @50L Cryostat, Bldg182, CERN

VUV-MPPC (VUV4)







An array of 2 x 2 of 6 x 6 mm² SiPMs Total area: 144 mm2

PDE ~15% @128 nm @ ~25% @LXe and ~30% @ 450nm

Vop ~56 Volts @ 25 °C & ~49 Volts @LAr

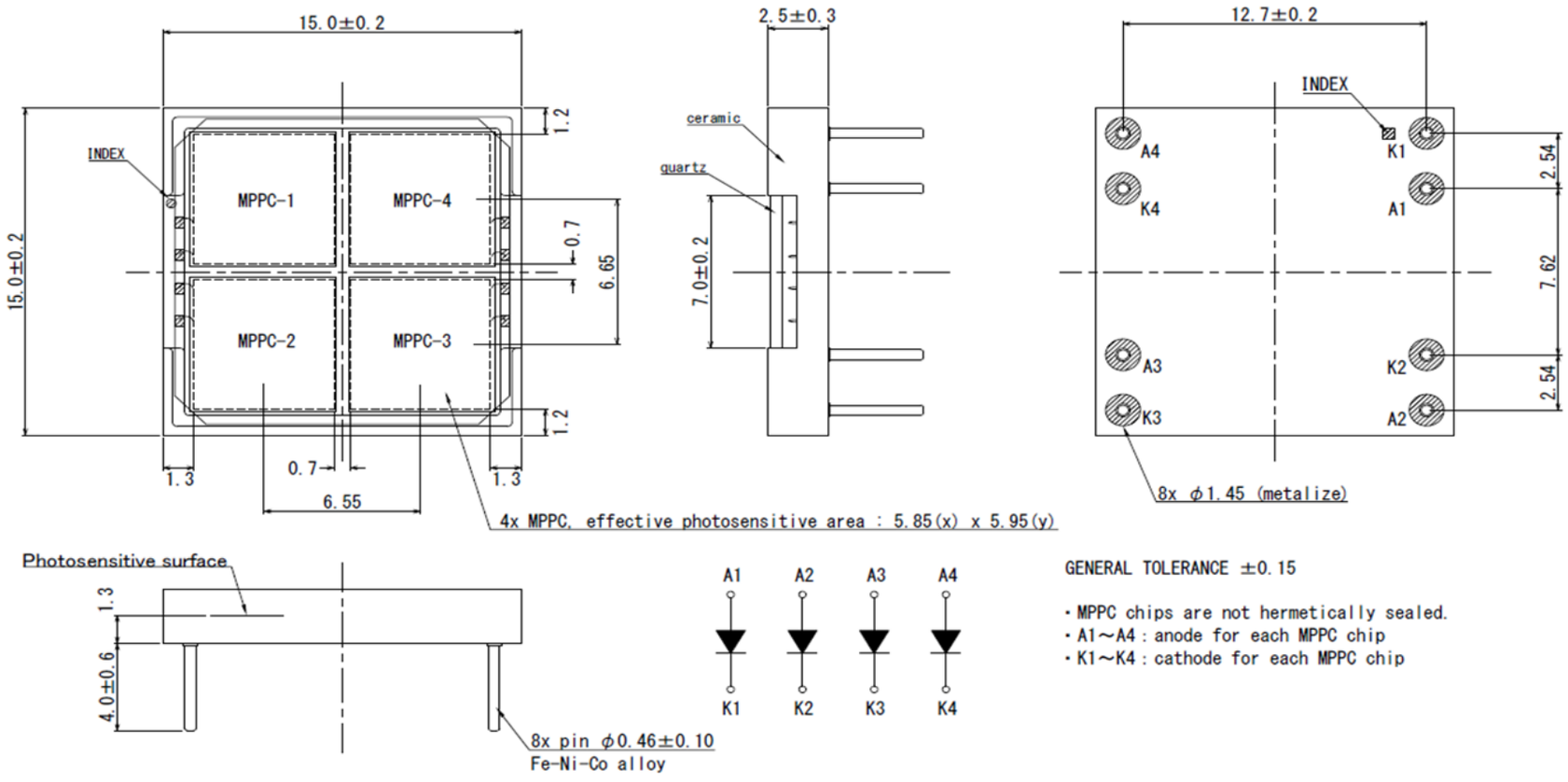
https://hamamatsu.su/files/uploads/pdf/3_mppc/s13370_vuv4-mppc_b_(1).pdf

We have 4 pieces of VUV-4 SiPMs @ CERN to be used for tests

Ta=25degC Shipping dat ##########

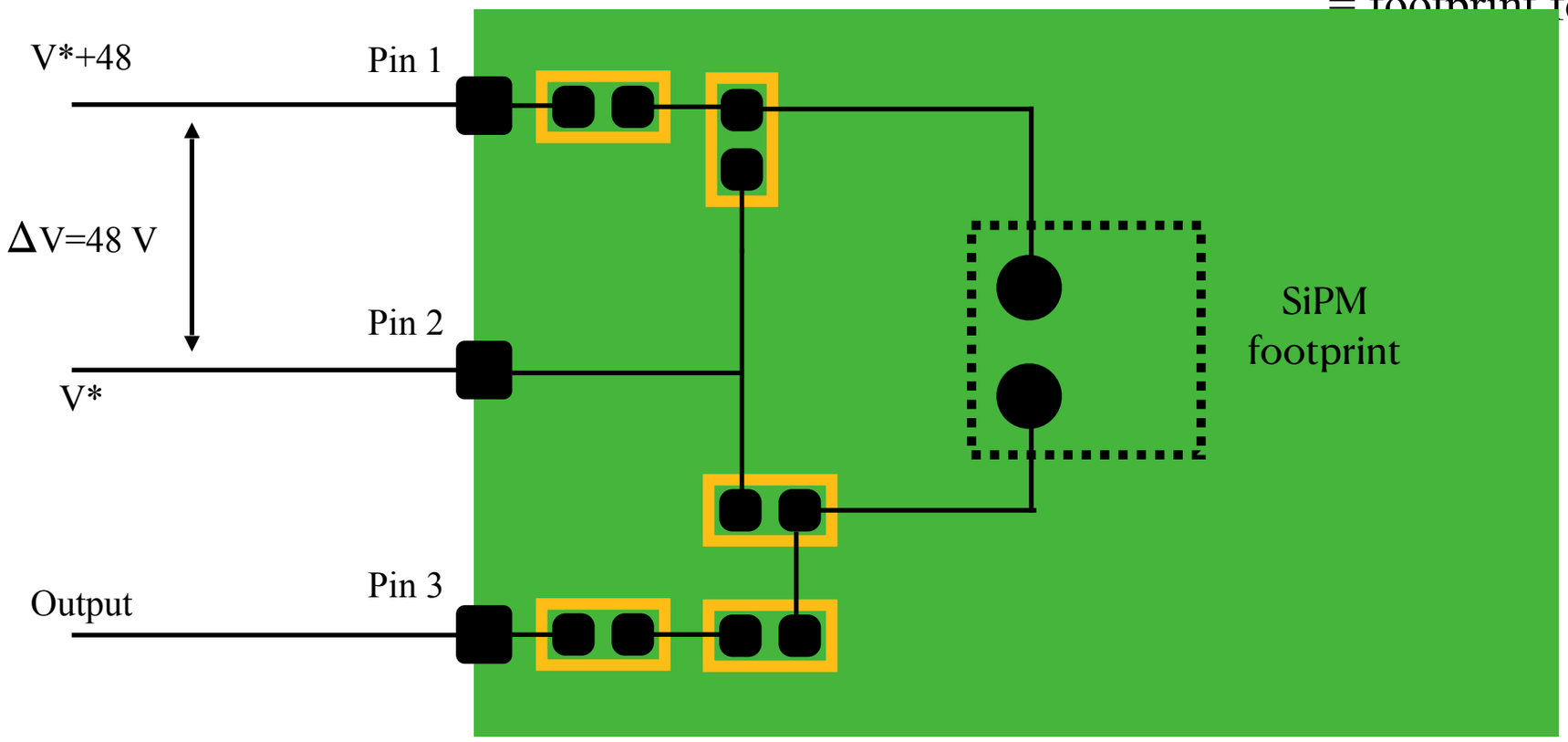
Serial No.	Element No.	Vop[V]	dark[μA] @Vop
266	A1	55.94	1.56
	A2	55.96	1.18
	A3	55.96	1.26
	A4	56.00	1.40
267	A1	55.94	1.21
	A2	56.00	1.22
	A3	56.00	1.35
	A4	56.03	1.49
268	A1	56.02	1.39
	A2	56.03	1.32
	A3	56.00	1.45
	A4	55.96	1.54
269	A1	56.11	1.45
	A2	56.12	1.48
	A3	56.11	1.77
	A4	56.11	1.64

@ 25 ºC

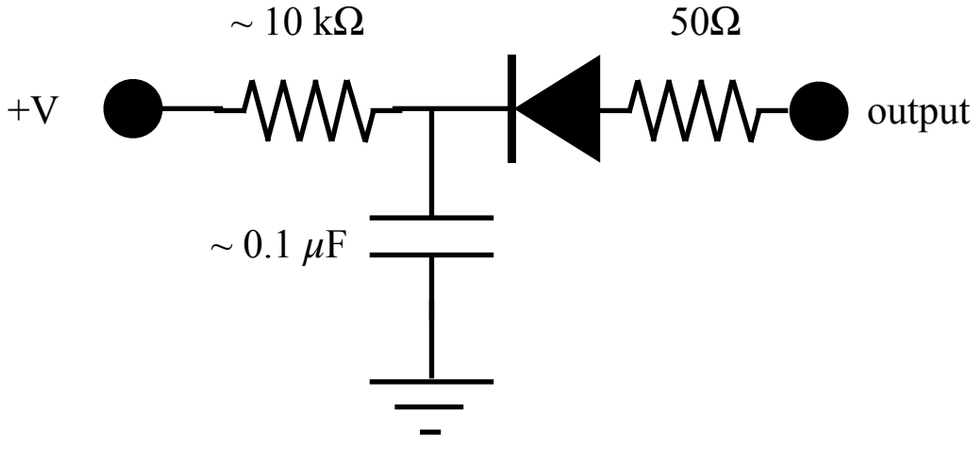


First SiPM board draw:

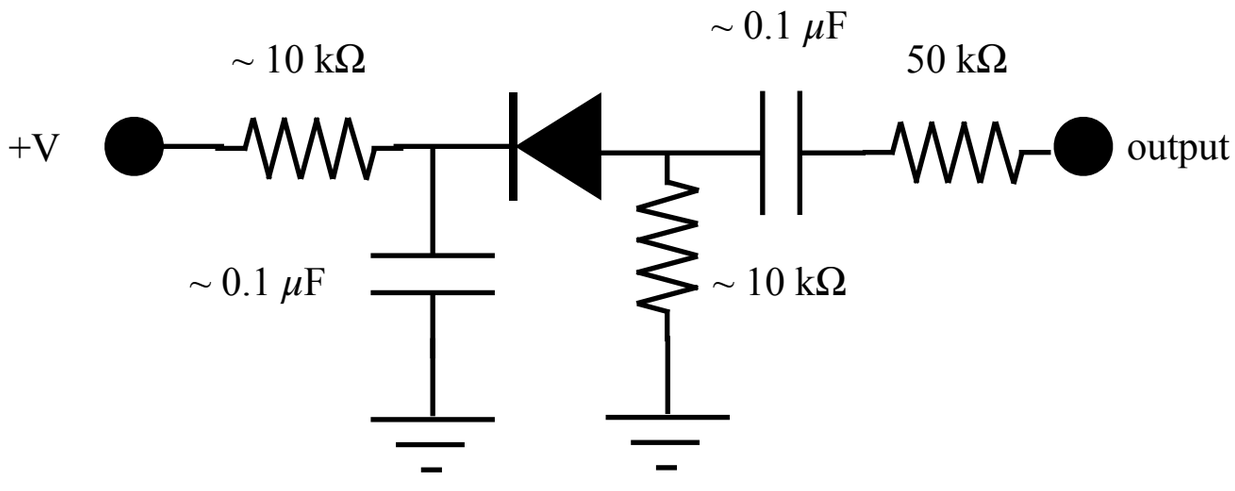
= footprint for surface mounted components



Configuration Standard

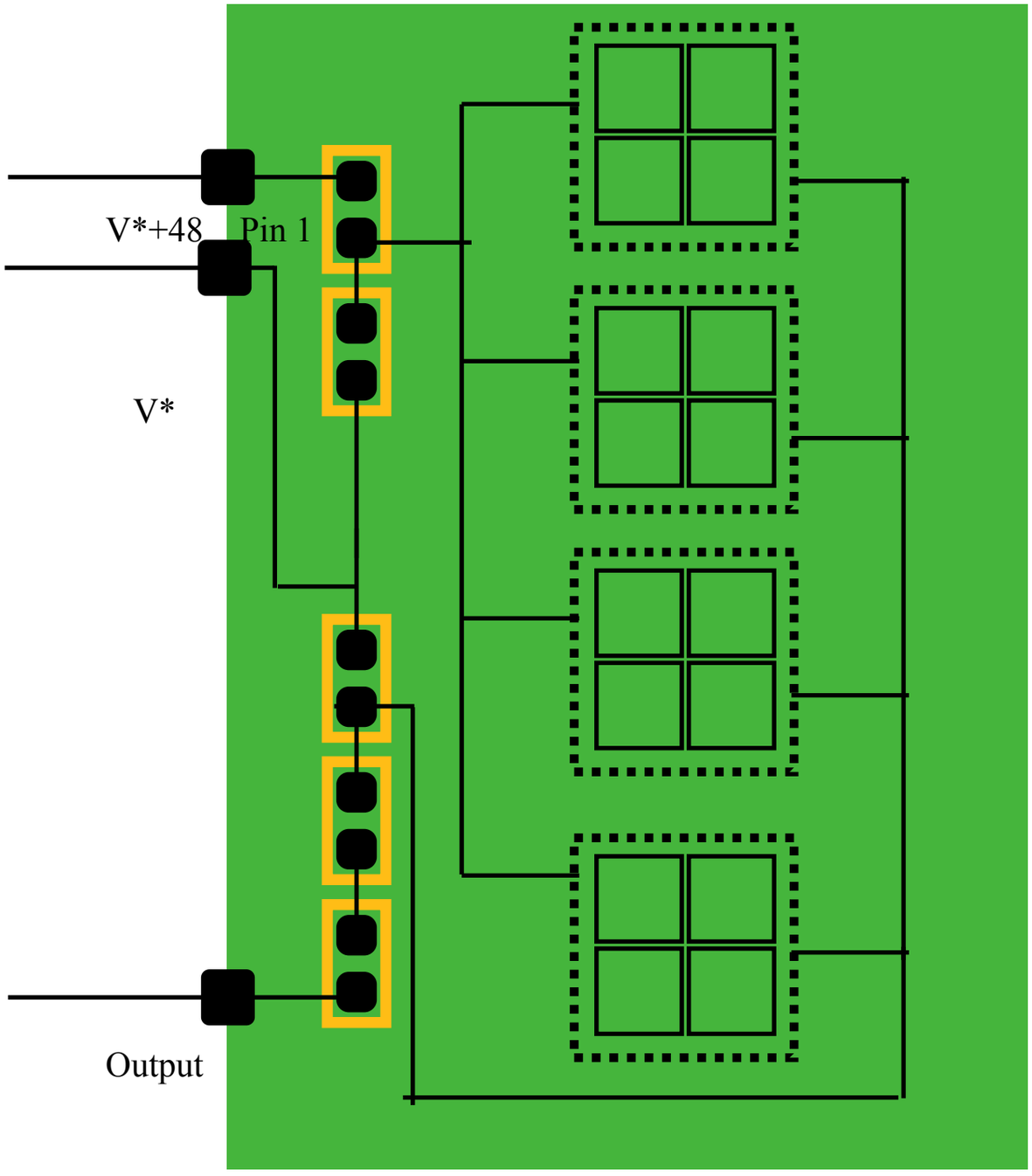


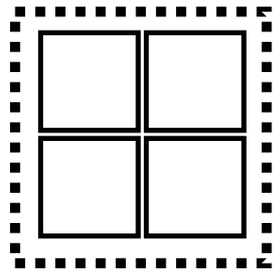
Alternative Configuration, SSP style.



Example of 4 Array (4x4) readout board.

With a very simple design we can choose the configuration, using jumper (0Ω) and let the footprint open

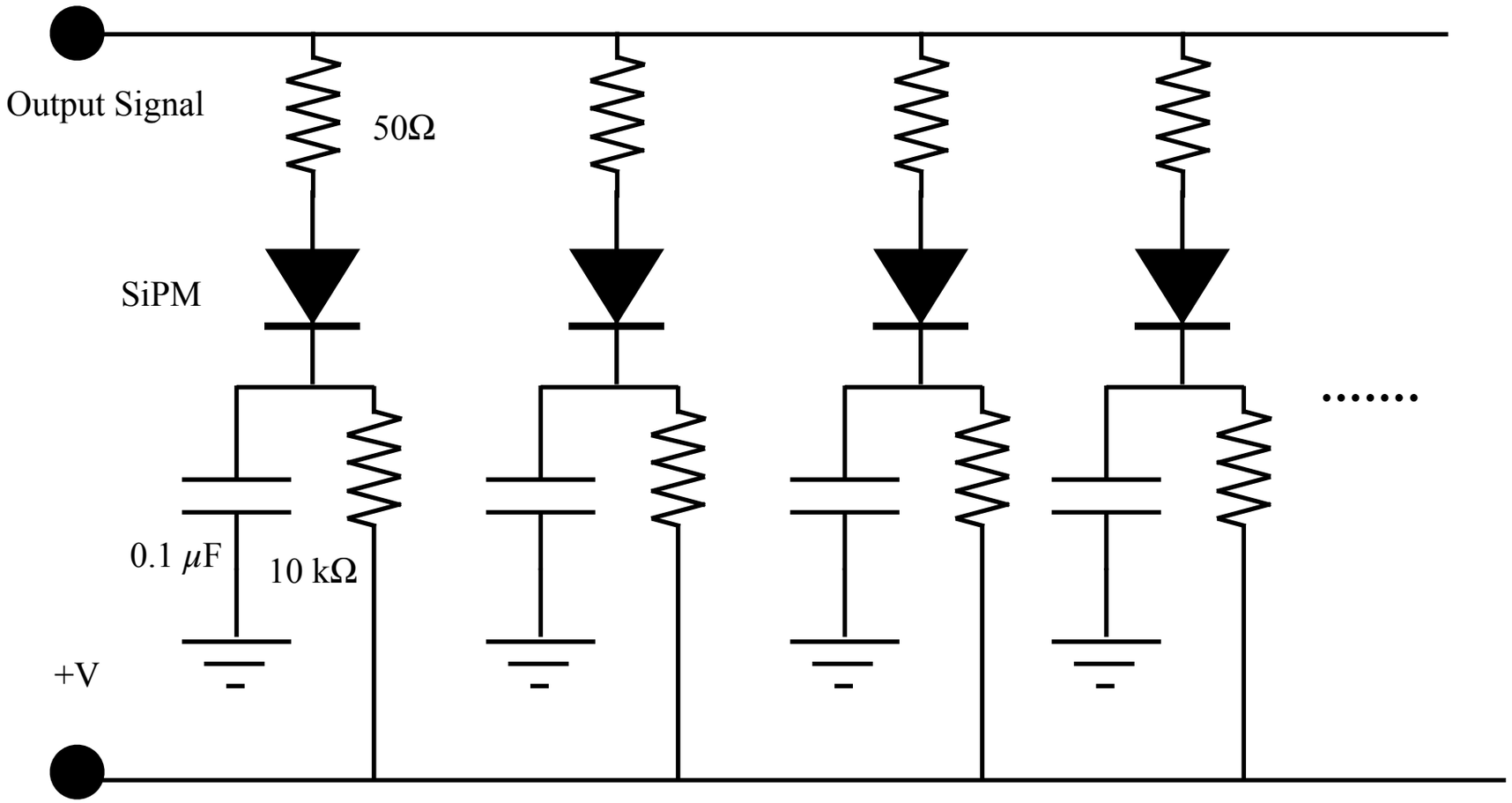




SiPM footprint

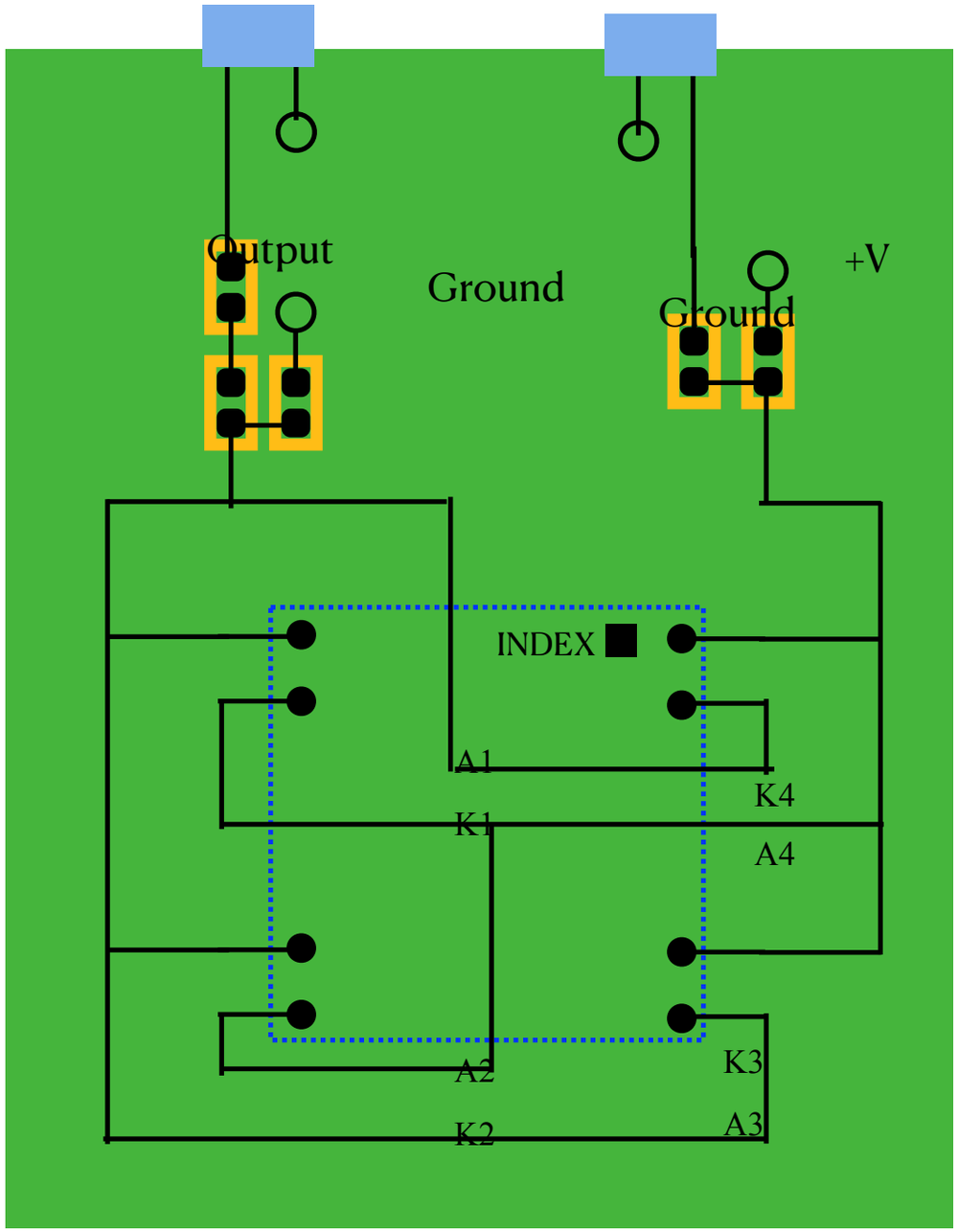
= footprint for surface mounted components

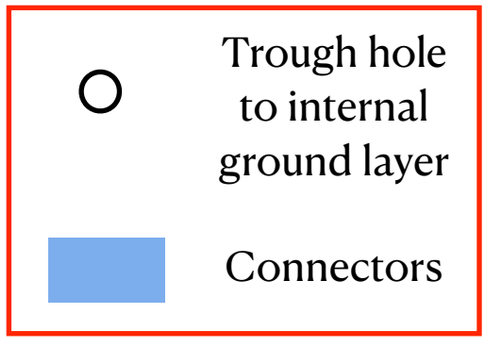
SiPM decoupled circuit:



More accurate designs, for a single 2x2 array

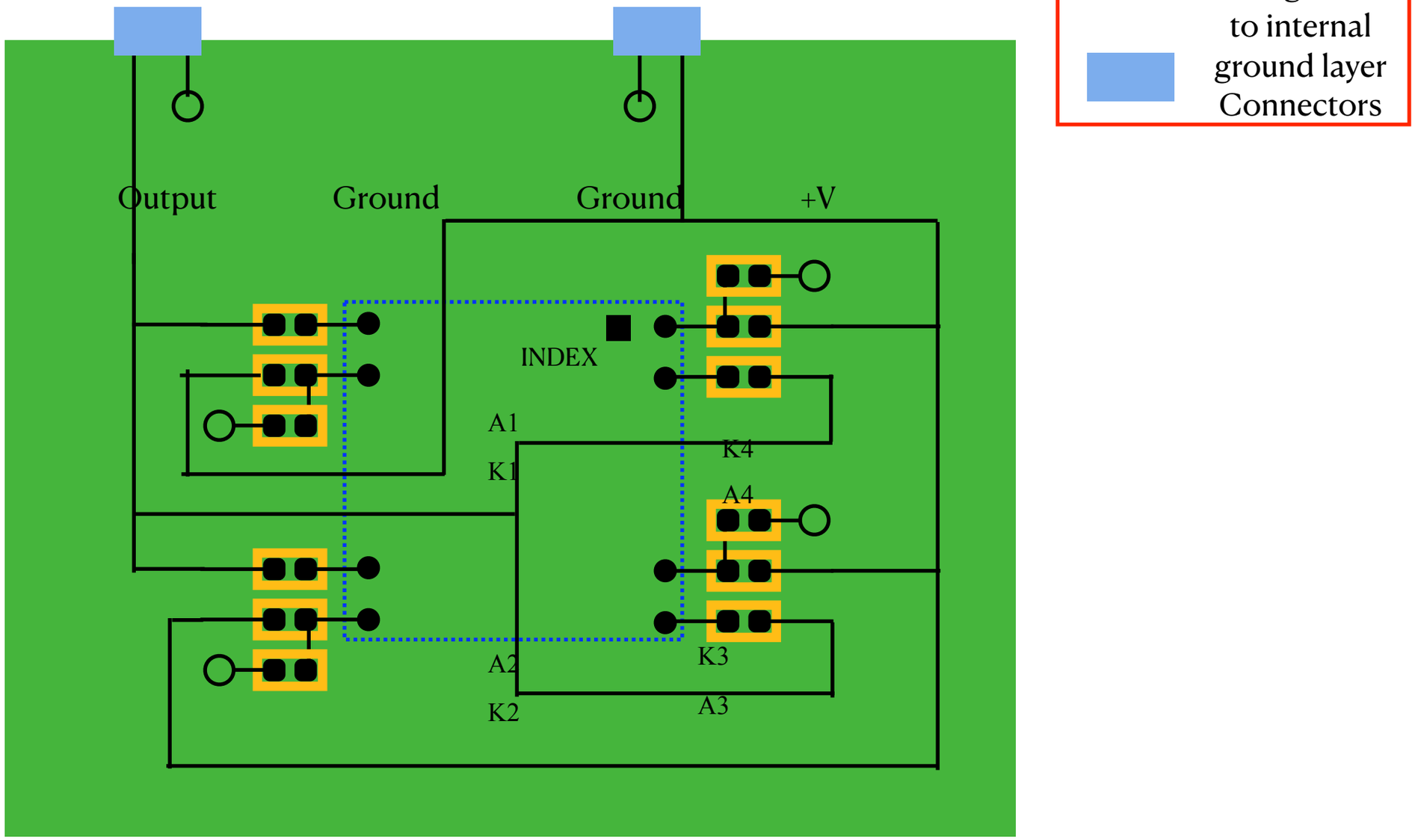
SiPM circuit:

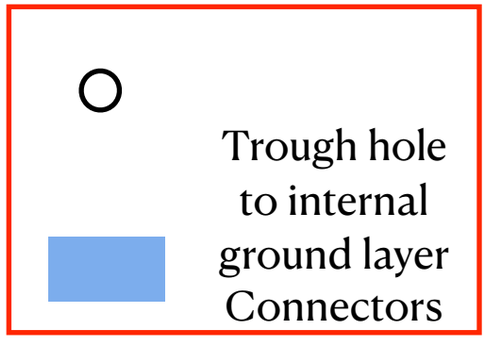




Both +V and Output are paired with ground pins to have te possibility to connect coaxial cables. This to allow standard test before to use the PoF system.

SiPM decoupled circuit:





SiPM board with multiple configurations: