xARAPUCA Tiles in the VD Cathode Structure

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VD Photon Detector Project

	2020	2021	2022	> 2023
Concept (Proposal)				
Prototype (ColdBox Test & Concept Validation)				
Optimization (Final Design)				
Mass Production				

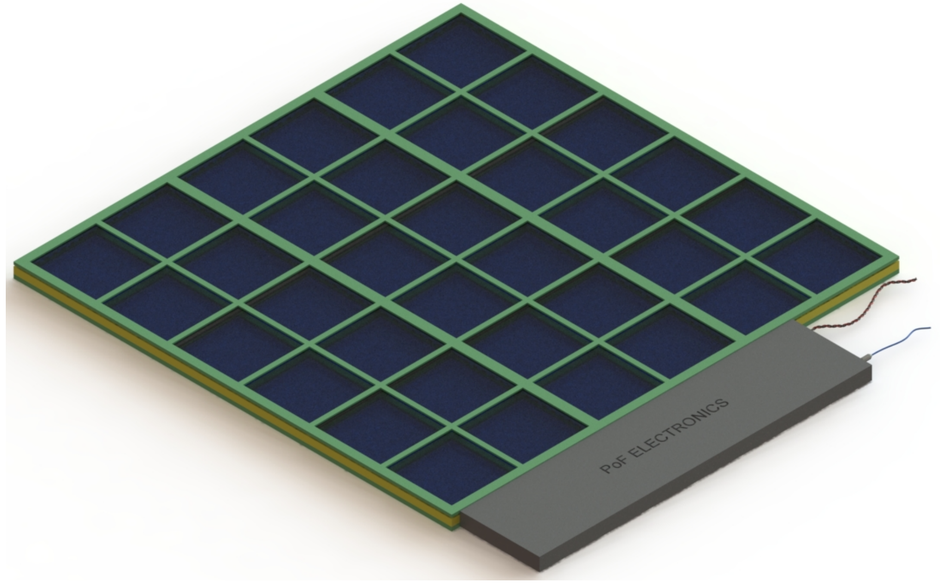
xARAPUCA Tiles (and CE box+In/Out Cables/Fibre) fabricated for Prototype test in Cold Box may very likely be different from xARAPUCA Tiles for Production

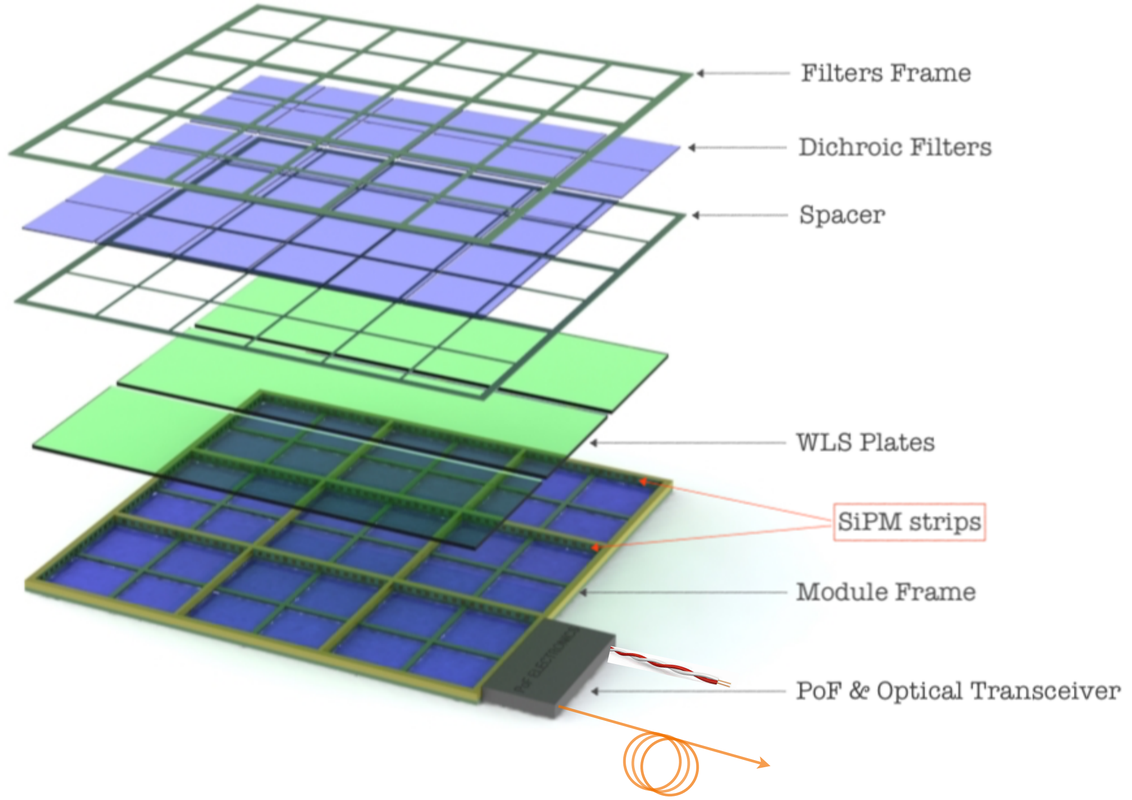
xARAPUCA current design (3D Model developed by Henriques F) derived from HD (PD for SinglePhase Module#1) design, optimized under extremely severe mechanical constraints [e.g. fit in tiny space allowed in APA mechanical frame].

For VD xARAPUCA optimization under [presumably] less severe constraints from the Cathode structure may lead to some changes (e.g. change of materials is not excluded at this moment) - Dave W (DUNE PD Consortium Tech Lead) will illustrate on the experience from HD PD optimization and perspectives for VD PD optimization.

Our goal for Today's discussion is intended to define:

- constraints and requirements for the realization of the prototype system [Cathode Module + 2 xARAPUCA Tiles] for the ColdBox Test at CERN in 2021
- Guidelines for design optimization

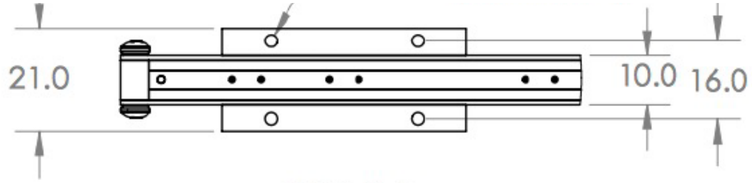




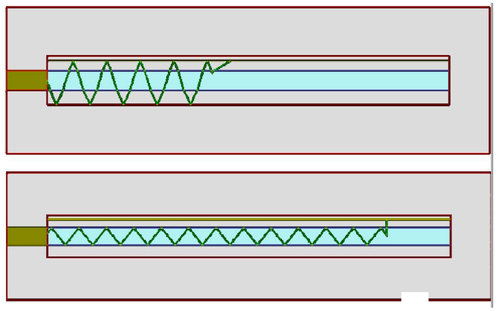
Active area = $\sum$Areas (dichroic filters $10 \times 10\ cm^2$) = 0.36 m^2

Cathode Requirement: Minimize any element of the Cathode that could project shadow over the active area (mesh and bars)

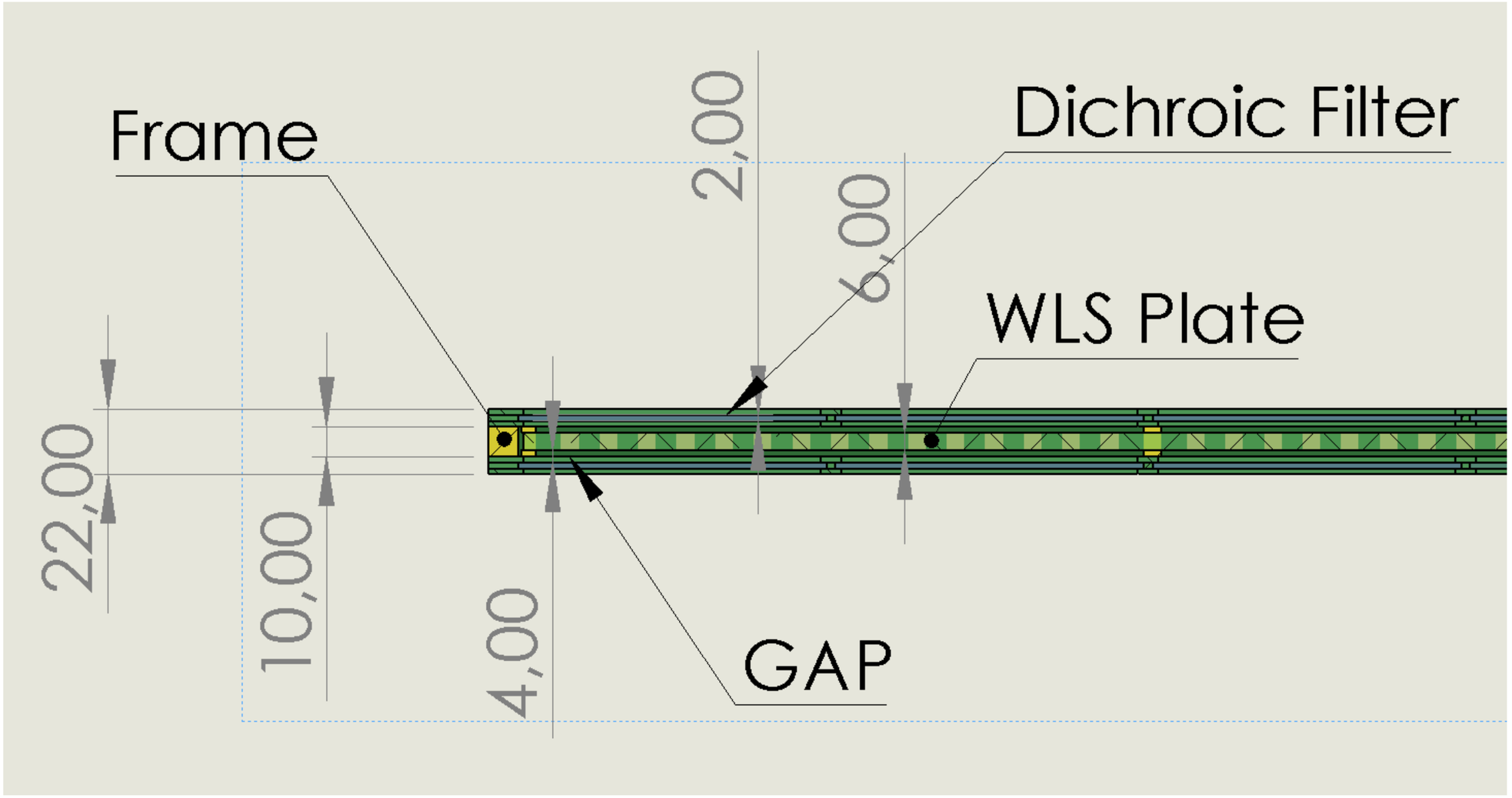
Total Thickness = Dichroic Filter(1 mm) + Gap(2 mm) + WLS plate(4 mm) + Gap(2 mm) + Dichroic Filter(1 mm) = 10 mm -

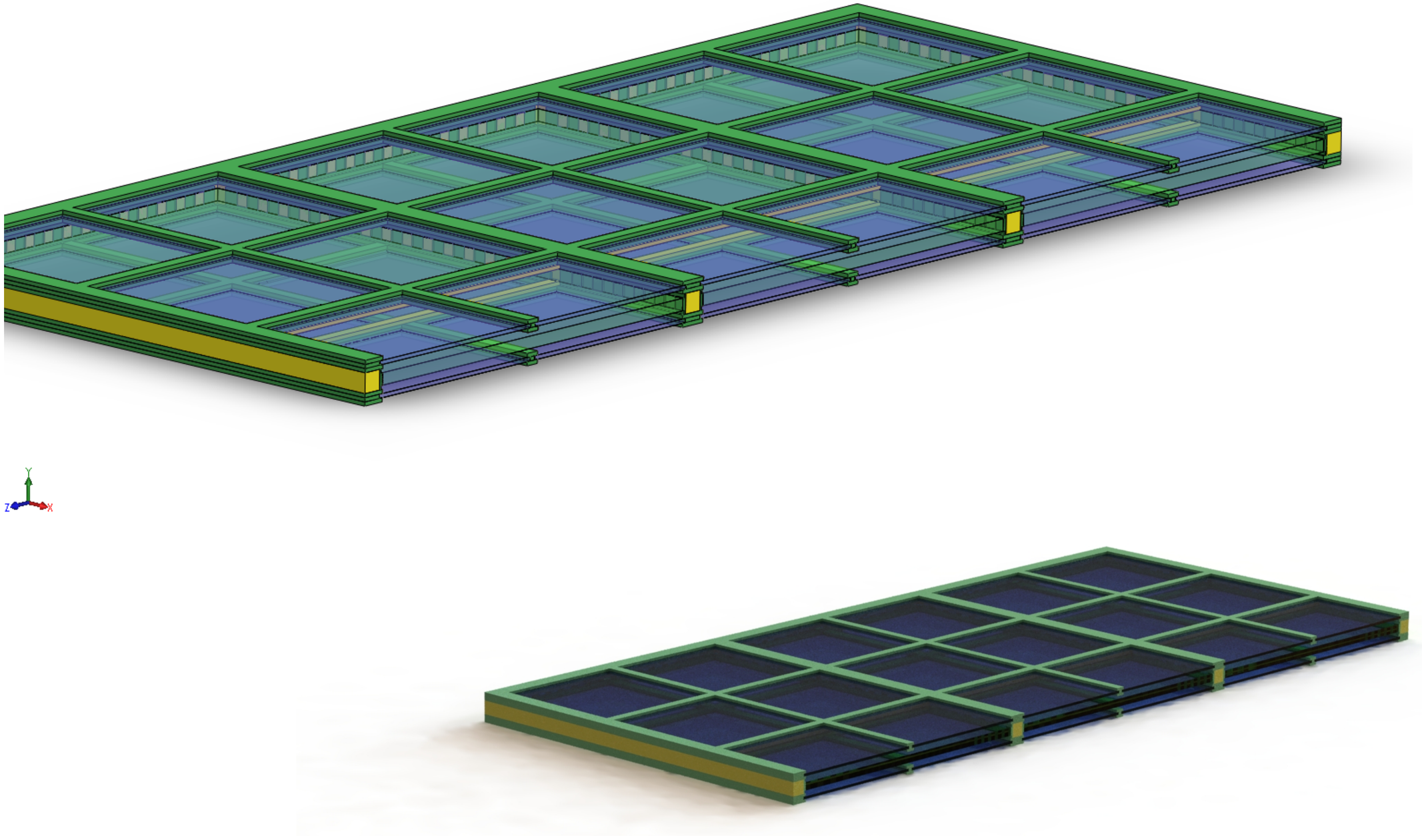


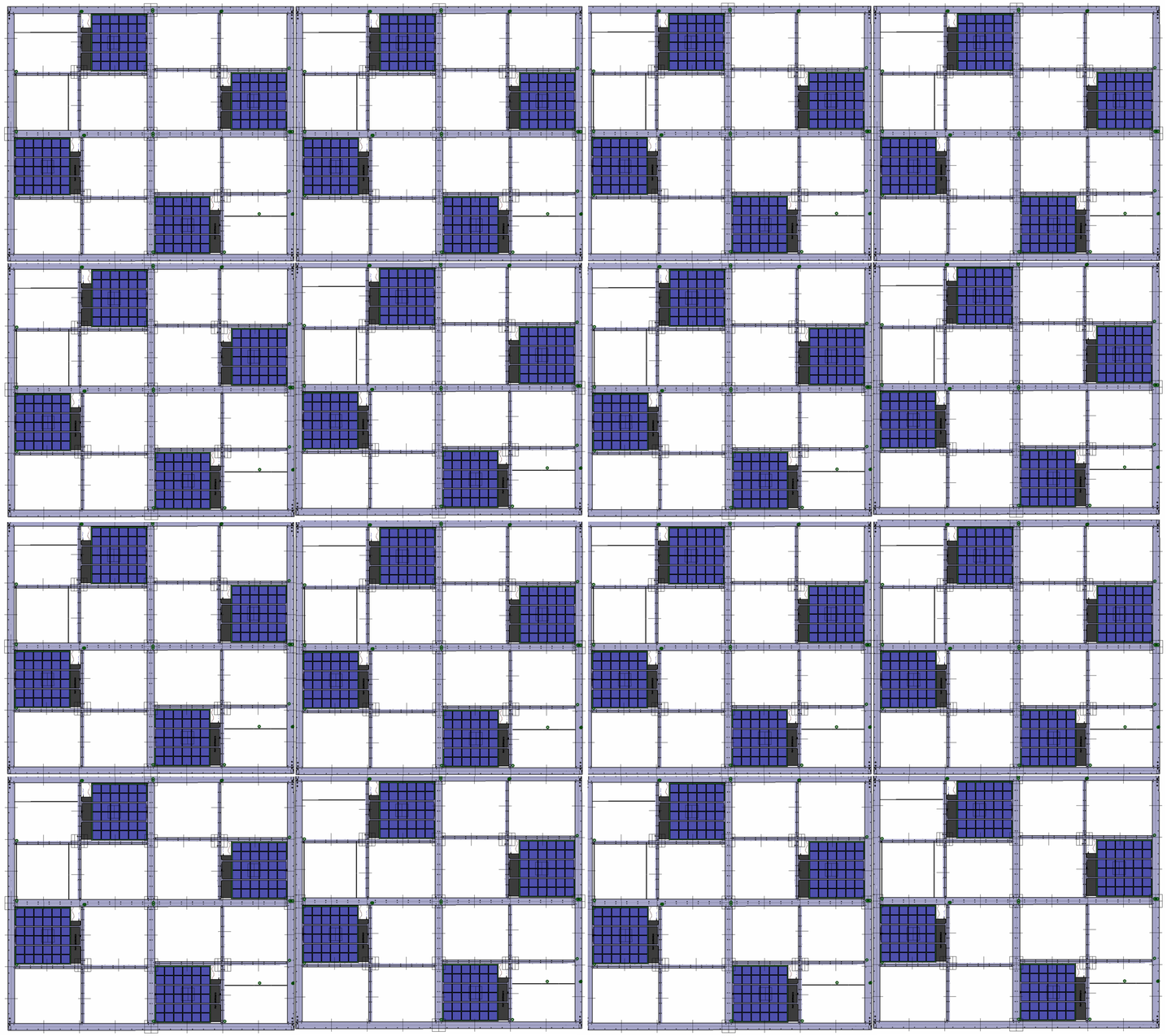
PD Requirement: Gap (2 mm) - optimized by MC simulation



Weight = 10.4 kg - determined by material (dichroic glass + WLS acrylic + FR4 frame) - optimization is possible (if needed)


Frame
2,00
Dichroic Filter
6,00
WLS Plate
22,00
10,00
4,00
GAP





PD **Requirement:** 14% Active Coverage

Square shape (60 cm side) chosen when Cathode shape was initially defined also as square (3 x 3 m^2) and *side length* = multiple of (commercially available) dichroic filter side length

Tiles position inside Cathode Module most evenly distributed with current structure segmentation

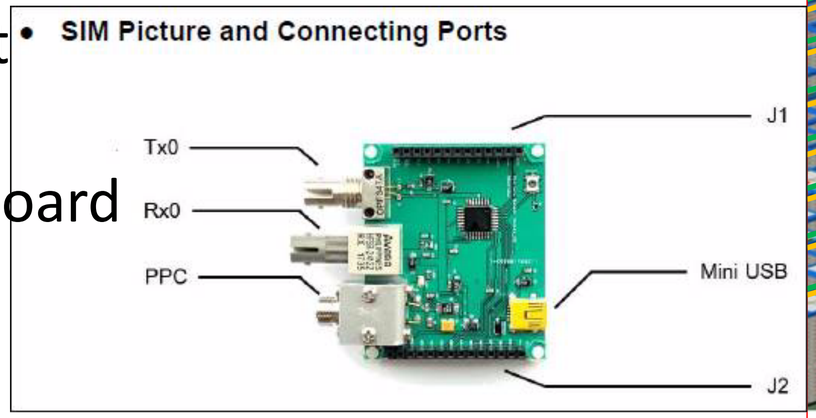
If a different structure layout is suggested, shape and position of the ARAPUCA tiles can be readjusted

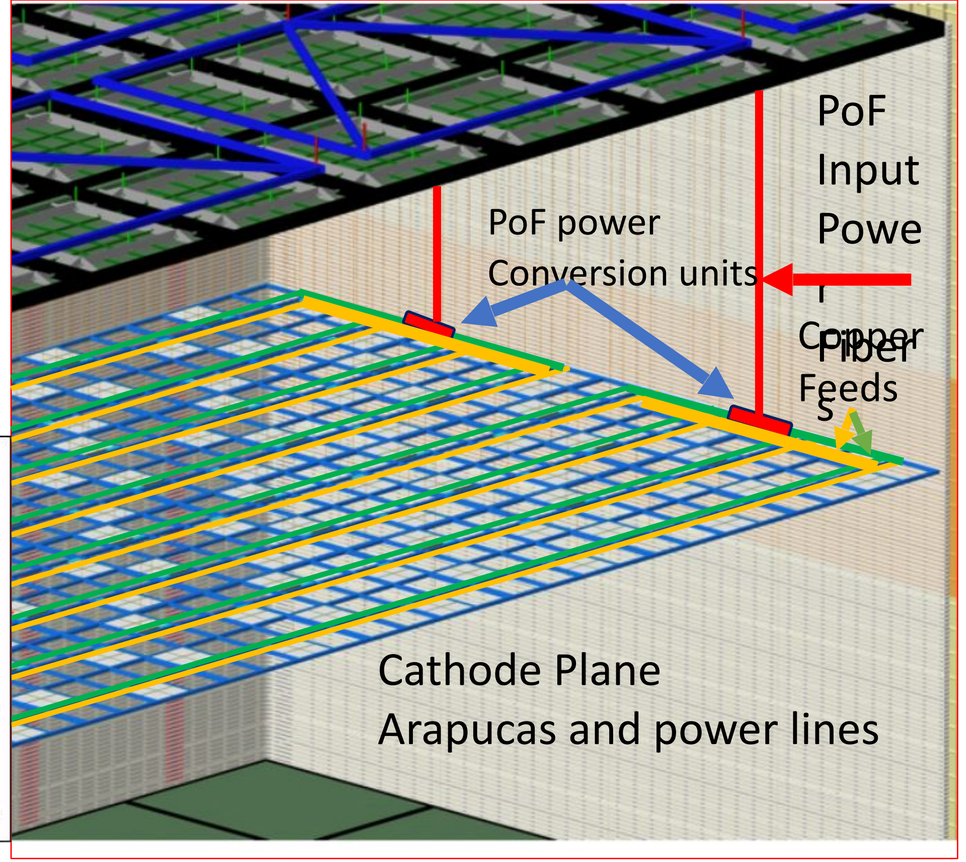
Electronics Digital Base Plan (box outside of SiPMs)

- Two stages of op amps (ganging and preamp)
- Three ADCs (could be single package)
- Consolidator – FPGA/ASIC
- Transmitter (Fiber – LED) Footprint unknown
- Voltage conditioning circuit
- Clock buffer

All would fit on a 12 cm^2 board

Could be smaller –

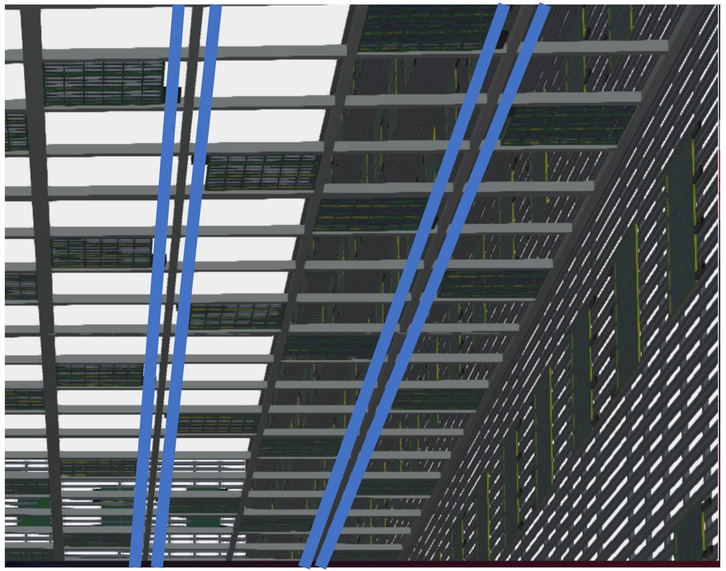




Wires/cables:

- One fiber out for transmitted data
- One Voltage wire and return reference for SiPM
  30 A.W.G. .3 lbs/1000 feet (shown in pic as green and yellow)
- One voltage wire and return reference for Cold Electronics
  30 A.W.G going to each ARAPUCA – .2lbs/1000 feet

Could use 32 A.W.G – less weight – less strength



Copper and Fiber Cables

- Each Arapuca will have a fiber transmit cable
- Each Arapuca will have a copper clock cable connected to an end of cathode
- Each Arapuca will have two copper cables connected in series to power SiPMs
- Each Arapuca will have two copper cables for powering electronics box