TDAQ group report

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for the Mu2eII tdaq subgroup

Outline

- Achievements to date
- Plan

Architectures under study

Two TDAQ architectures proposed so far:

1. **2-level Trigger (L1 Trigger + HLT)**
2. Software Trigger using GPUs

L1 + High Level Trigger

- Aggregate the data into a board equipped with multiple FPGAs
- Run the early stage of the track reconstruction + full calorimeter reconstruction
- Apply a L1 decision and move data to the HLT farm which runs full track reco

- **Main focus:**
  - **a.** do some processing on FPGA and the remainder on software
  - **b.** where are the boundaries?
  - **c.** can we make a L1 trigger decision at FPGA level?
  - d. track pattern-recognition on FPGA?
  - **e.** Need to develop FPGA algorithms

L1 + High Level Trigger: where do we stand?

- **Jinyuan Wu** illustrated a possible algorithm that can be implemented on FPGA
  - Need to access performance with simulated data
- Ryan illustrated to Richie and I how to use Vivado for doing development using High Level Synthesis
- Robert Soleti recently showed interest in doing development with HLS4ML
- Ideally, part of this development could be used/tested already in Mu2e
- We made a contribution to a white paper: **Applications and Techniques for Fast Machine-Learning in Science** – N. Tran et al., to be submitted on Big Data and AI in High Energy Physics
- **Richie Bonventre** gave a talk to CPAD

Software Trigger on GPUs

- Antonio and I have been in contact with Gianluca Lamanna from Pisa
- He suggested us a way to make preliminary tests using **OpenAcc** to parallelize KinKal package
- Plane to start working on it after in April

Main focus:

- Trying to set up OpenACC for estimating the performance gain of the KinKal track-fitter algorithm
- Interface with artdaq? Starting referring to the paper:
    - GPU-accelerated machine learning inference as a service for computing in neutrino experiments

Expected timeline

- Waiting simulated data from the Mu2e-II software group
    - This will allow us to start some preliminary tests
- We will restart our meeting in May
- Focus during the summer in testing FPGA/HLS algorithm development
- In the same period, we expect to move forward the GPU benchmark studies