Short-term Plan

DUNE Far Detector #2
Photon Detector System

Last update: April 14, 2021

Upcoming Milestone Reminder

Milestone Target Date	Milestone Definition
End-of-May	Pair-wise demonstration of 1st promising candidate for each component with power solution
End-of-August	2x v1 prototypes ready for CERN Cold Box Test

Prototype Status

- How many SiPMs will we have?
  - 120 SiPMs expected by end of April
    - Carla C. & Glass-to-power 60cm x 60cm proof of concepts have begun
    - Have begun CERN cold test mechanical assembly concept
  - Expect 500 SiPMs in time for cold box test from Milano/Madrid/Prague
  - Split among two prototypes (160 SiPM each)
    - Prefer to avoid mixing types in same prototype (rather use <160)
      - Preferable to try different type in each prototype
- We are targeting one digital and one analog prototype (two options for each)
  - Analog Tx for 1 tile:
    - 160 SiPM ⇒ 2 x 80 SiPM ⇒ 2 Analog Tx channel
      - or option to 1 Analog Tx channel
  - Digital Tx for 1 tile:
    - 160 SiPM ⇒ 2 x 80 SiPM ⇒ 2 x ((5 x 4 passive gang) x 4 active gang) ⇒ 2 x OpAmps ⇒ 2 ADC channel
      - or option to insulated thermostat

Component	Who?	Last-week Goal	1-week Goal	April Goal	May Goal
xARAPUCA	Maura S	Optimize topology, identify source	Identify first candidate power interface	15 boards (120 SiPMs) from Milano/Madrid/Prague	Optimize topology, identify source
Passive Gang	Dante T, Gustavo C, Dave C	Optimize topology	Identify first candidate power interface	Fabricate v1 test circuit board	Optimize topology for v2
Active Gang	Dante T, Gustavo C, Dave C	Optimize topology	Identify first candidate power interface	Fabricate v1 test circuit board	Optimize topology for v2
Digital Tx	Alan P, Dave C	Identify first candidate power interface	Assemble v1 test circuits.	Document plan for v1 cold test demo with power solution	Assemble v2 test circuits and test.
Analog Tx	Sabrina S, Jaime D, INFN?	Identify first candidate power interface	Assemble v1 test circuits.	Document plan for v1 cold test demo with power solution	Assemble v2 test circuits and test.
SERDES / FPGA	Andres QP, Divya S, Jonathan E	Identify first candidate power interface	Layout v1 test circuits. Test v0 power delivery in cold.	Assemble v1 test circuits. Test v0 power delivery in cold.	Document plan for v1 cold test demo with power solution and assemble v2 test circuits.
ADC	Gustavo C, Andres QP, Divya S, Jonathan E	Identify first candidate power interface	Layout v1 test circuits. Test v0 power delivery in cold.	Assemble v1 test circuits. Test v0 power delivery in cold.	Document plan for v1 cold test demo with power solution and assemble v2 test circuits.
Control Rx	Alan P	-	Identify first candidate power interface	Document plan for v1 cold test demo with power solution	Assemble v1 test circuits and test.
Sync Distribution	Jonathan E	-	-	-	Identify first candidate power interface
Power Solutions	Bill P	Develop concepts for digital electronics voltage and current	Provide FPGA and ADC v0 power delivery for cold test.	Document plan for v1 cold test demo with power solutions	Pair-wise demo of v1 cold power solutions.

Spreadsheets

- Cold Qualified components:
  - https://docs.google.com/spreadsheets/d/1dCKDbuXOuSvq9h1HQ2d9sXCRqmNE4AAi7NyTwuSiF2Q/edit?usp=sharing
- Power Specs by component:
  - https://docs.google.com/spreadsheets/d/1ZeUE1z3lH9bQ906UZQhzCqV-Y0kPB0fPDfBbOw4dHs0/edit?usp=sharing