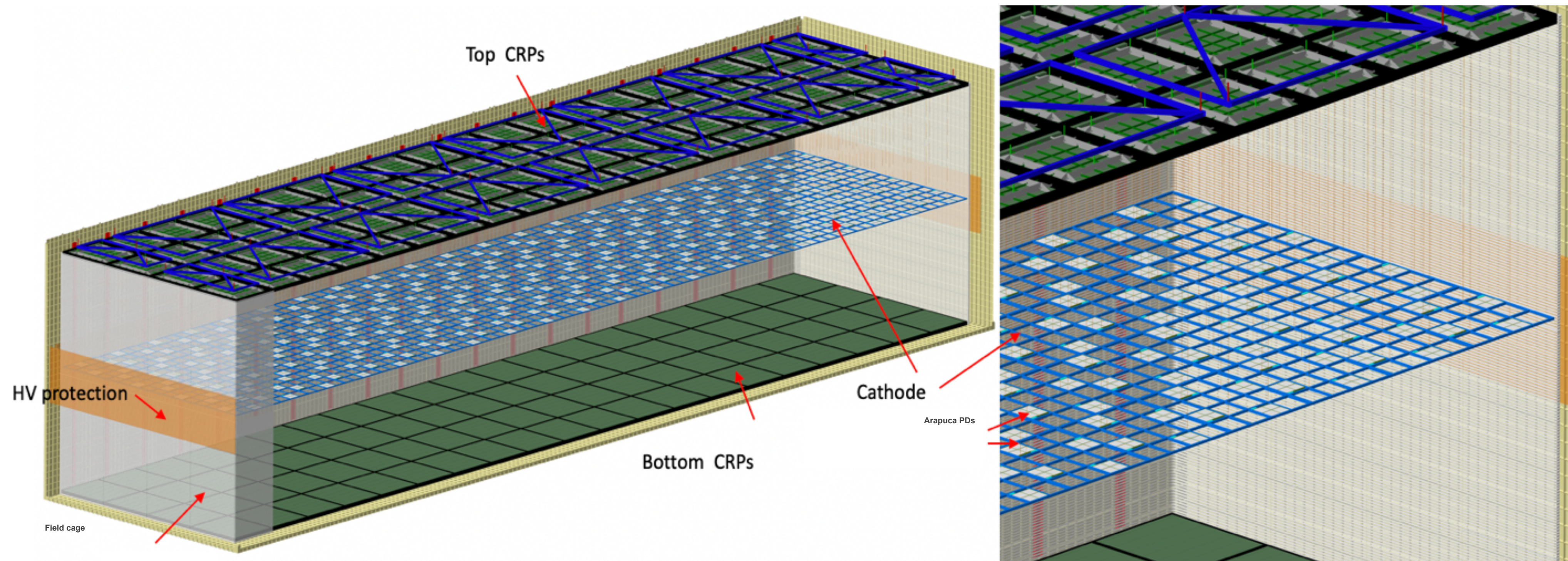


Vertical Drift Photon Detector (VD PD)



Ettore Segreto (UNICAMP)
Flavio Cavanna (FERMILAB)

28 April 2021

- (min) Requirements and VD PD matching

- The VD Reference PD System (PDS):

- Main Features: LY maps, energy resolution and position resolution.
- Low En UG Physics with a $\sim 4\pi$ PDS
- Cost estimate - (from WBS)

- The VD Backup PDS option:

- Main Features: LY maps matching min requirements (t0 for TPC)
- Cost estimate

- R&D toward VD Reference PDS:

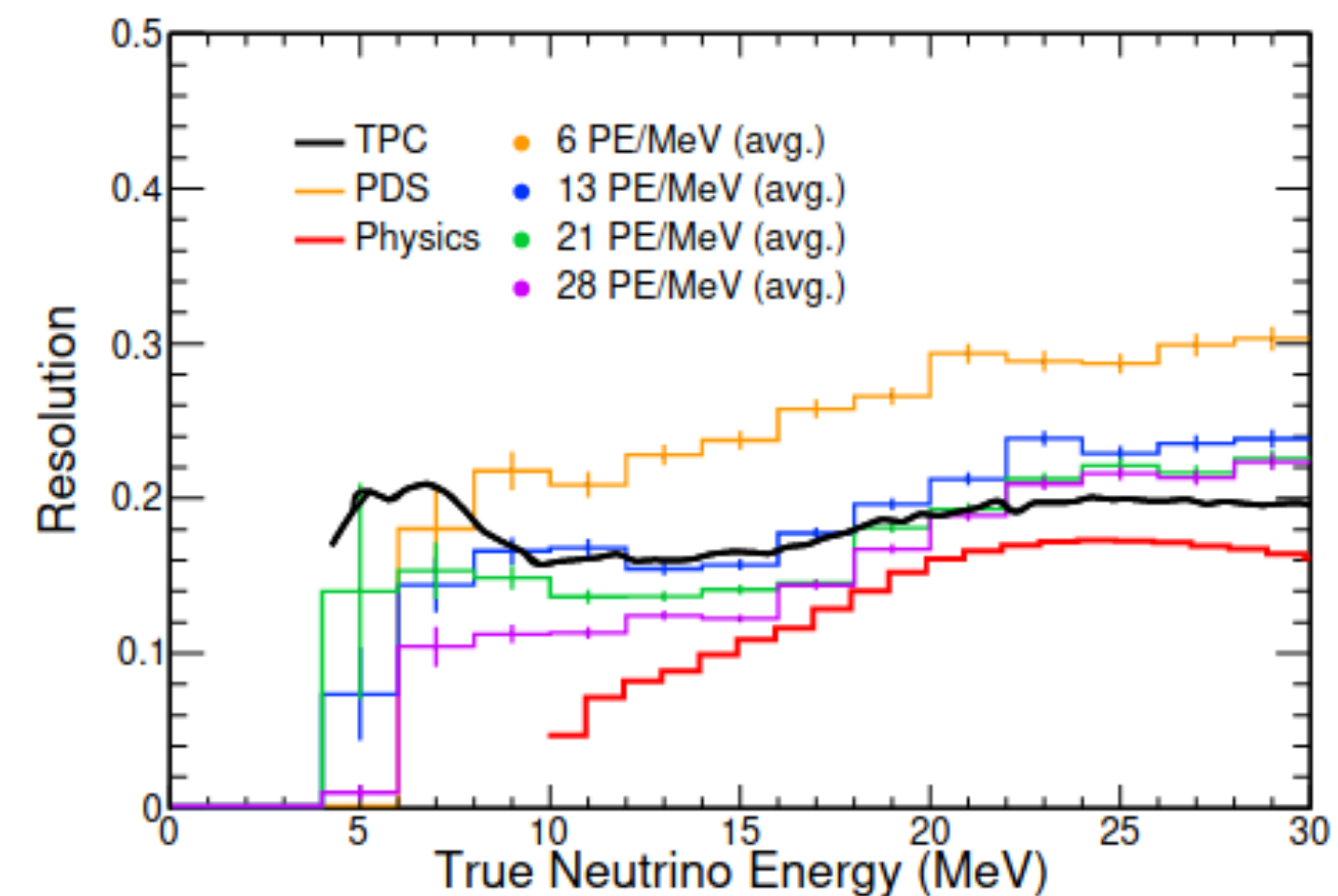
- The challenge & the solutions under development
- The achievements so far:
 - xARAPUCA Tile (improvements)
 - Power over Fiber
 - [Analog] CE+Transmission
 - [Digital] CE + Transmission (in progress)
- Formation of VD PD core-group

- Summary

PD HD Requirements

Label	Description	Specification (Goal)	Rationale	Validation
SP-FD-3	Light yield	> 20 PE/MeV (avg.) > 0.5 PE/MeV (min.)	Gives PDS energy resolution comparable to that of the TPC for 5-7 MeV SN ν s, and allows tagging of $> 99\%$ of nucleon decay backgrounds with light at all points in detector.	Supernova and nucleon decay events in the FD with full simulation and reconstruction.
SP-FD-4	Time resolution	$< 1 \mu\text{s}$ (< 100 ns)	Enables 1 mm position resolution for 10 MeV SNB candidate events for instantaneous rate $< 1 \text{ m}^{-3}\text{ms}^{-1}$.	

The Physics requirements have been translated into detector requirements through detailed full simulations of the SP HD far detector and of large samples of Supernova and nucleon decay events and rad. Background



Path towards PD VD Detector Requirements

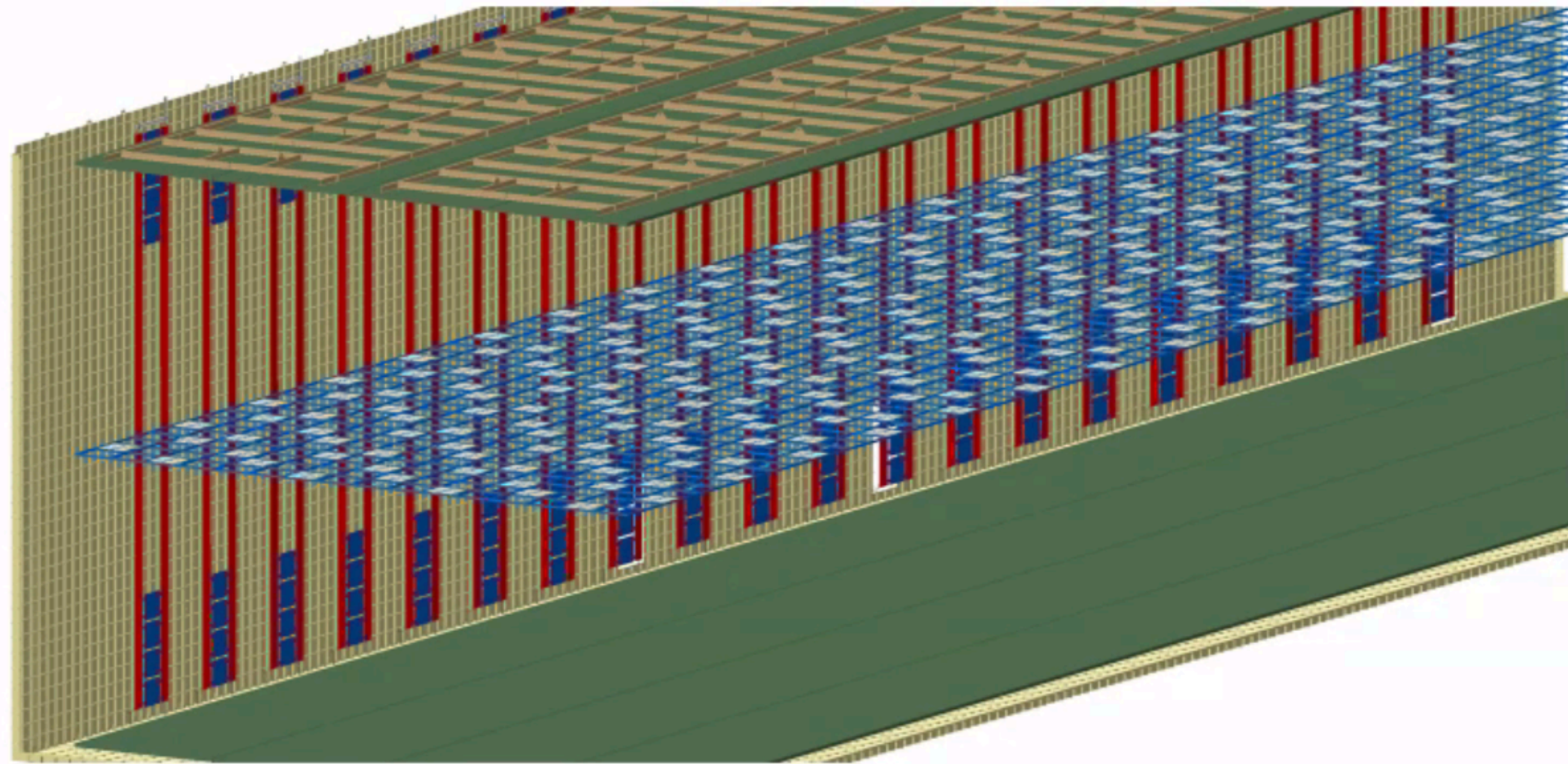
- The new VD TPC design offers more flexibility/less mechanical constraints than in the HD for the design of the PDS \Rightarrow possibility of enhancing PDS performance \Rightarrow expanding Physics reach with VD PDS
- There are major differences in dimensions (**longer light source-detector distances**) and distribution of photo-sensitive area around the LAr active volume
- The full MC Simulation study for HD PD Requirements is a solid starting point for the VD PD **Minimum Requirement** determination
- Current assumption:
 - to keep $\langle LY \rangle = 20$ PE/MeV [HD Requirement] as VD Minimum Requirement - related to the average Energy Resolution of the VD PDS
 - to re-evaluate the $\langle LY_{Min} \rangle$ Requirement for VD. For now, keep $\langle LY_{Min} \rangle = 0.5$ PE/MeV [HD Requirement] as VD Minimum Requirement - related to T_0 tagging for nucleon decay background events everywhere inside the VD active volume

Based on these Requirement assumptions, two design options have been identified

[both based on xARAPUCA technology for light detection \oplus Xe-doping - $\mathcal{O}(10$ ppm)]

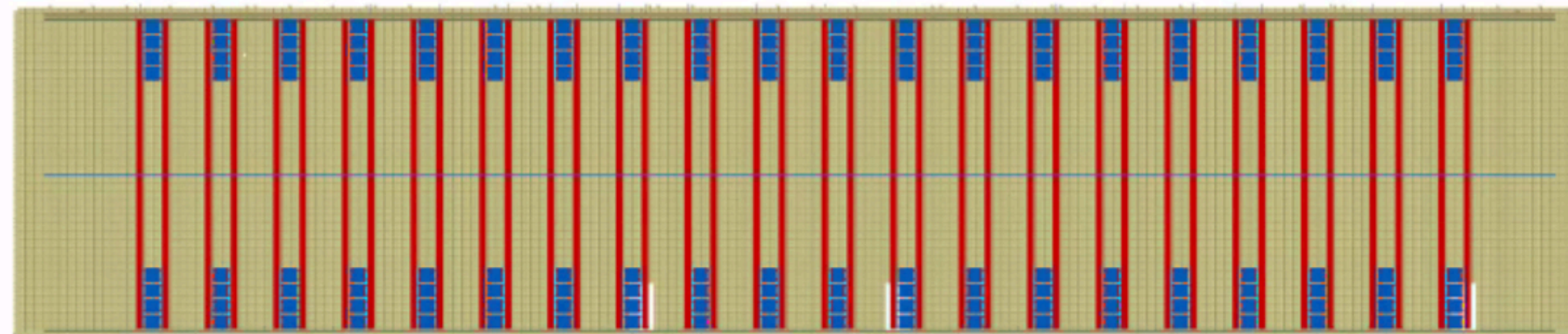
VD PDS Options: Reference ~4pi Design and Backup Design

Reference Design (Cathode & Membrane mounted PDS ⊕ Xe doping)

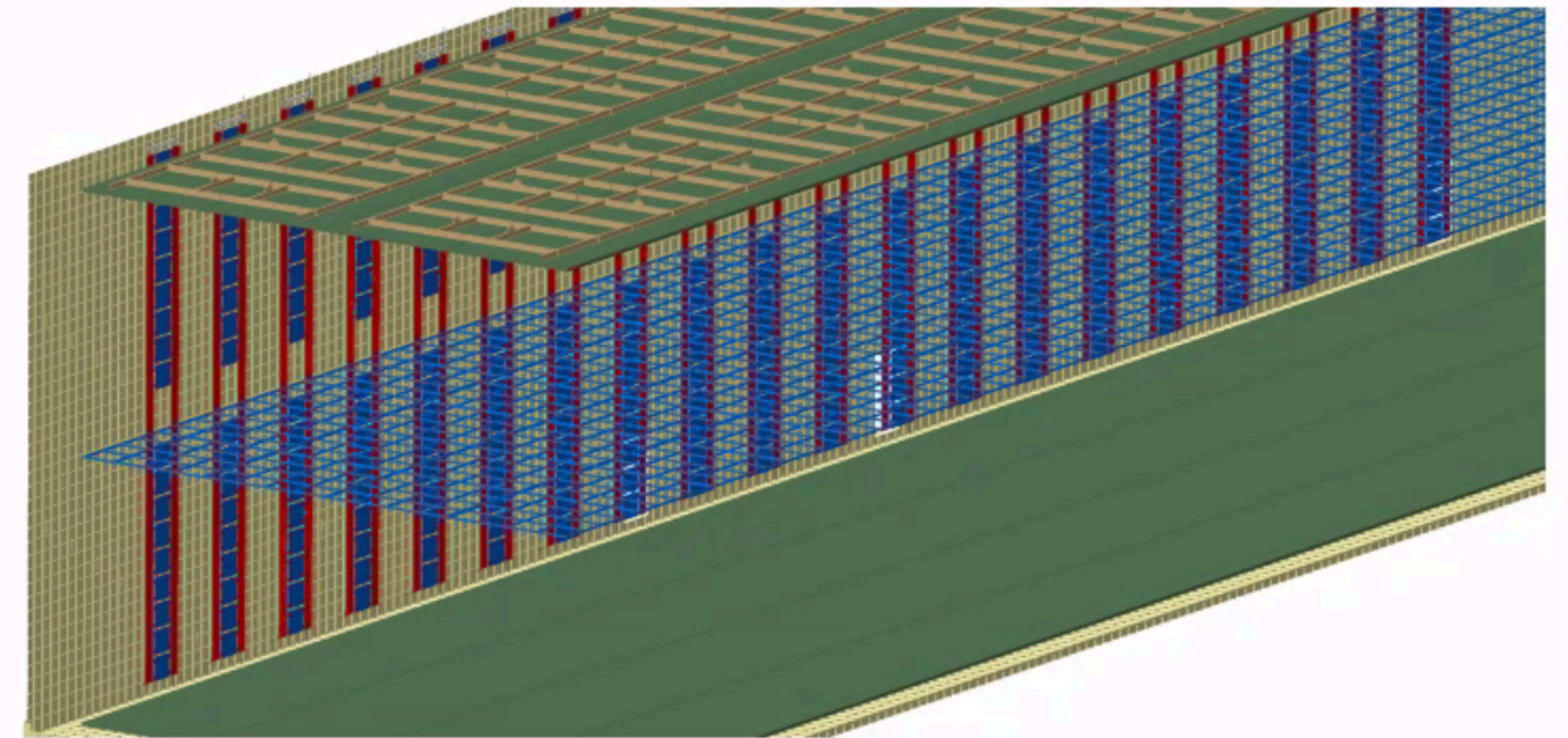


4 pi layout :

- Full trigger capabilities down to 10 MeV
- Energy, Position and T0
- xArapucas 60x60 on the cathode, 115 mq, analog readout
- xArapucas 60x60 on the cryo membrane, ~3m from Cathode

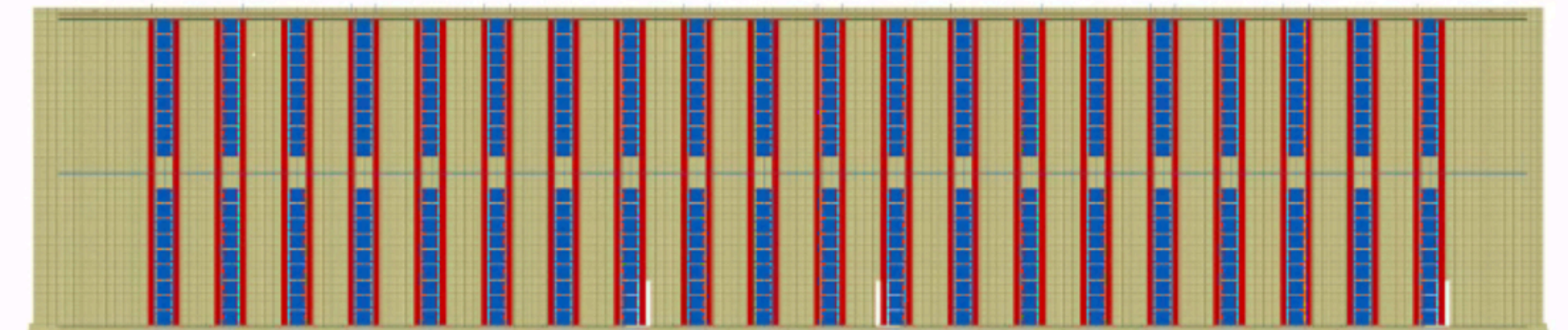


Backup Design (All-Membrane mounted PDS ⊕ Xe doping)



Minimal layout:

- Trigger via charge TPC readout down to 10 MeV
- T0, (Energy)
- xArapucas 60x60 on the cryo membrane, 20 columns, each column 18 xArapucas, SPHD readout



the VD Reference design

- The VD PDS reference design has different and more performant objectives than those of the design implemented in HD PDS, by exploiting the greater flexibility of the new VD TPC mechanics, while keeping costs and power dissipation in LAr within the same limits as the HD PDS.
- The main objective in the VD PDS Reference design is to make the LY uniform throughout the volume and higher on average, so as to be able to perform calorimetry and space reconstruction (and therefore also Trigger with max efficiency) down to a very low threshold \Rightarrow enabling extension of DUNE Physics reach in the UG Low Energy range.
- The added risk is from operating PDS on HV planes (i.e. requiring transmission of Power and Signal over fiber)
- The HD requirements are comfortably met in the VD Reference design. The HD requirements thus represent the *minimum requirements* for VD, while the VD goals are more stringent and ambitious - and motivate the 4pi design.
- *Risk Opportunity: the Reference Photon Detector is completely independent and redundant to the Charge TPC. This represents a big risk mitigation for physics if the TPC needs some maintenance period or will show some problems with time*

the VD Backup design

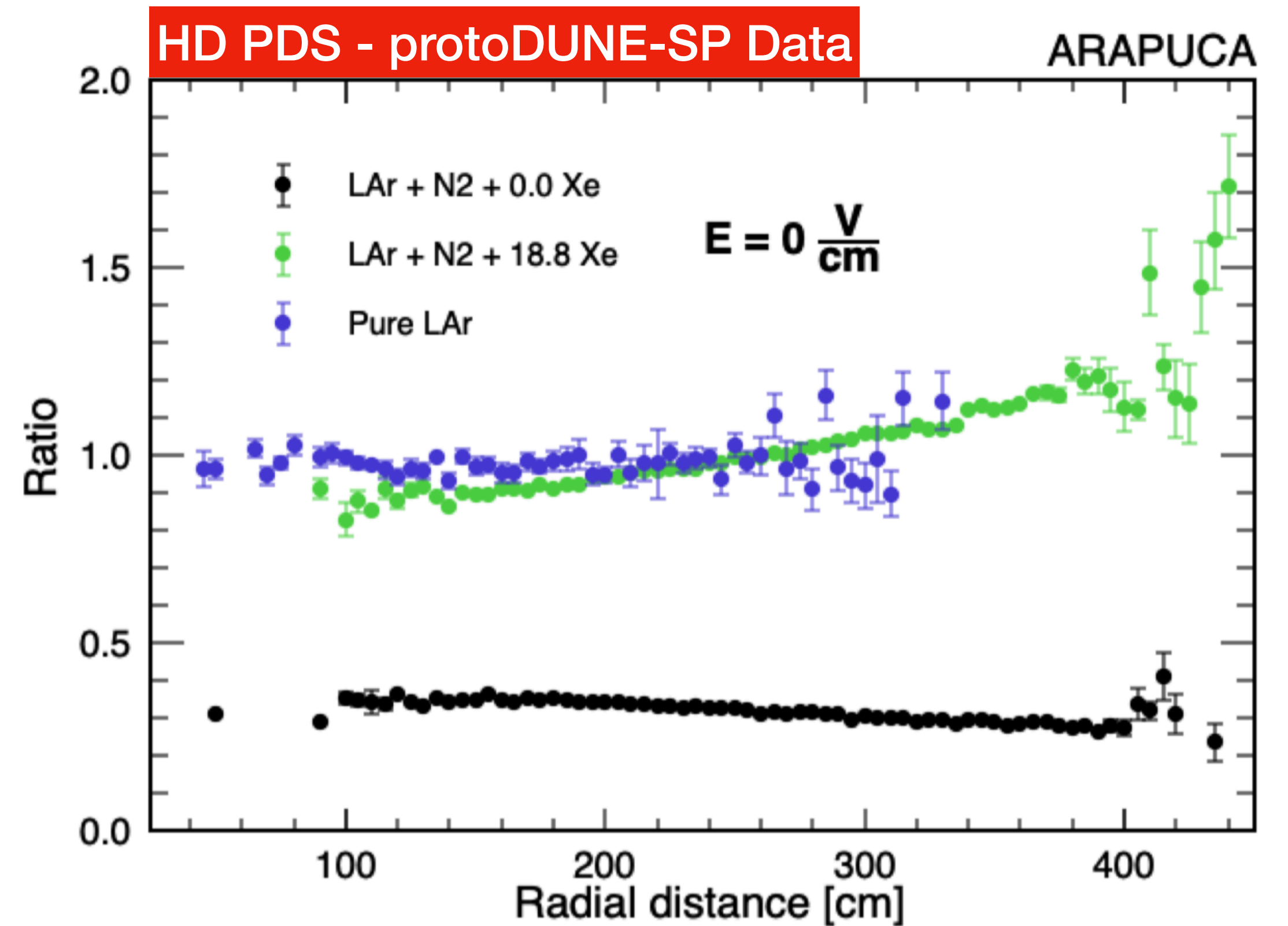
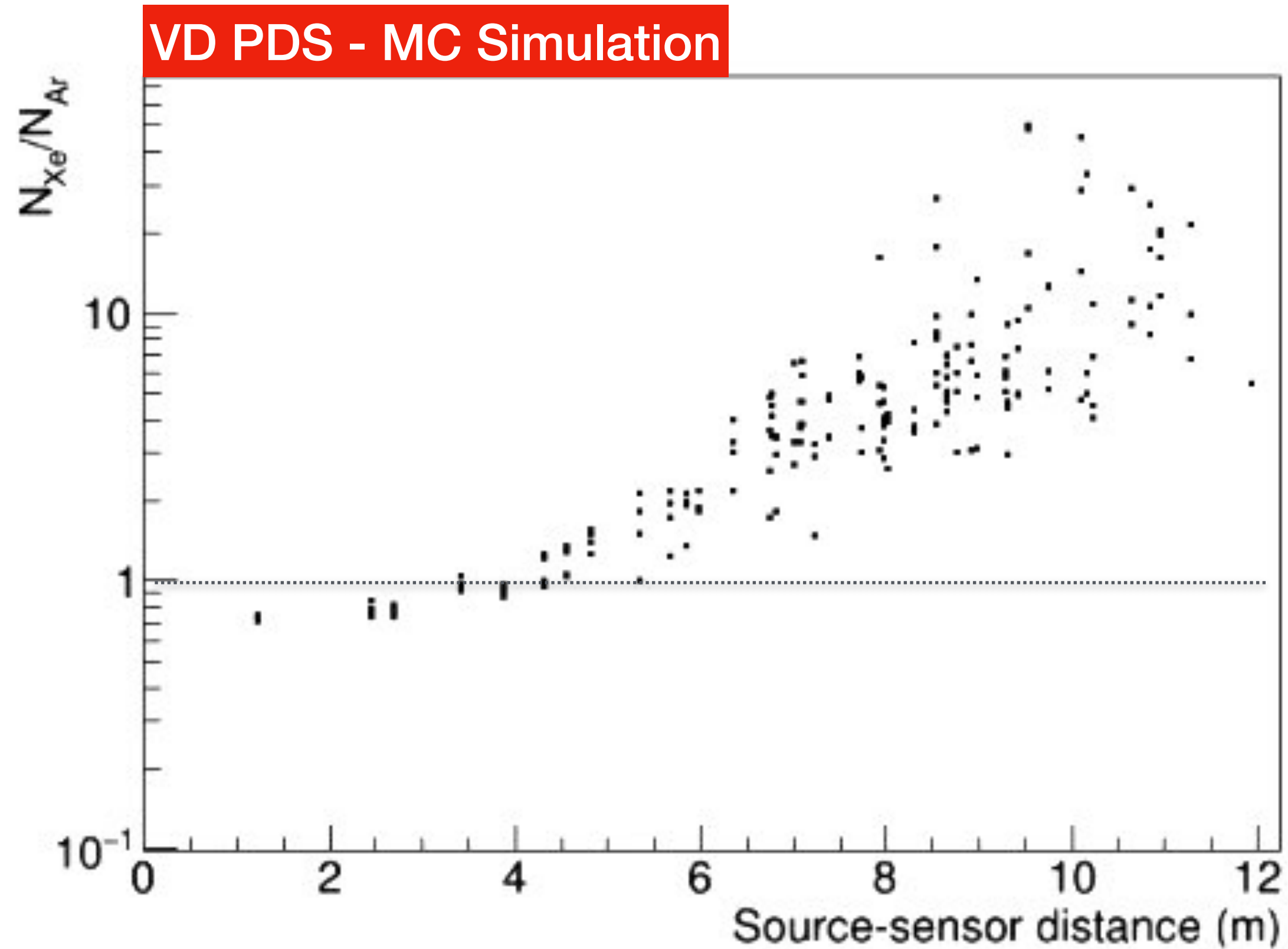
- The all-membrane Backup option is a minor variation of the horizontal drift detector, and as such is already well-developed and carries low risk
- All VD-specific portions of the backup design will be developed as part of the preparations for the reference system.
- The backup design, as well as the reference design, require a more transparent (70%) field cage (FC) for which a solution has been found and will be tested in a dedicated test stand at CERN

Why choose the Cathode & Membrane mounted as the reference design?

- The reference design presents the opportunity to greatly increase the performance of the VD PD system, with a cost no greater than the all-membrane option
- While there are risks associated with the power over fiber and fiber readout required for the reference design, we have a robust R&D plan to address the risks and we have a low-risk backup plan if necessary.

Why choose Xe doping as baseline option?

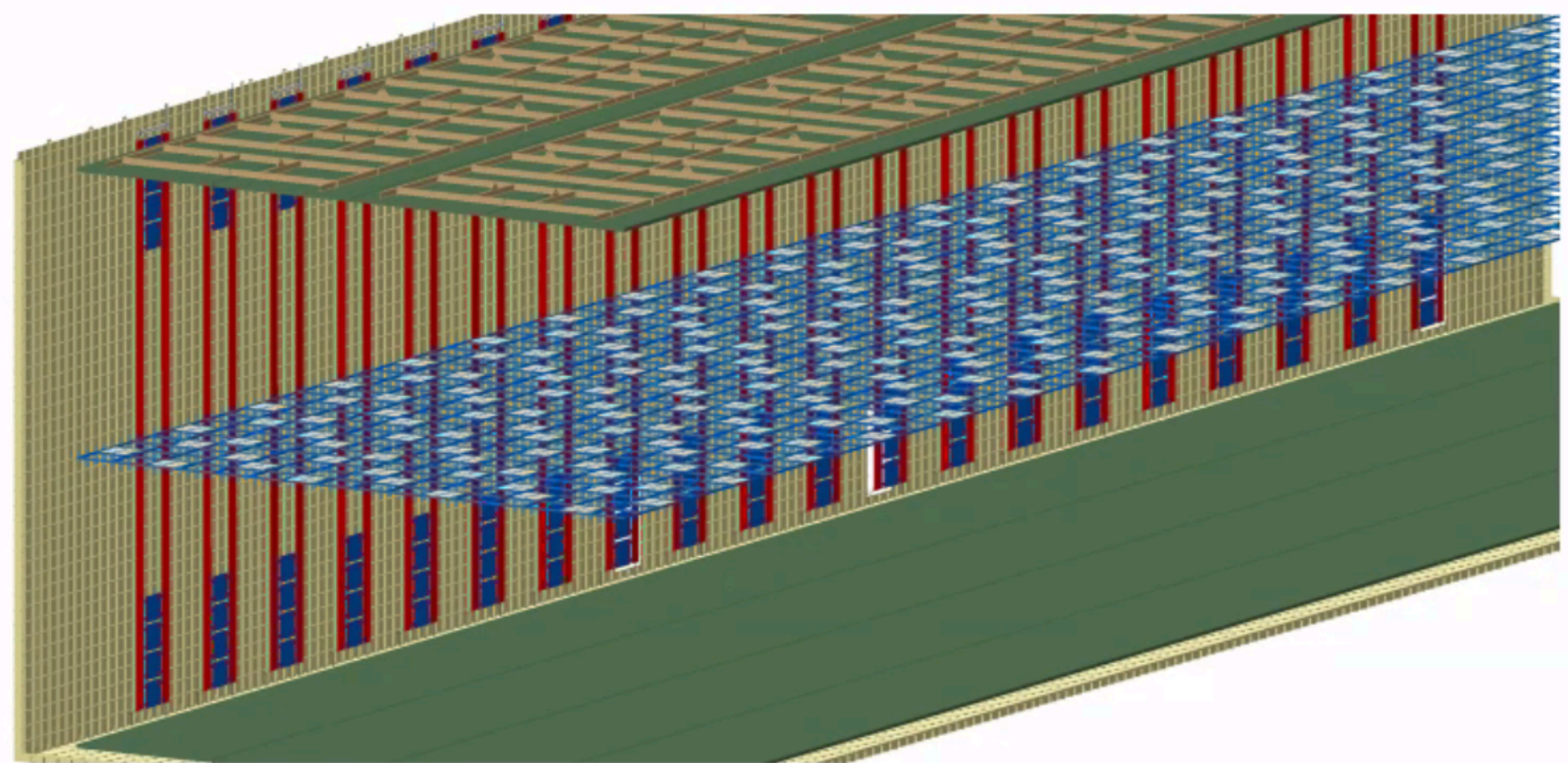
The collected light is found to be larger for Xe-doped Argon, due to the effect of the longer Rayleigh scattering length enhancing collection probability for light emitted at longer distances from the photon-detectors (+30% in VD - from MC simulation)



This supports the choice of Xe-doped Ar as scintillation medium in VD.

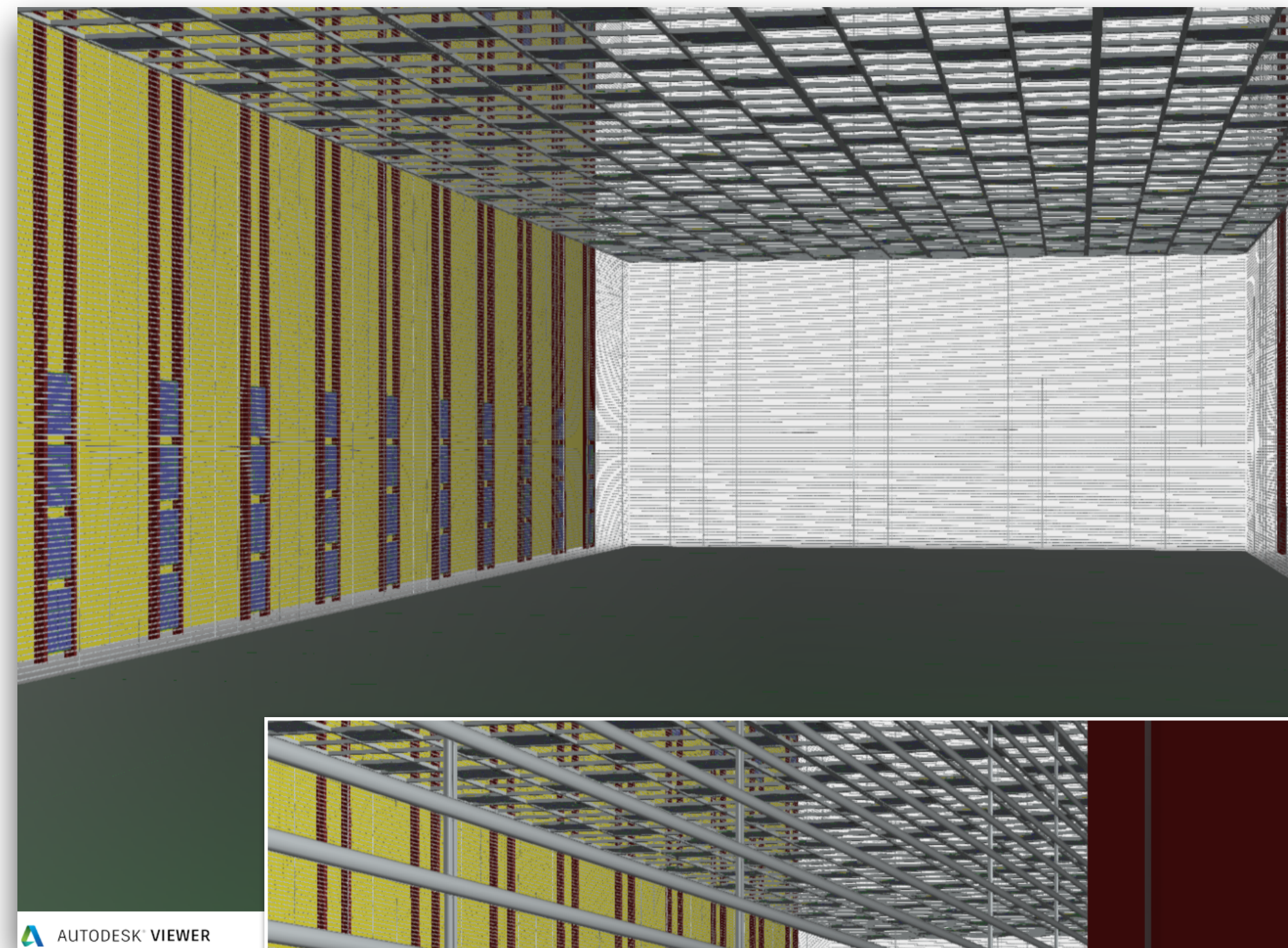
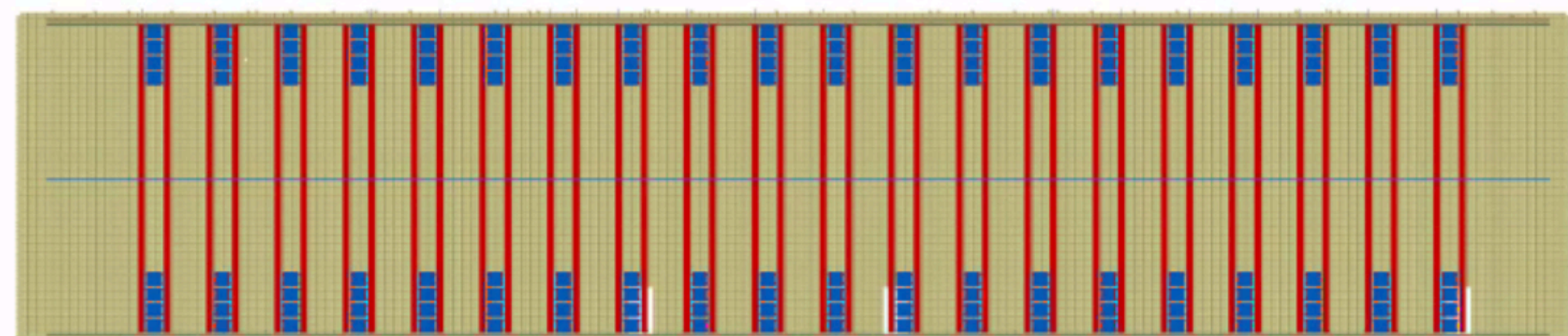
The VD PD Reference Design

Reference Design

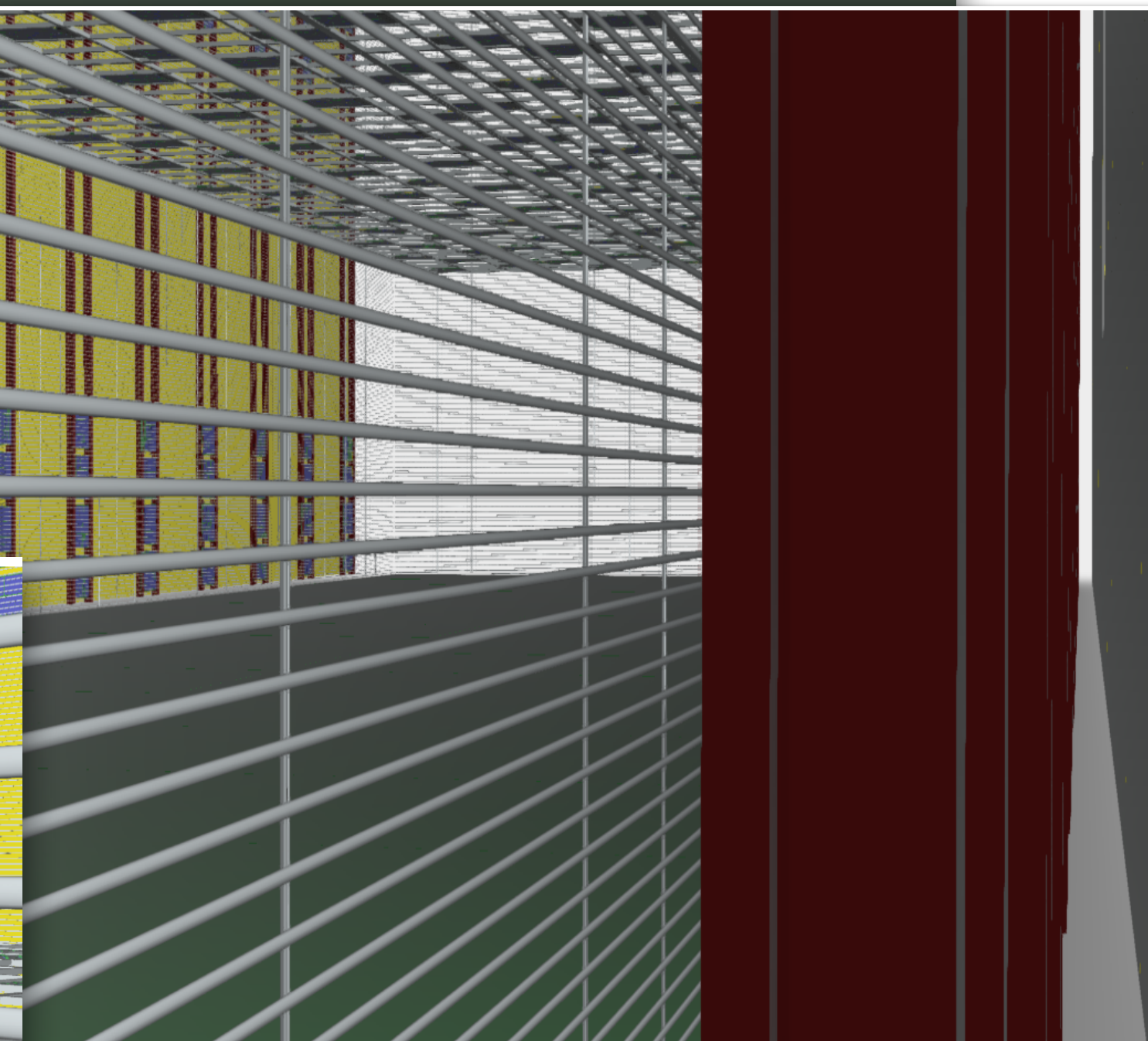
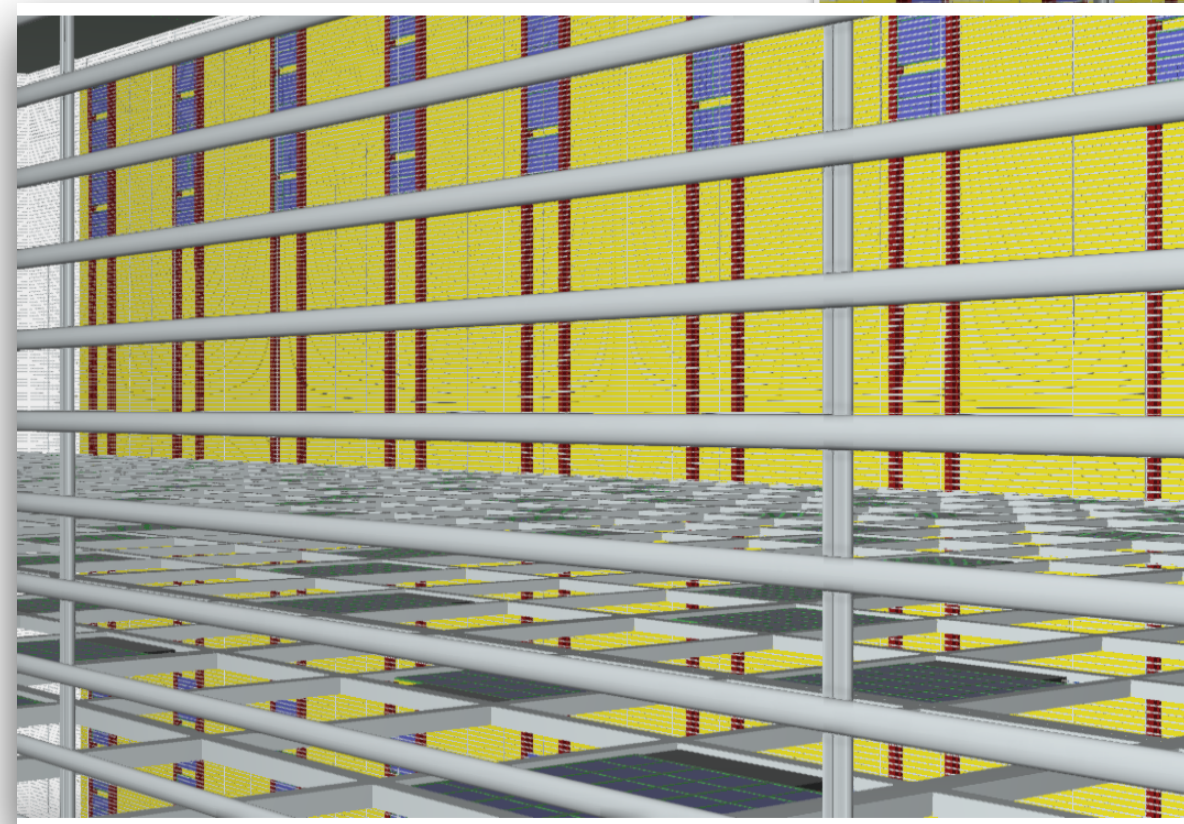


4 pi layout :

- Full trigger capabilities down to 10 MeV
- Energy, Position and T0
- xArapucas 60x60 on the cathode, 115 mq, analog readout
- xArapucas 60x60 on the cryo membrane, ~3m from anode



modified FC - 70% T



Reference design for the VD **PD System**

PD Active Optical Coverage distributed onto **3 sides of the LAr Volume**

(**Cathode side** and 2 Long Membrane Cryostat sides, w/ modified FC - 70% T)

+

PD Passive Optical Coverage (reflector) on the Anode side

+

Xe doping (minimize Rayleigh scatter for light at far distance)

The Reference design endorses the **$\sim 4\pi$ coverage concept (originally suggested in the VD proposal)**:

⇒ good uniformity of response, very low detection & trigger threshold, energy resolution and position resolution capability

- Detailed study of PD impact on LowEn UG Physics (trigger and reconstruction, combined with TPC) is the main goal of the current DUNE Simulation Task Force effort

Simulations

Assuming 24000 photons per MeV of energy deposited (70% for Xe and 30% for Ar) and 3% detection efficiency

Baseline geometry

PDs 60 cm behind FC

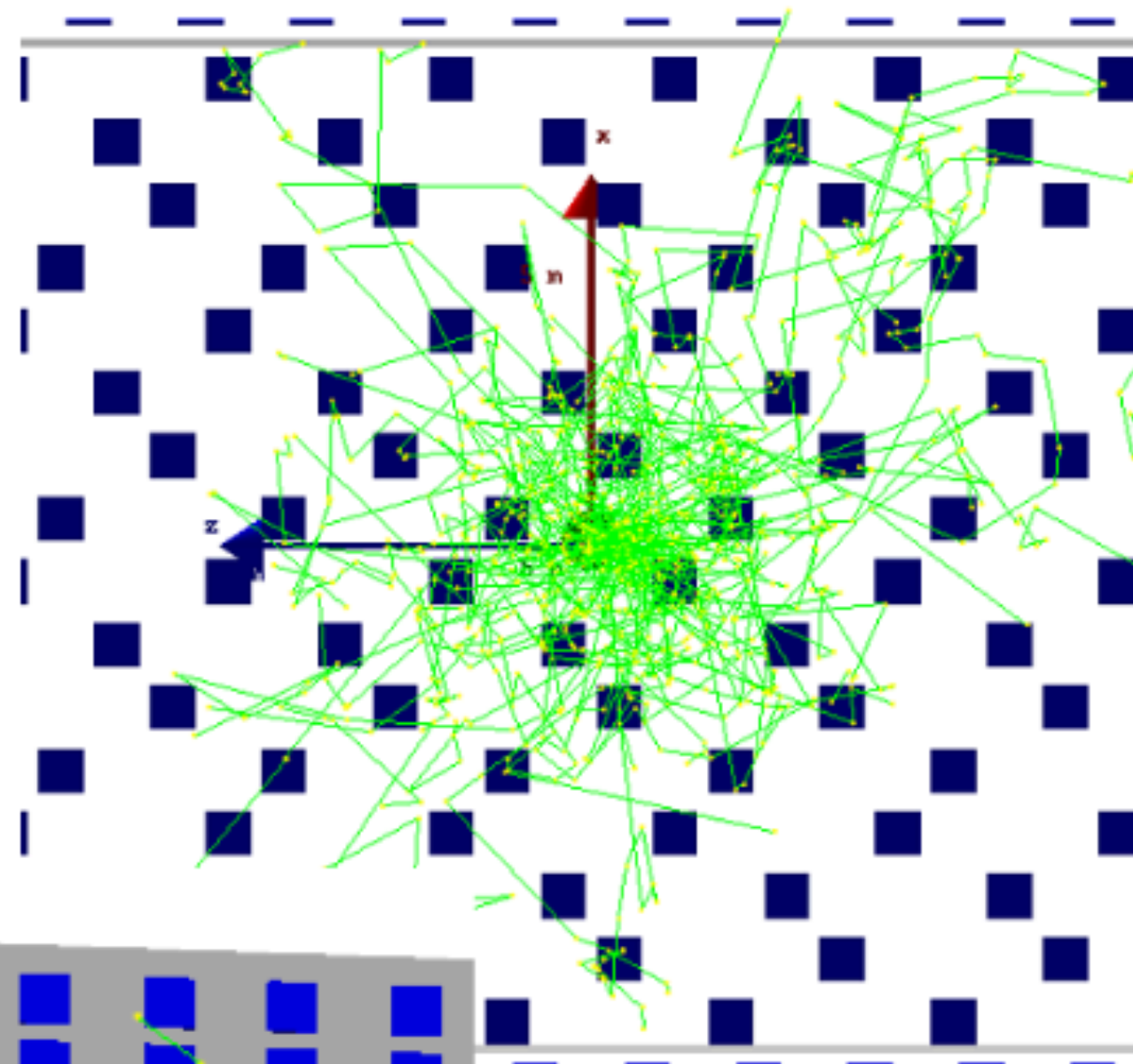
Semi-transparent FC: $T=70\%$

Cathode $T = 80\%$

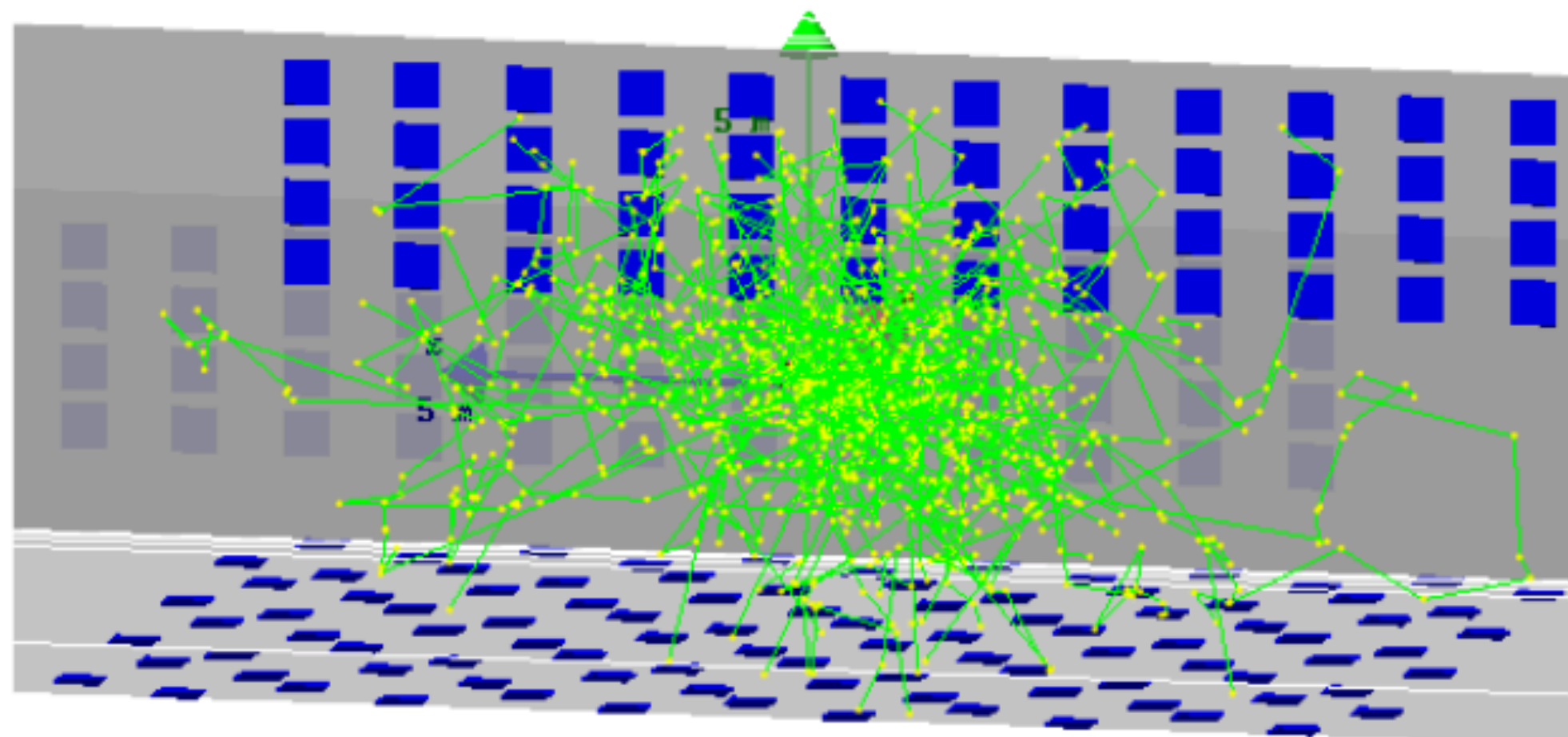
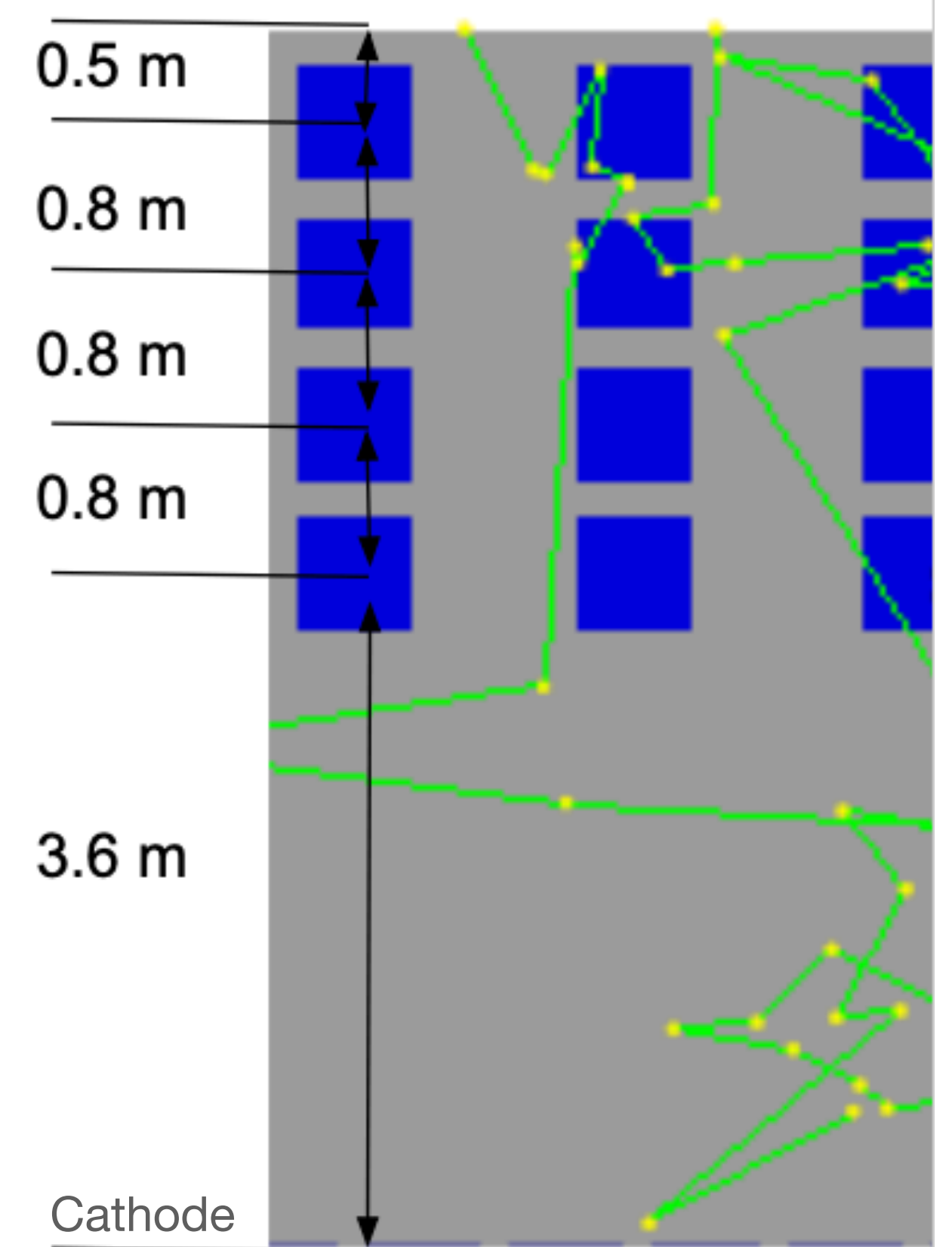
Anode $R=20\%$ (Xe)

$\lambda_{\text{Ar}} = 99.9 \text{ cm}$, $\lambda_{\text{Xe}} = \sim 8.5 \text{ m}$

(Top View) xARAPUCA Tiles on the Cathode

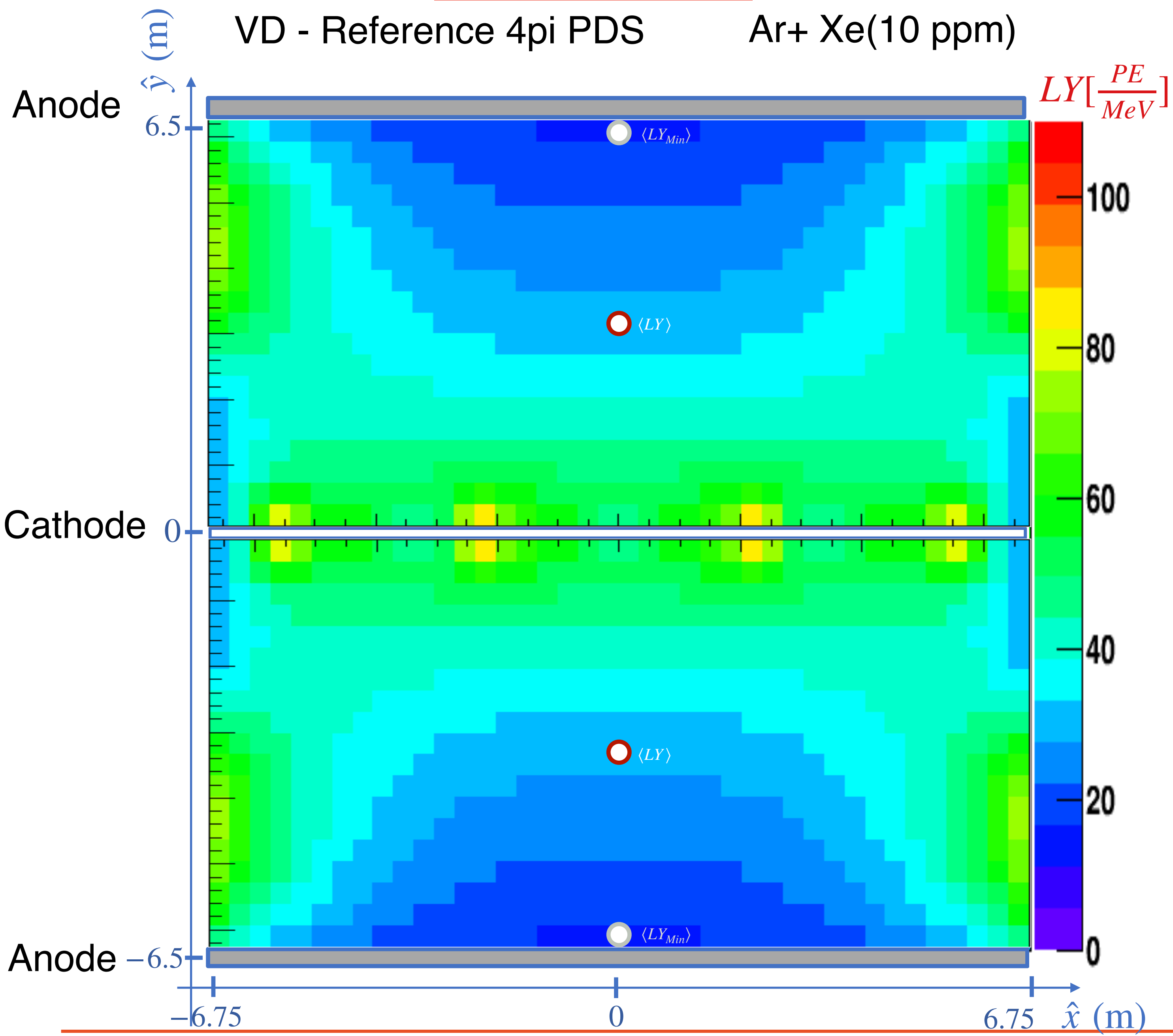


(Side View) xARAPUCA Tiles on the Membrane



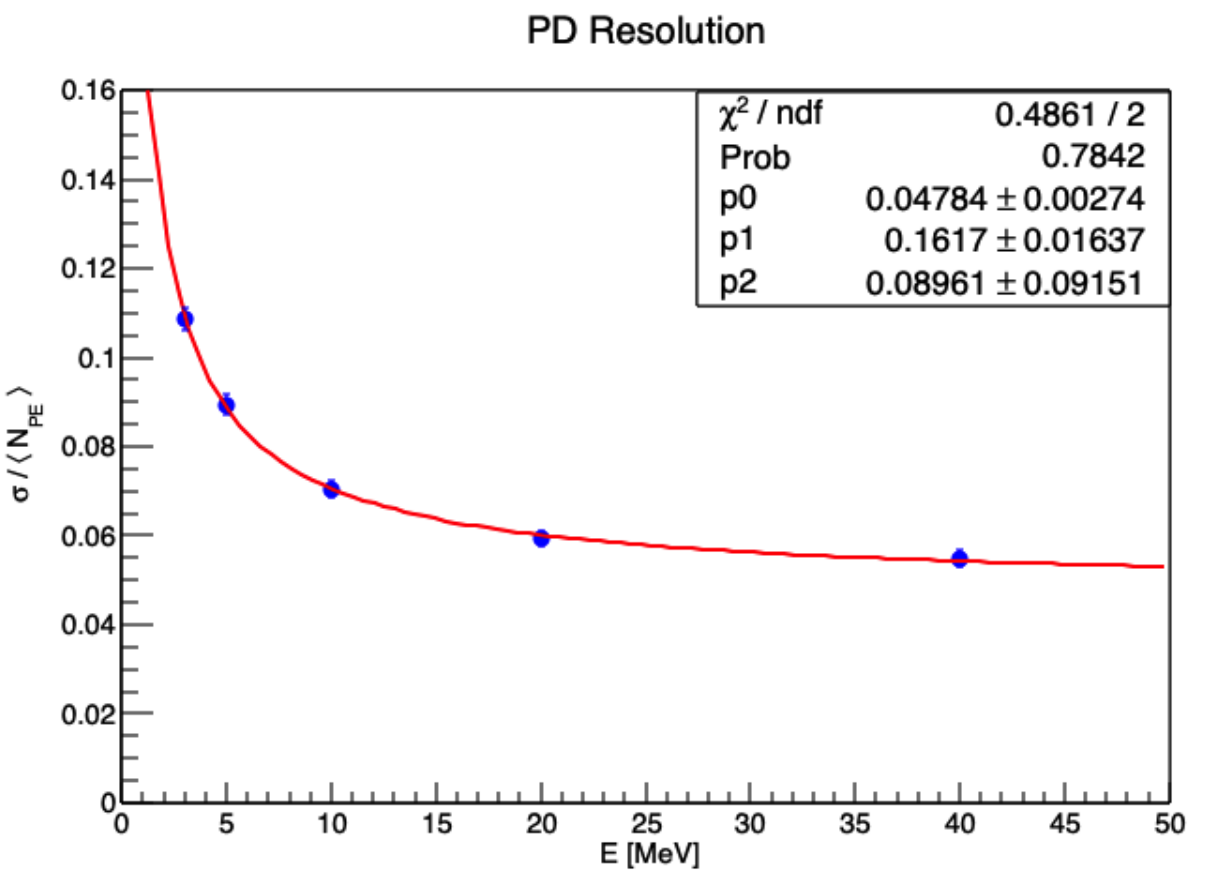
Light Yield (LY) Map

VD - Reference 4pi PDS Ar+ Xe(10 ppm)

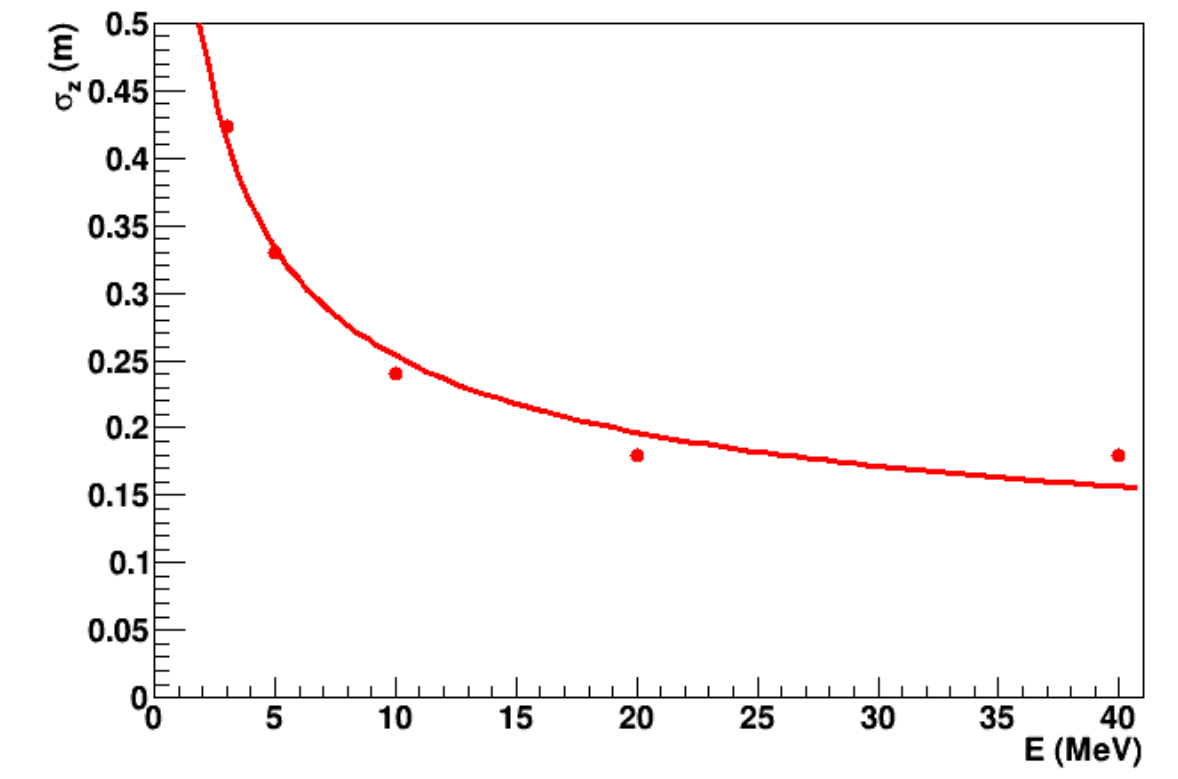


Calorimetric Energy and Position reconstruction from detected photon counting

Energy Resolution
 from statistical fluctuation (p1) on detected PEs, electronics noise (p2) and uncertainty on energy calibration (p0)



Position Resolution
 from detected PEs barycenter determination.



- $\langle LY \rangle = 38 \text{ PE/MeV}$
- $\langle LY_{Min} \rangle = 16.5 \text{ PE/MeV}$

Light Yield: **Ar + Xe** and different **anode reflection**

Assuming 25000 photons per MeV of energy deposited (19000 for Xe and 6000 for LAr) and 3% detection efficiency. Anode reflectivity for Xe light.

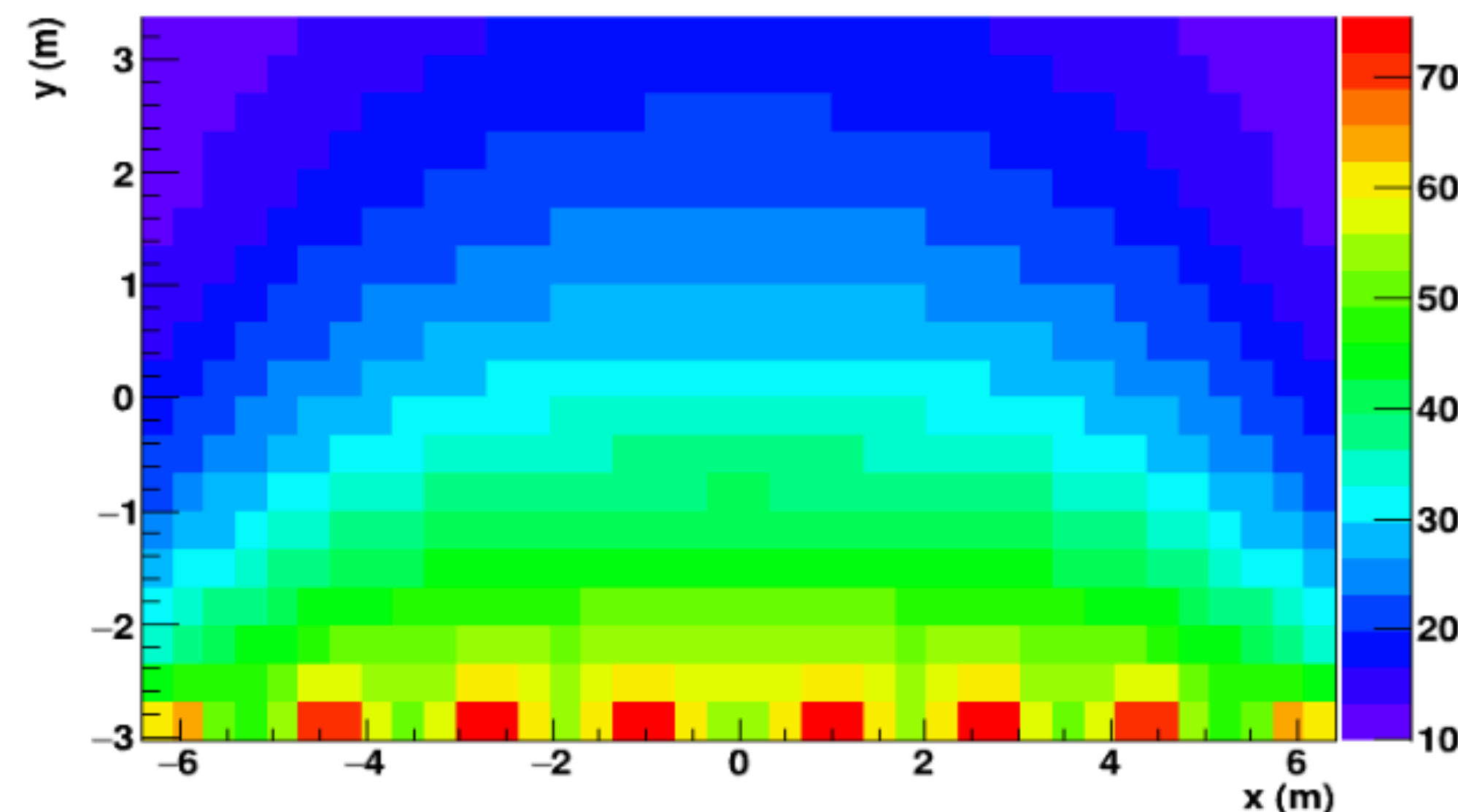
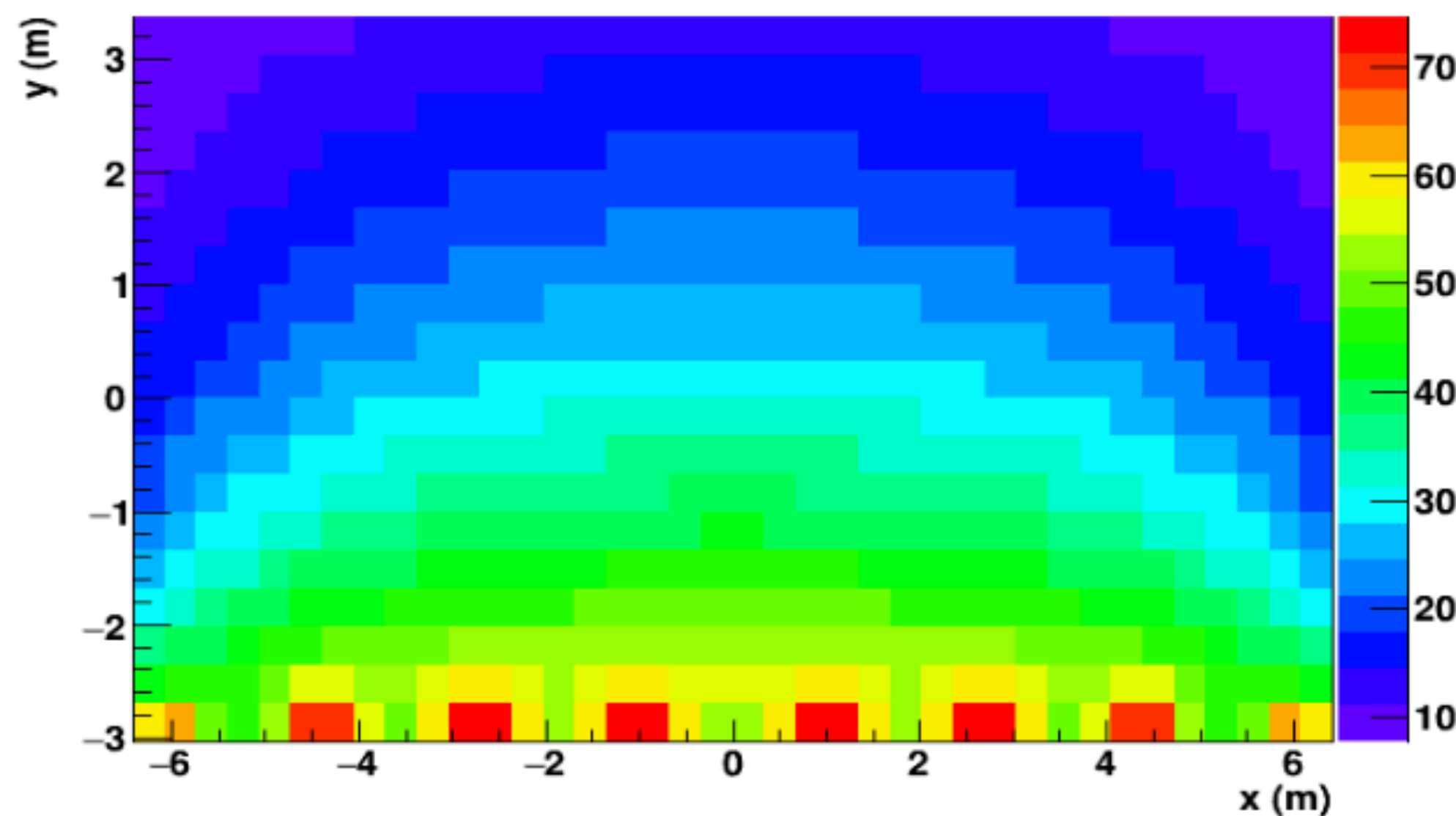
<LY> up ~ 5.9%

<LY> = 29.0
<LY_min> = 7.7

<LY> = 30.7
<LY_min> = 9.9

Pe per MeV

Pe per MeV



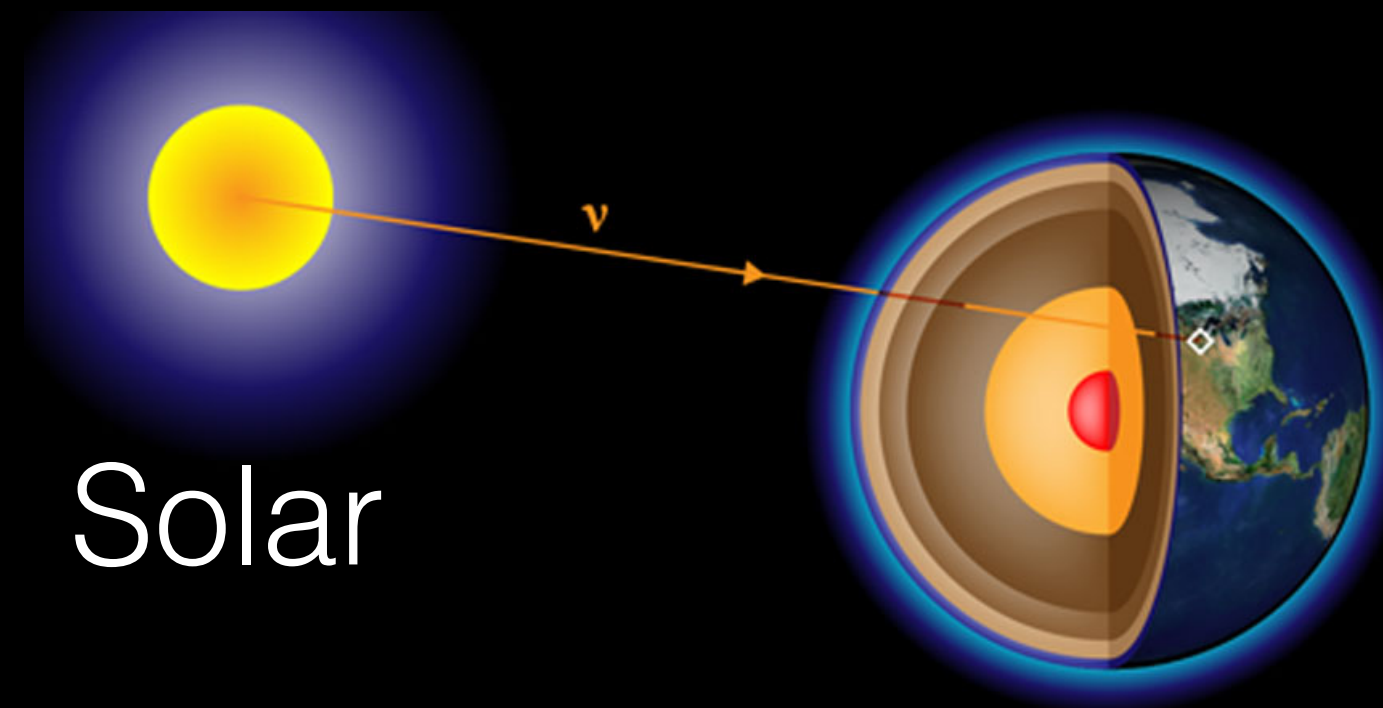
R = 25%

R = 50%

Cathode: T = 80%

LY Response from Cathode ONLY

Enlarging the DUNE Physics Scope



VD
PDS

- CoreCollapse SN is the most spectacular phenomenon in Nature and is imprinted in neutrino signal
- Low energy UG neutrinos opened discovery space in particle and astro-particle physics
- *It is critical to DUNE Science Program to succeed at measuring low energies rare UG neutrinos*
- *It is is critical to lower Trigger E-threshold to extend range of SN detection (toward and beyond Galaxy edge).*
- *It is critical to guarantee good Time resolution and improve Energy resolution for SN-signatures in time & energy spectra*

SuperNova

Reference Design Cathode + 40% Membrane Cost Splits

Table 4: VD 4π PDS Reference Configuration

	Quantity	Surface Type
X-ARAPUCA Tiles	640	320 double-side [Cathode Plane] 320 single-side [Membrane Two Long Walls]
Dichroic Filters	34,560	
WLS plates	640	
PhotoSensors (SiPM)	102,400	51,200 [Cathode plane] 51,200 [Membrane Two Long Walls]
Read-out Channels	640	320 [Cathode plane] 320 [Membrane Two Long Walls]
SiPMs per channel	160	[Cathode plane]
	160	[Field Cage walls]
Total Optical Area	346 m ²	115 m ² + 115 m ² [Cathode Plane] 58 m ² + 58 m ² [Membrane Long Walls]
Active coverage	14%	[Cathode Plane]
	8%	[Membrane Long Walls]
	0%	[Membrane Short Walls]

- R&D FY21
 - \$0.8M labor \$0.2M M&S
- Prototype and long-term validation
 - \$0.5M labor \$0.2M M&S
- ProtoDUNE2 1/20th scale Pilot
 - \$0.3M labor \$0.7M M&S
- Production
 - \$2.8M labor \$6.3M M&S
- **Total Reference Design: \$10.8 M**

Vertical Drift Photon Detector System Summary		
Item	Cost/Each	Cost/System
Cathode PDS		
Cathode Mount Tiles	\$ 6,220	\$ 1,990,272
Cathode Tile Mount Electronics	\$ 4,200	\$ 336,000
Cathode Non-Tile Mount Electronics	\$ 2,500	\$ 100,000
Cathode Warm Electronics	\$ 30,000	\$ 60,000
Cathode Power-over-Fiber	\$ 1,320	\$ 422,507
Total Cathode System		\$ 2,908,779
HD-based Cathode Calibration/Monitoring System		\$ 282,236

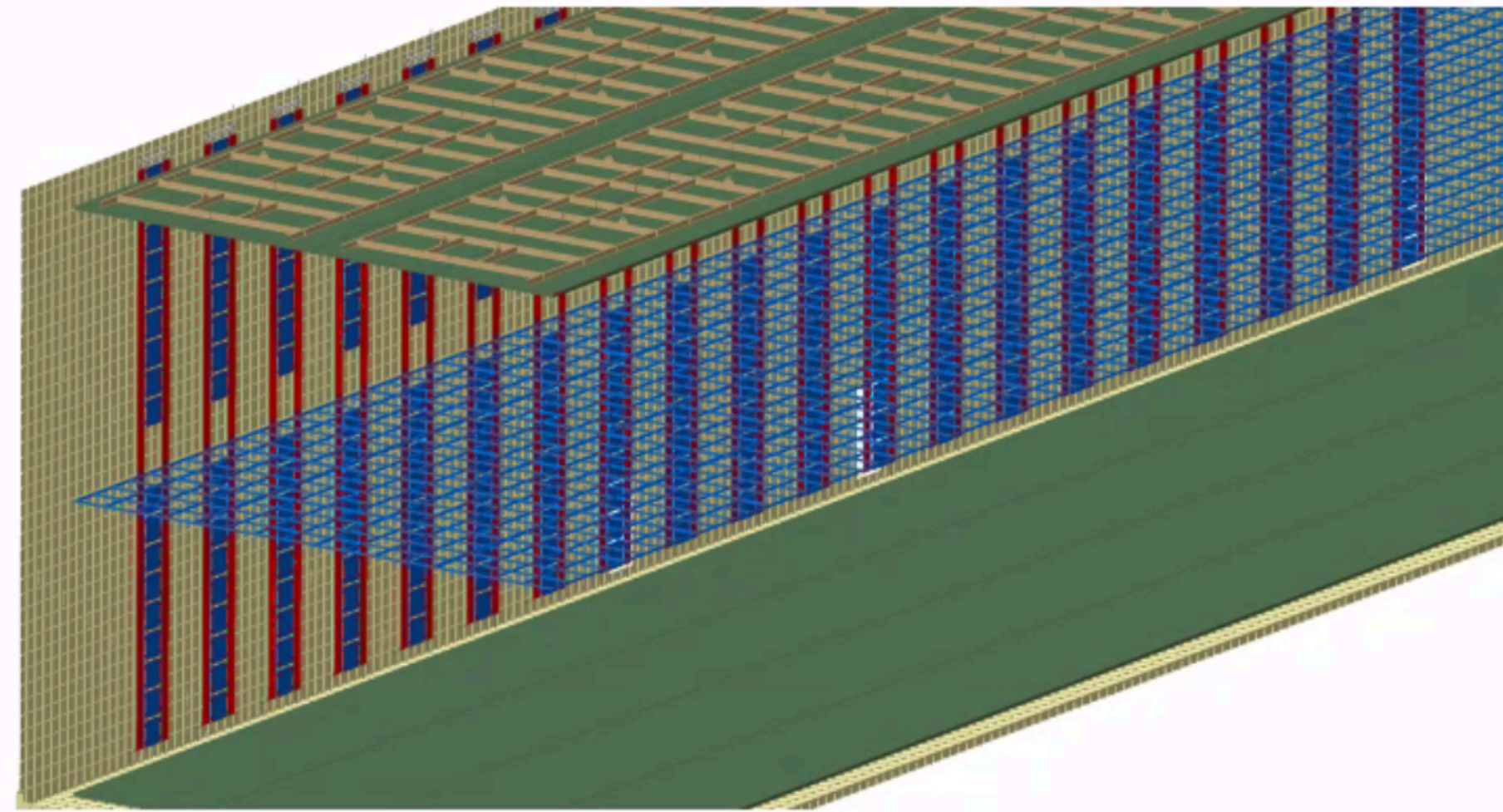
Cathode contribution of core production M&S (i.e. \$3.3M):

40% membrane (320 tiles) core production M&S (i.e. \$2.8M)

Membrane Electronics Cost:	\$ 578,000
Membrane Detector Cost:	\$ 1,633,536
Membrane Warm Electronics Cost:	\$ 216,000
Total Membrane M&S:	\$ 2,427,536

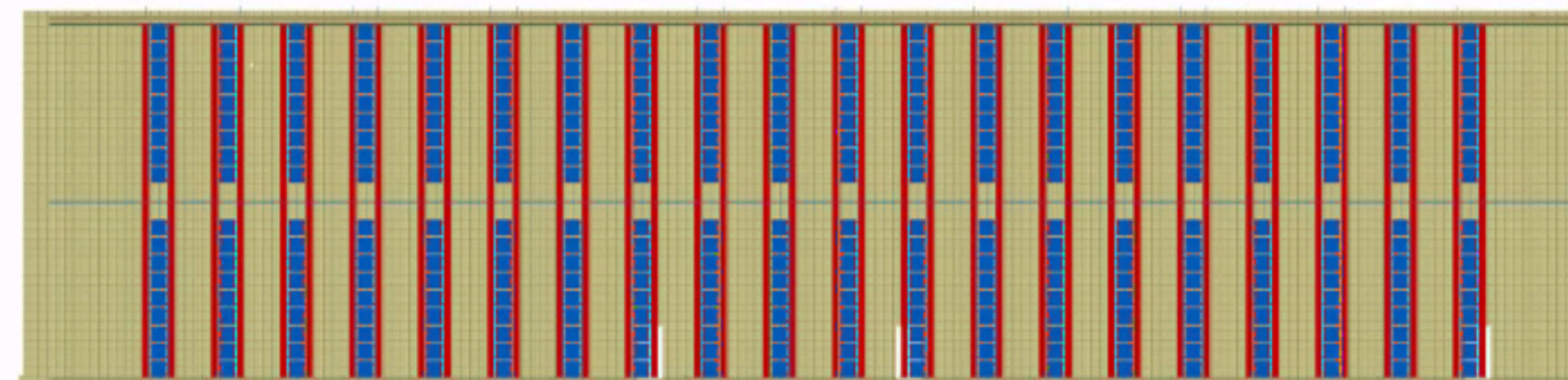
Production M&S of **Cathode+40% membrane** is \$6M + travel costs and test stands and production infrastructure = **\$6.3M**

The VD PDS Backup Design



Minimal layout:

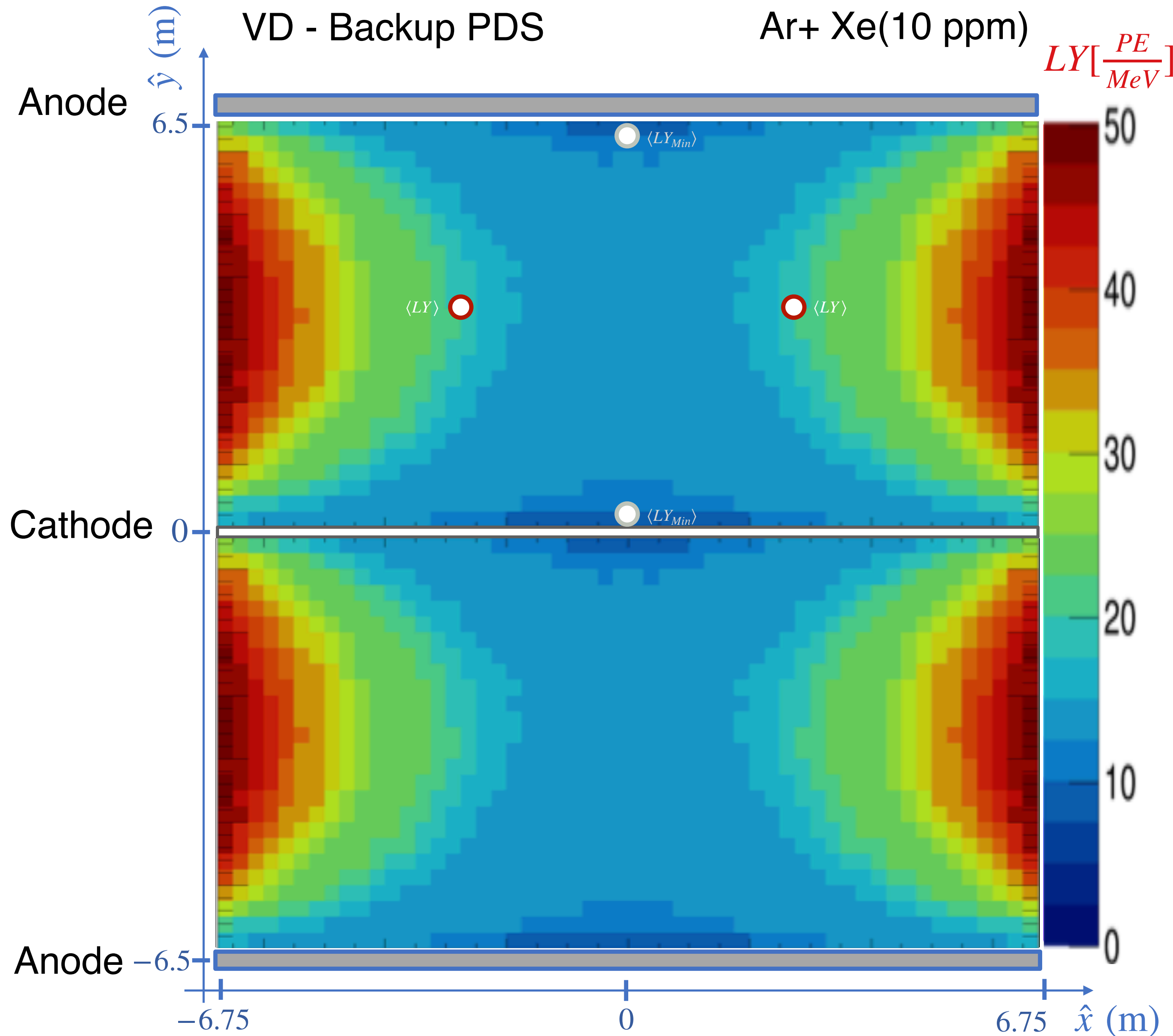
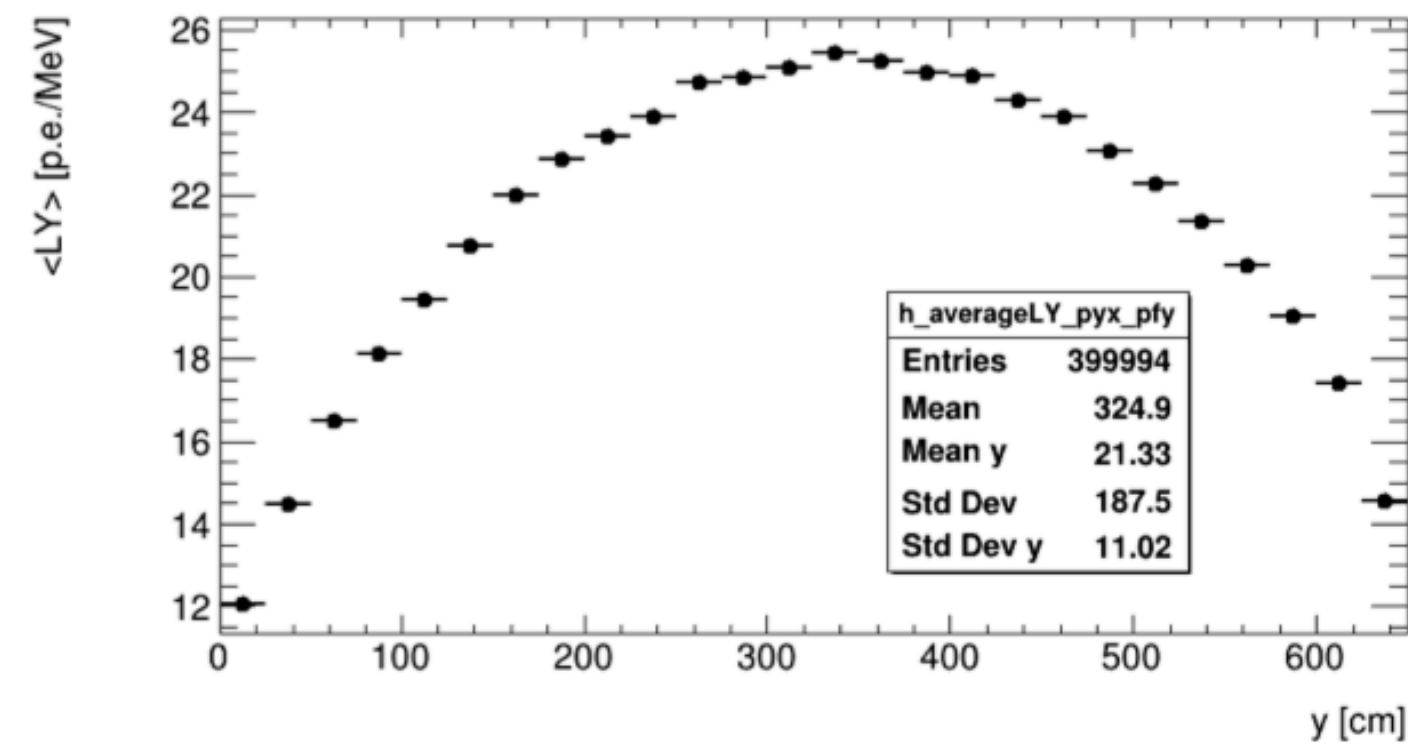
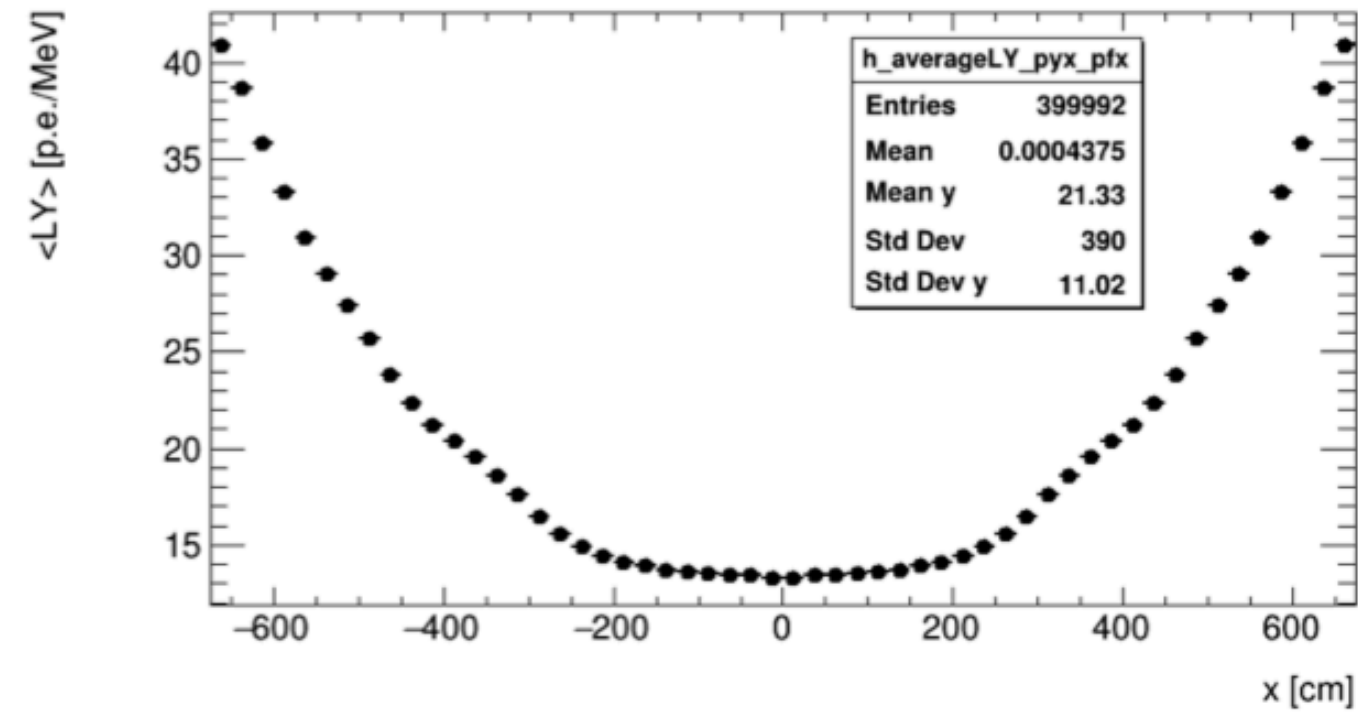
- Trigger via charge TPC readout down to 10 MeV
- T0, (E)
- xArapucas 60x60 on the cryo membrane, 20 columns, each column 18 xArapucas, SPHD readout



Simulation (FLUKA)

Assuming 24000 photons per MeV of energy deposited (70% for Xe and 30% for Ar) and 3.5% detection efficiency

- Integrated over all Z positions (includes edge effects)
- $\langle LY \rangle = 21.3 \text{ p.e./MeV}$
- $\langle LY \rangle_{min} = 7.7 \text{ p.e./MeV}$



Membrane-only Cost Splits

Table 5: VD PDS Backup Configuration

	Quantity	Surface Type
X-ARAPUCA Tiles	720	single-side [Membrane Two Long Walls]
Dichroic Filters	25,920	[all-Membrane Two Long Walls]
WLS plates	6720	
PhotoSensors (SiPM)	115,200	
Read-out Channels	720	[all-Membrane Two Long Walls]
SiPMs per channel	160	
Total Optical Area	260 m ²	130 m ² + 130 m ² [Membrane Long Walls]
Active coverage	15 %	[Membrane Long Walls]
	0%	[Membrane Short Walls]

- Prototype and long-term validation
 - \$0.3M labor \$0.1M M&S
- ProtoDUNE2 1/20th scale Pilot
 - \$0.3M labor \$0.6M M&S
- Production
 - \$3.1M labor \$6.1M M&S
- **Total Backup Design: \$10.5 M**

Membrane-only contribution of core production M&S (i.e. \$5.7M)

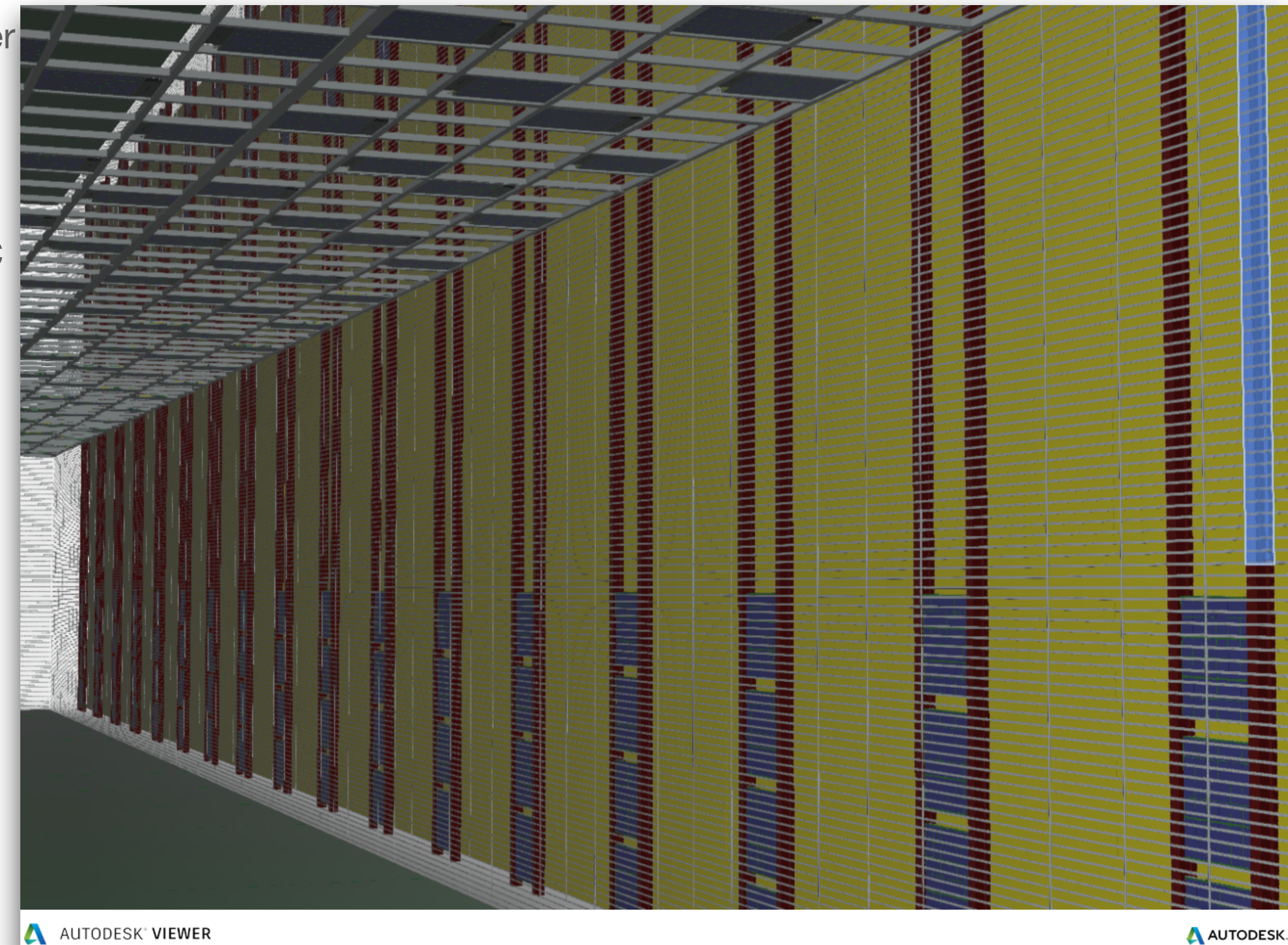
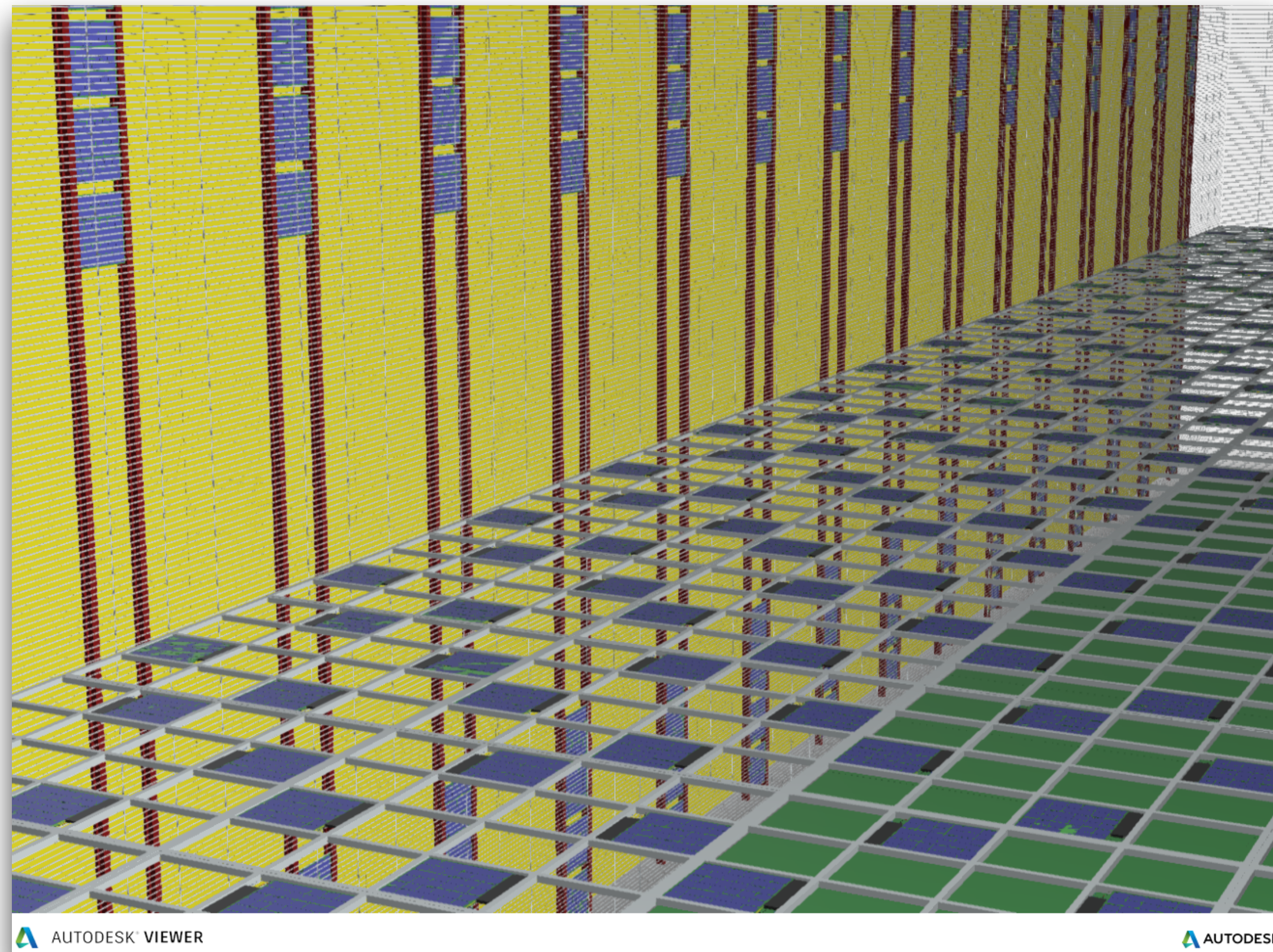
Membrane Electronics Cost:	\$ 1,300,500
Membrane Detector Cost:	\$ 3,675,456
Membrane Warm Electronics Cost:	\$ 430,000
Total Membrane M&S:	\$ 5,405,956

+ travel costs and test stands and production infrastructure = **\$6.1M**

The R&D phase for the Reference PD design

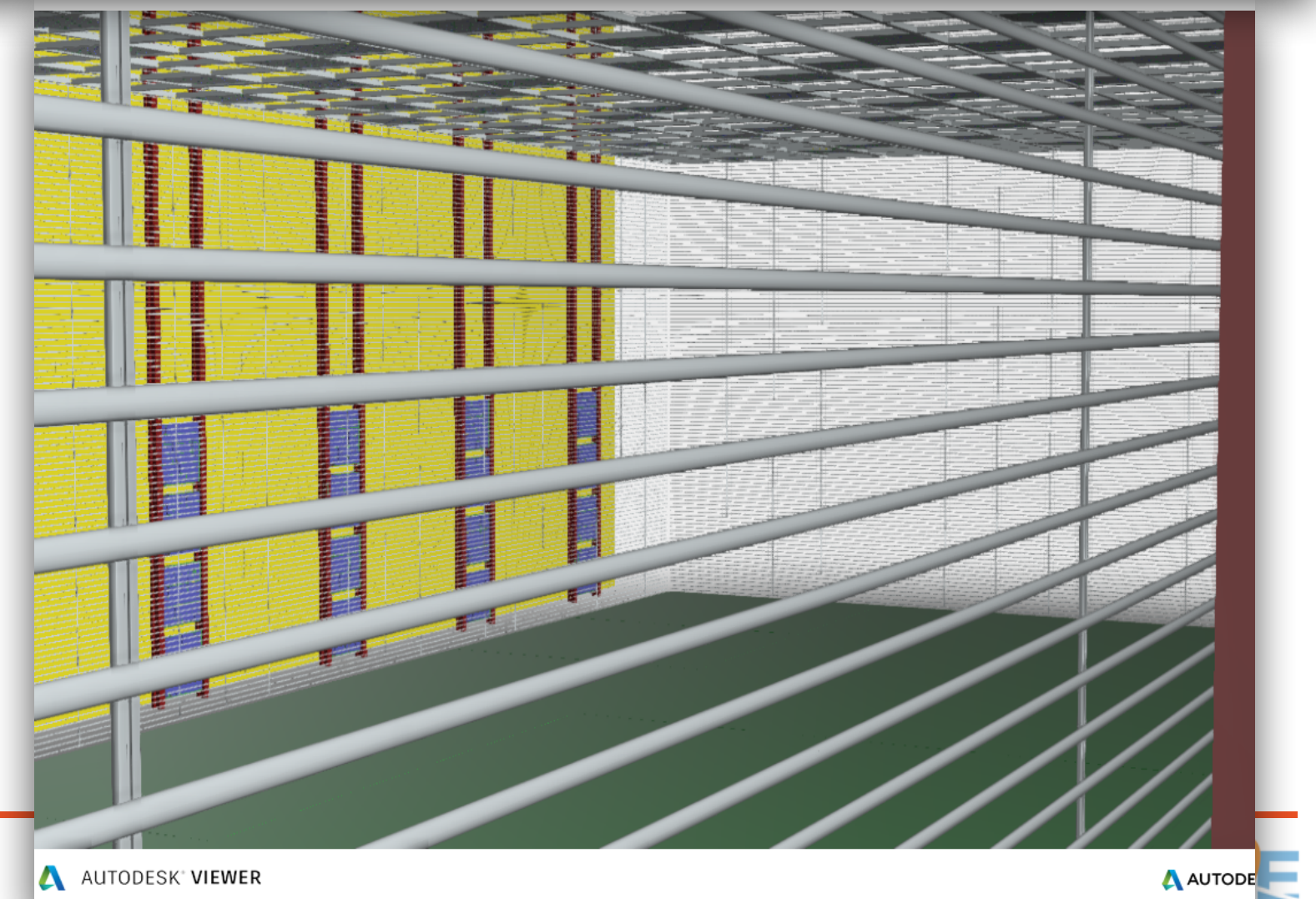
View from inside the Lower
Volume with PD
instrumented Cathode
(above)
and PD instrumented
Membrane behind the FC

View from inside the Upper Volume with PD instrumented Cathode (below)
and PD instrumented Membrane behind the FC



modified FC - 70% T

View of the Lower Volume
from behind the FC, as seen
by the Membrane PD
modules



Operating PD on HV surface (Cathode) requires

electrically floating Photo-sensors and r/o Electronics

⇒ **Power (IN) and Signal (OUT) transmitted via non-conductive cables (e.g. optical fibers)**

⇒ **none of the commercially available technologies (PoF and optolinks) is rated to operate in Cold (at LAr Temperature)**

A highly specialized R&D has been launched (mid Feb.'21) and is currently ongoing to validate COTS technology in Cold

or

develop Cold custom technology for this application

Boundary conditions for VD PD on HV surface

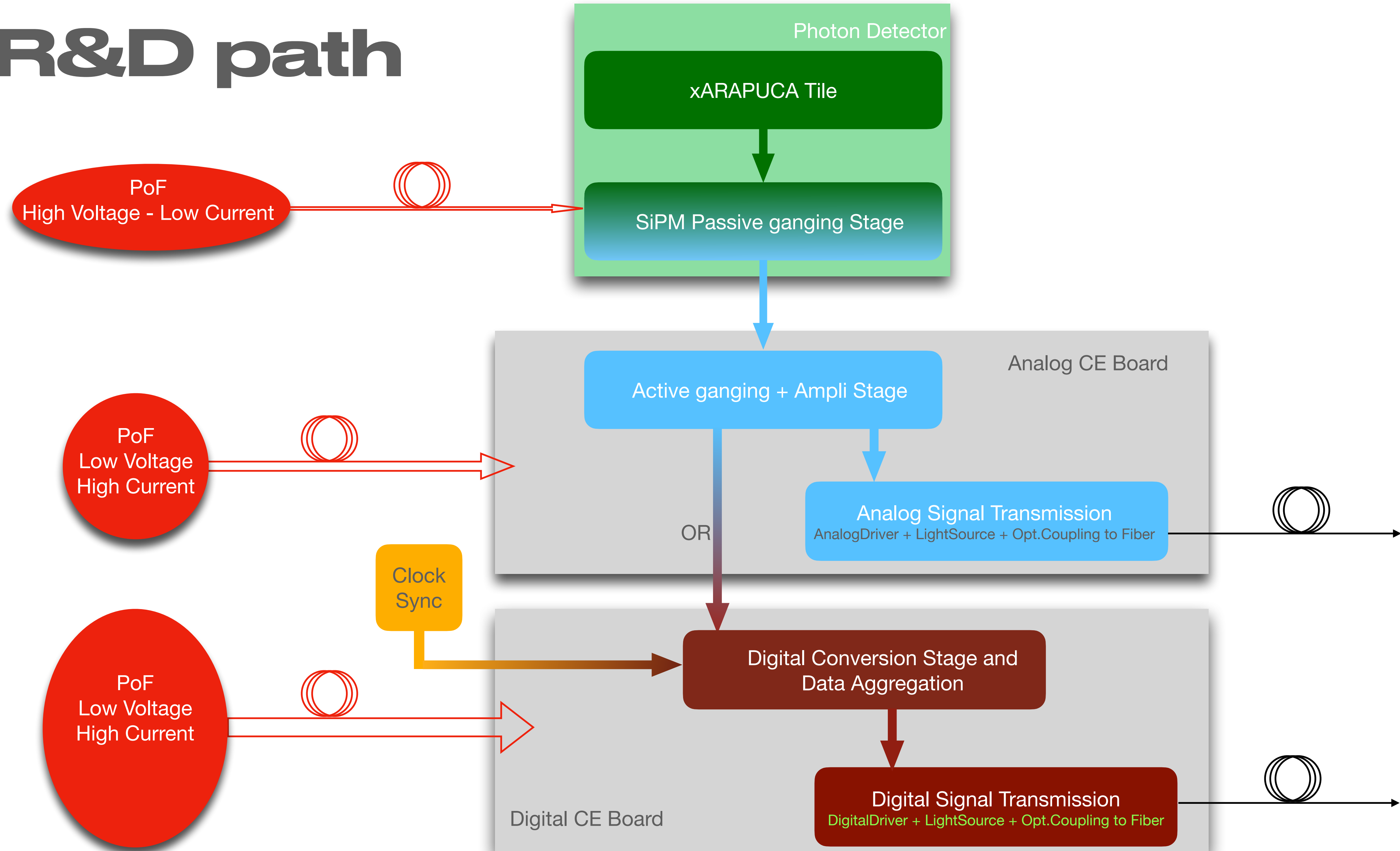
⇒ **Power budget and limitation for power dissipation in LAr**

⇒ **Cost envelop for VD PD**

[with baseline plan of substantial part of the “cathode” mounting scheme in DUNE-US Project]

⇒ **Creation of a new PD community from US, EU and International, within
the existing DUNE PD Consortium**

The R&D path



2021 R&D Strategy

- **Team of experts launched on each component:**

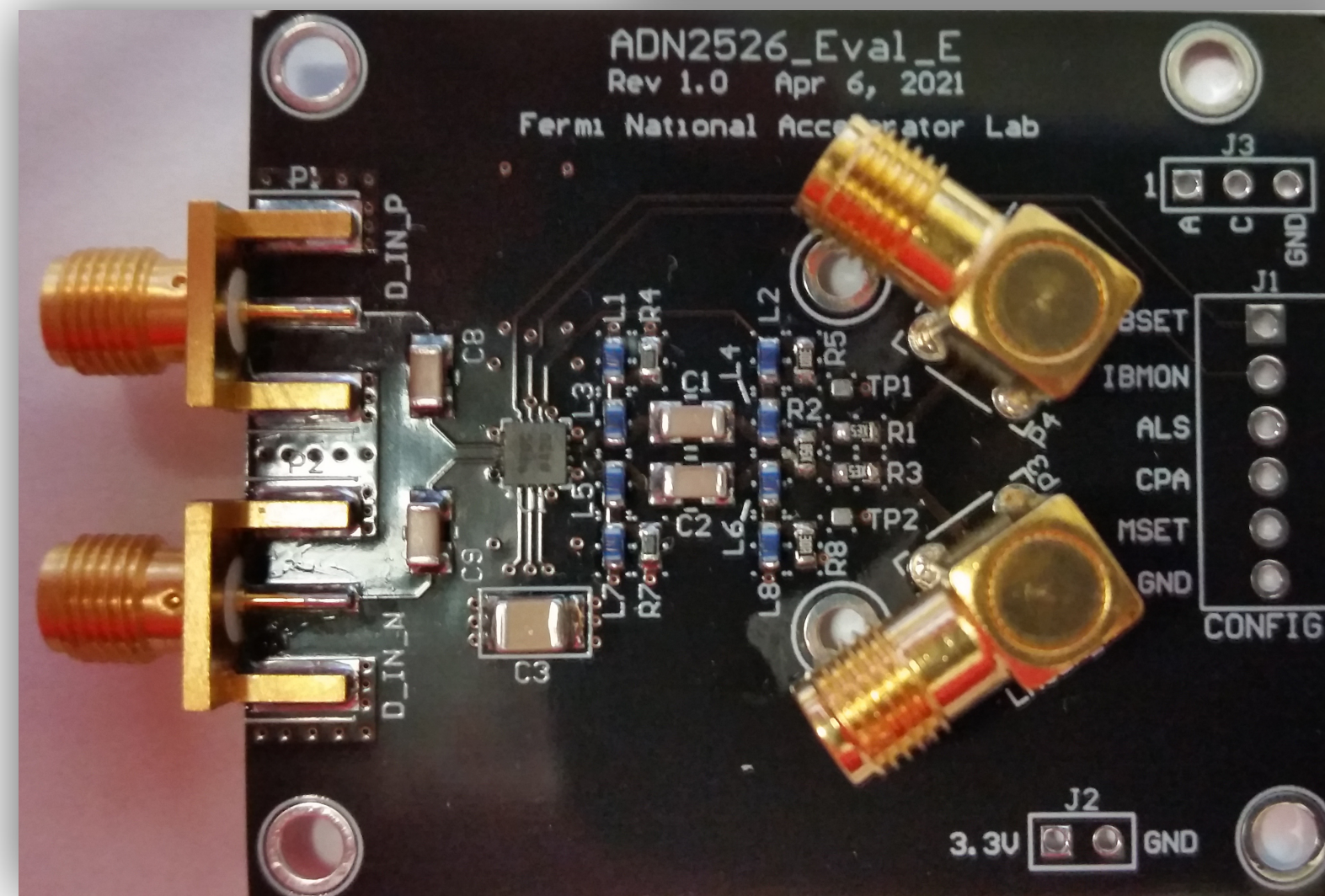
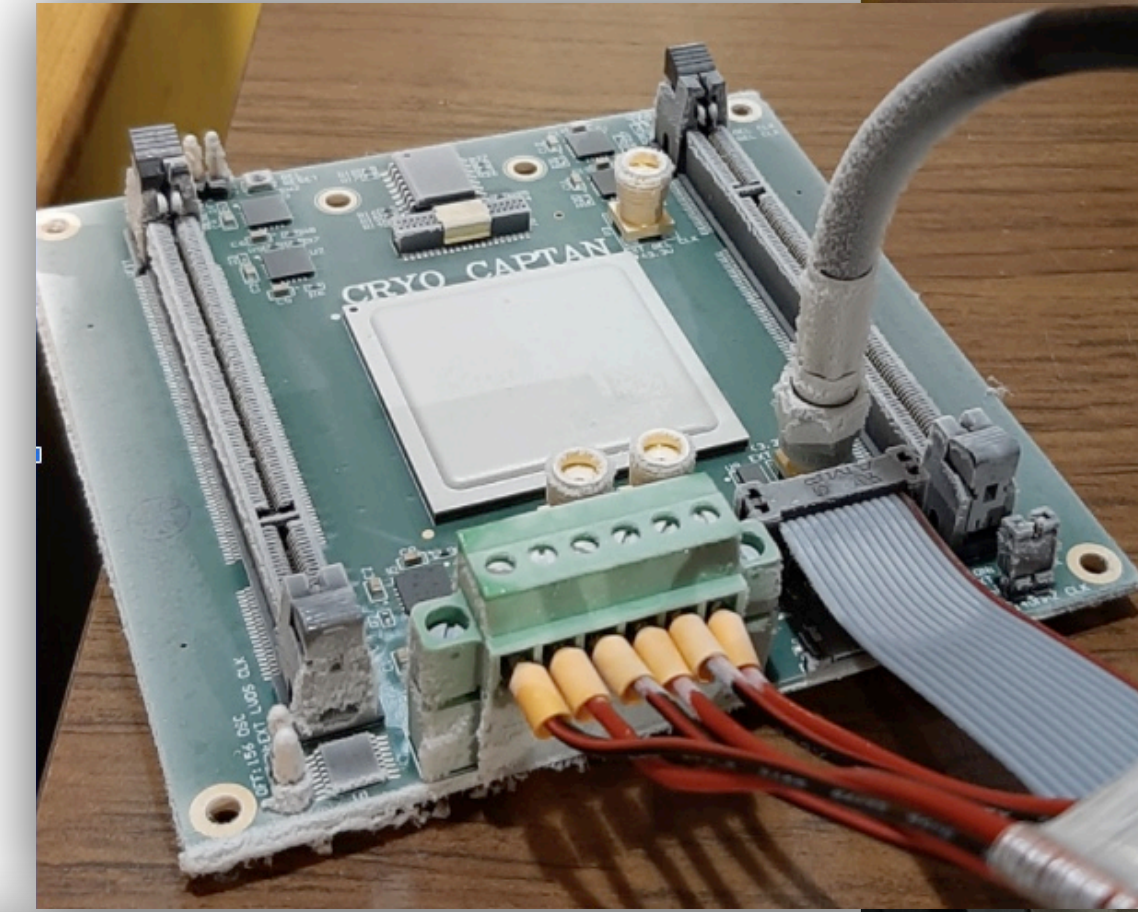
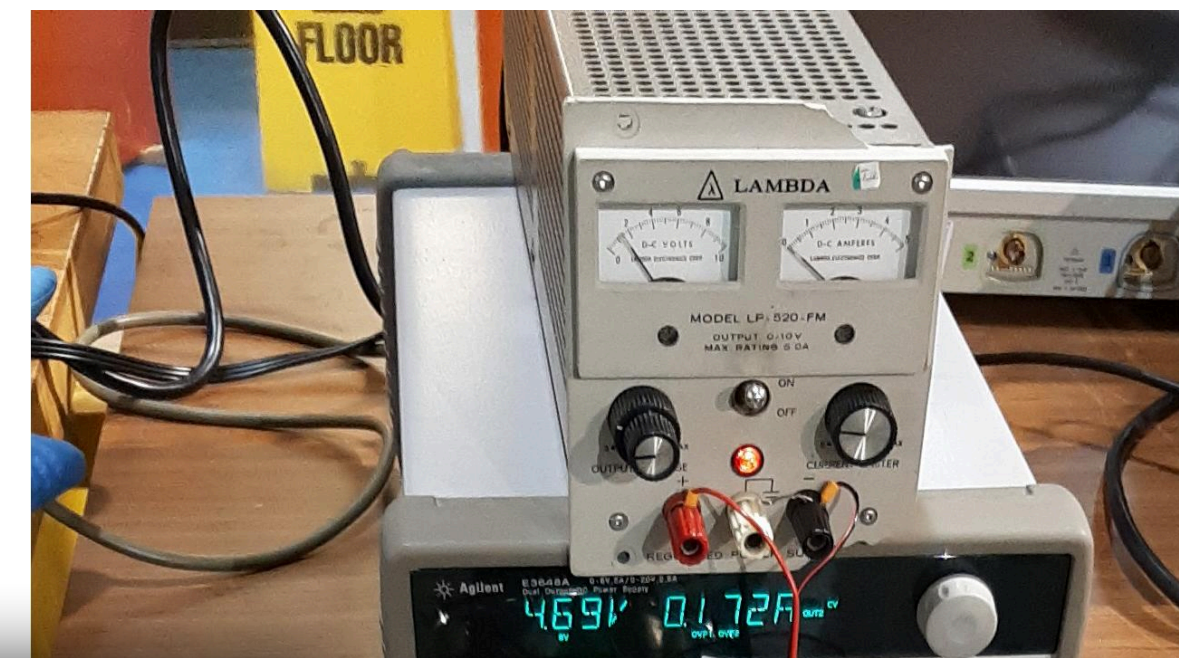
- xARAPUCA Detector Prototype
- Power over Fiber Solutions
- Passive Ganging Stage
- Active Ganging + Ampli Stage
- Analog Transmitter
- ADC
- FPGA
- Digital Transmitter (Tx)
- Control Receiver (Rx)
- Sync Distribution

- **Short-term: component cold tests (on-going) and CE board prototype integration (in progress) and tests**

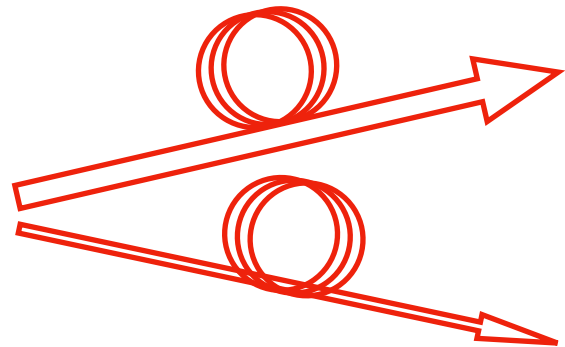
- **Targeting two prototypes for end-of-year CERN Cold Box Tests**

- **Leaving for FY22...**

- CE Packaging optimization
- Power consumption optimization
- Long-term (30-year) cold studies
- xARAPUCA optimization for Xe light collection

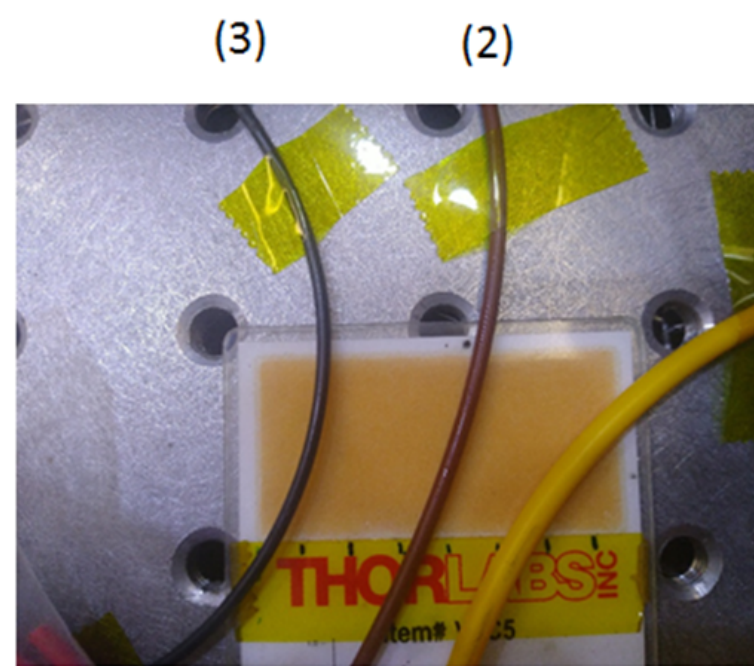


Power over Fiber (PoF)

Lasers Transmitter+ Fiber  + *Low Volt/High Current Receiver (CE)*
 + *High Volt/Low Current Receiver (SiPMs)*



Lasers – Deliver Power

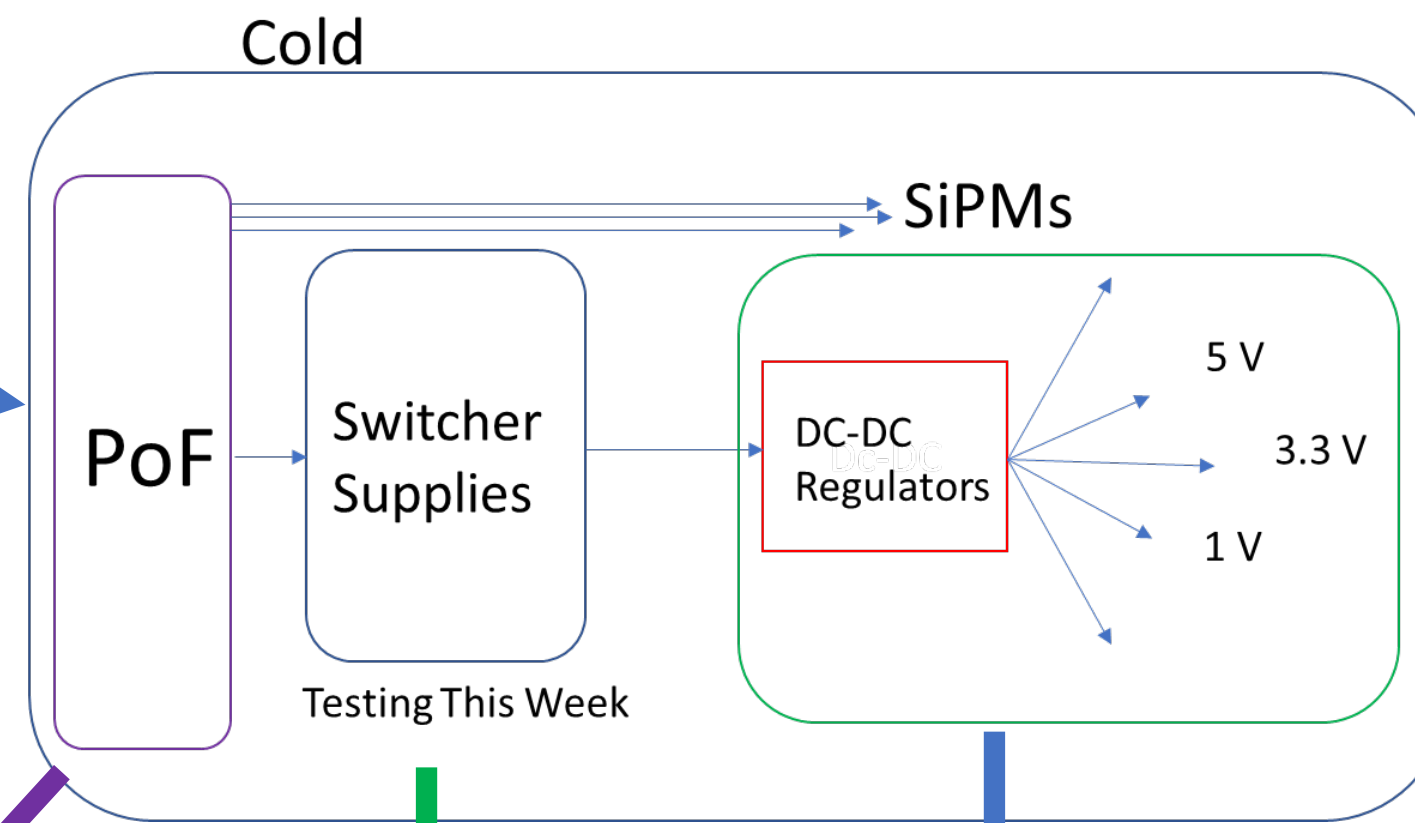


Fibers Testing

Light Receiver



High Voltage/vLow Current Light Receiver



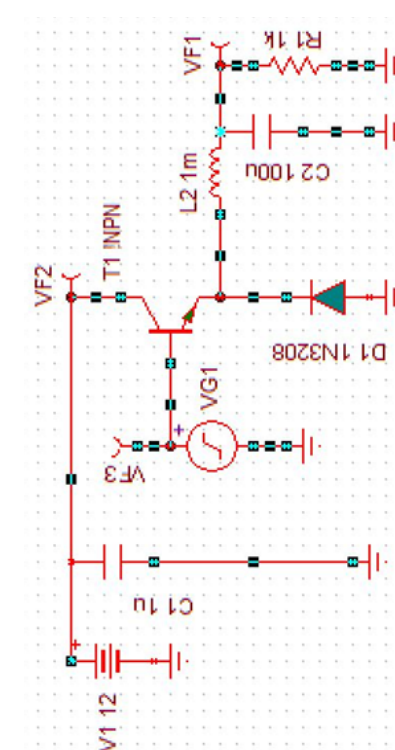
2 Systems:

SiPM: 48 Volts @ <1 ma

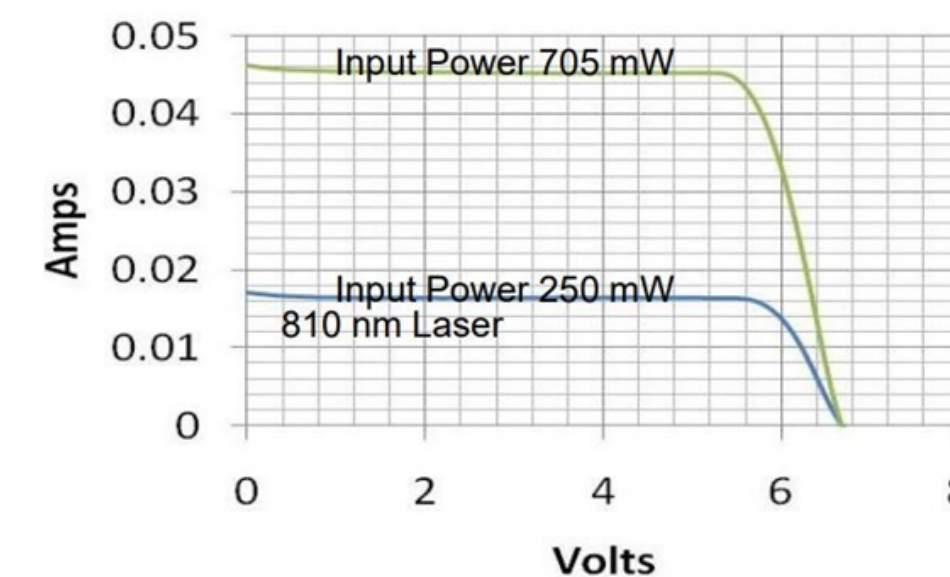
Electronics:

Communication Systems:

5, 3.3, 1 Volt @ Amps



I-V Data versus Input power

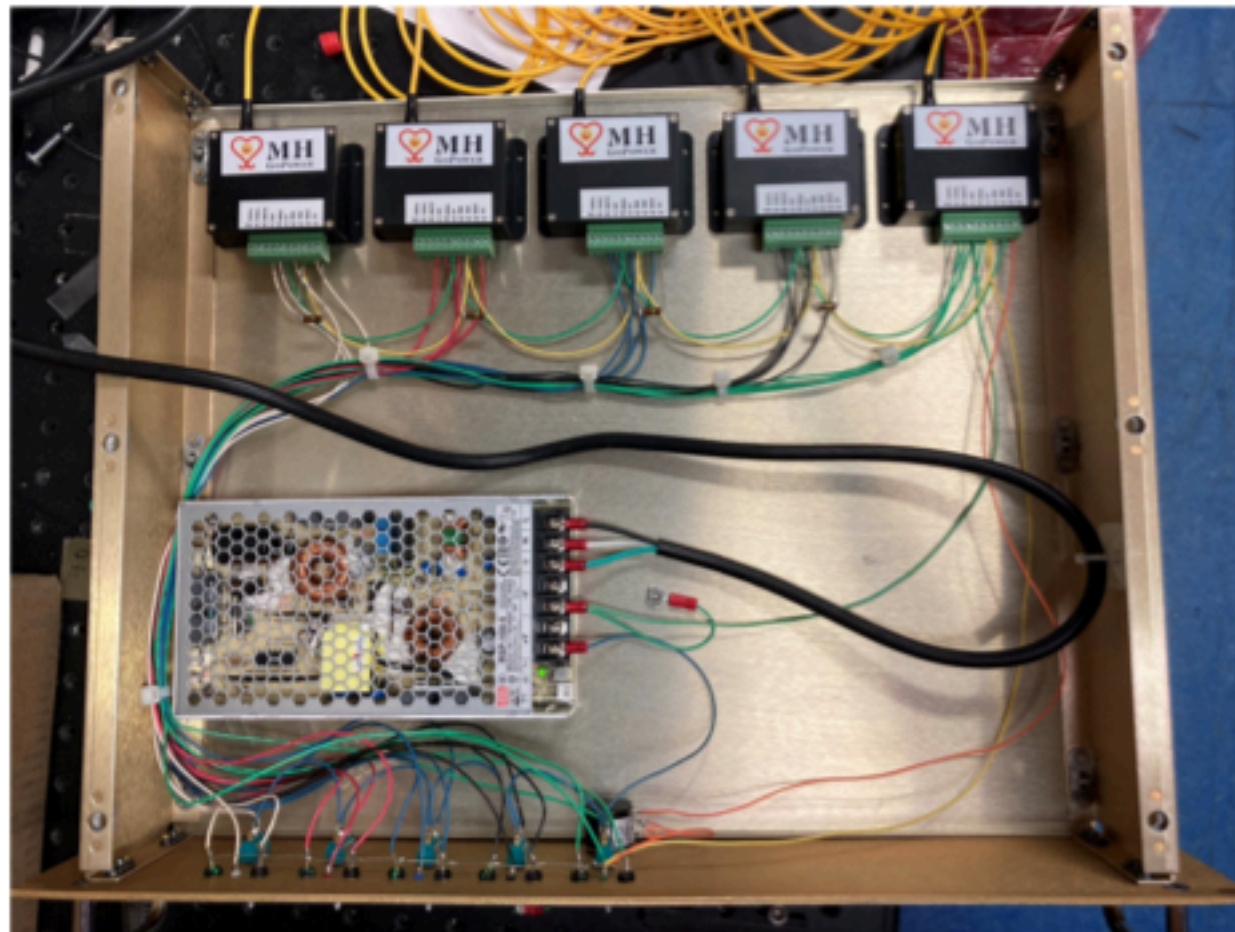
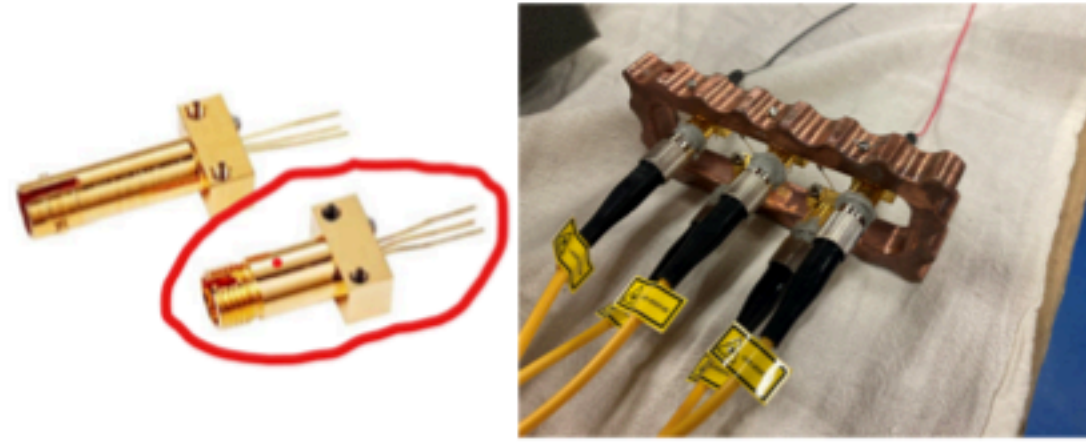


Low Voltage/High Current Light Receiver



6V LPC Package

Power over Fiber System



Cathode SiPMs

- 320 ARAPUCAs
- Divided into sectors (4 – 6)
- 48 Volts +/- 80 mv
- 50 ma (DC) / Sector (assuming 5ua/SiPM)
- Some storage capacitance at housing units

Tested power (FNAL/CERN)

Certified 48 v

Certified short-term stability

Verified power vs load

Need to verify long term viability

Test DC-DC converter to handle load variations

Electronics Box (x 80)

- 4 Transmitters
- 200mW bias(10ma@5V*4)
- TxPower 1.6W(80ma@5V)*4
- 4 OpAmp - Active Ganging
- 5V@10ma*4=.2W

4pi Reference Design

PoF Receiver

Opto-Electric Pwr Conversion Efficiency:

$$\epsilon_{OE}^{Si} \simeq 25 - 35 \%$$

Or

$$\epsilon_{OE}^{GaAs} \simeq 60 \%$$

Power Budget Estimates:

Analog CE+Transmission: < 200 W

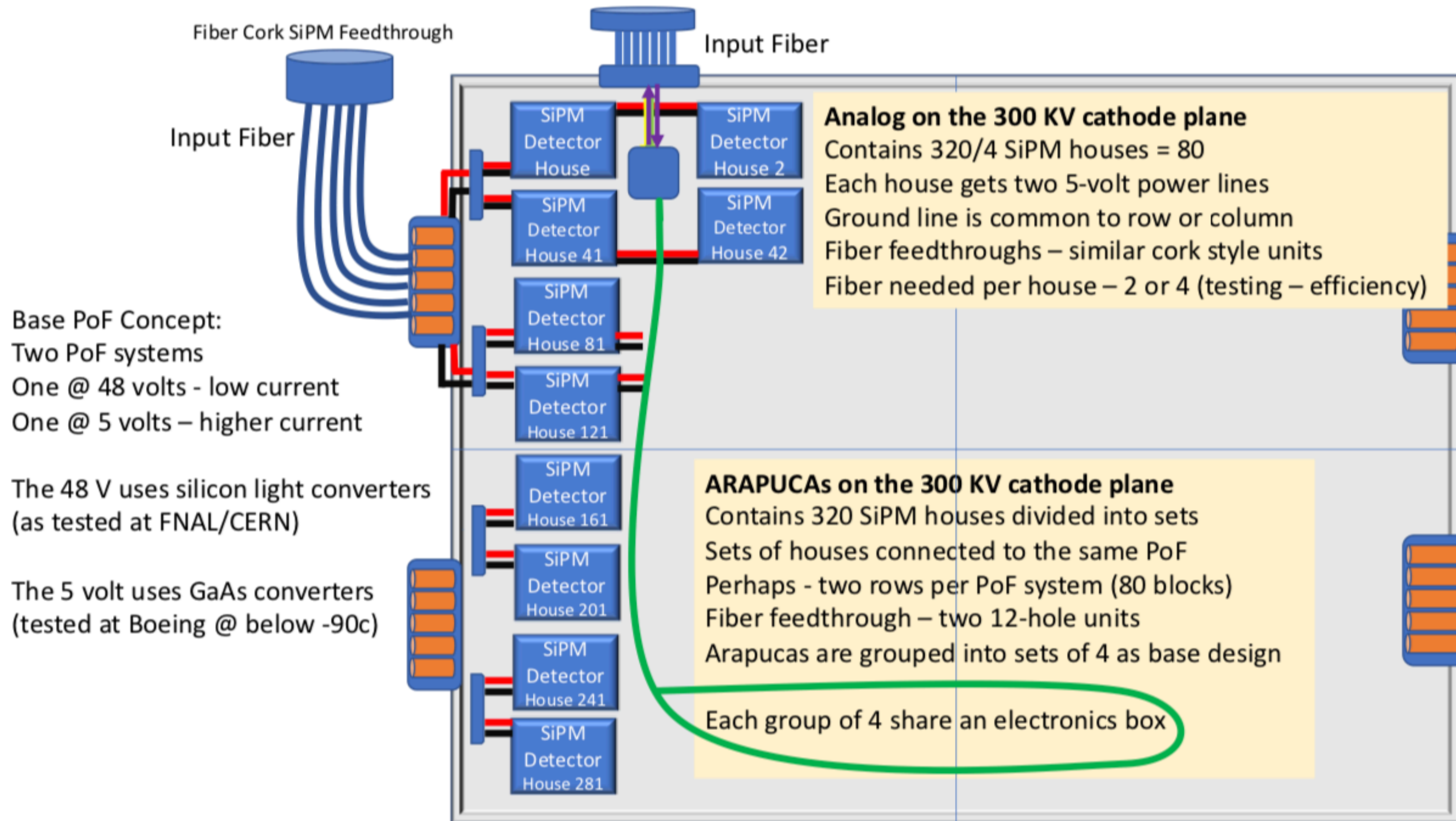
Dissipated Power in LAr:

Analog < 0.6 kW

Digital CE+Transmission: ~ 800 W

Digital ~ 2.5 kW
(~ 1.3 kW – if GaAs)

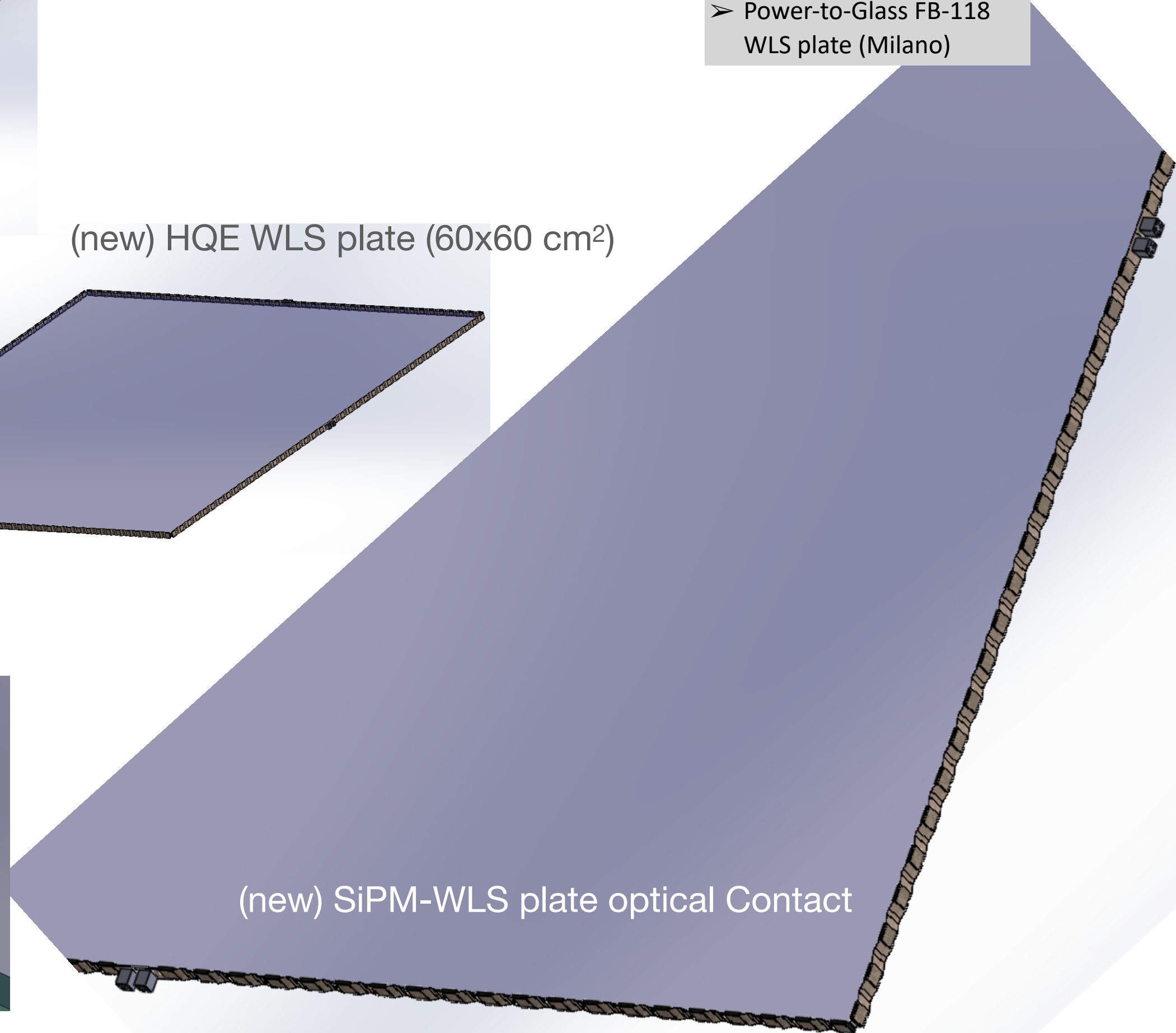
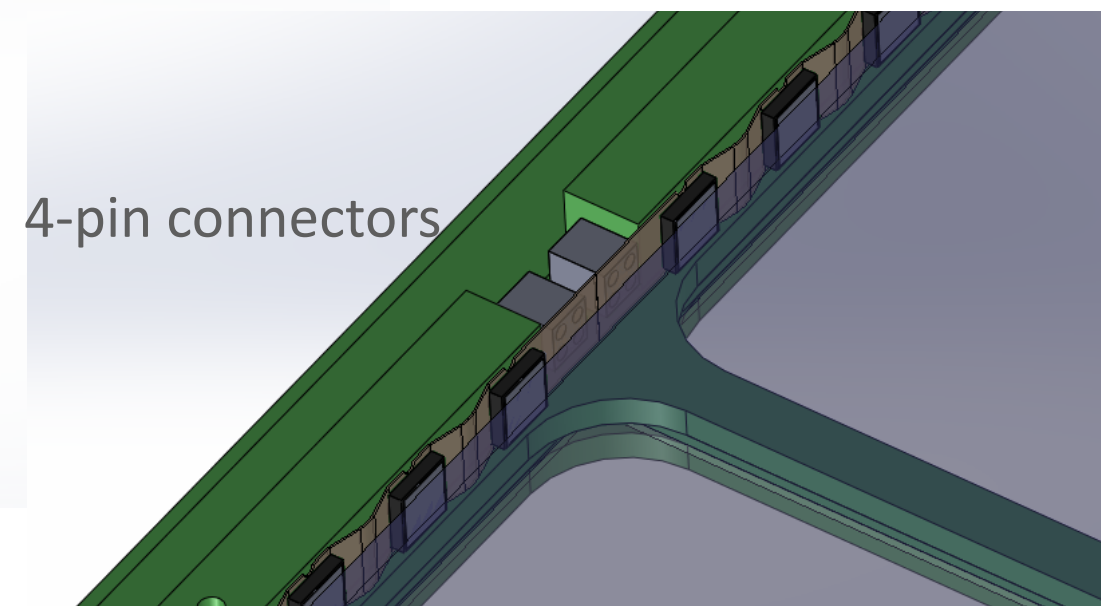
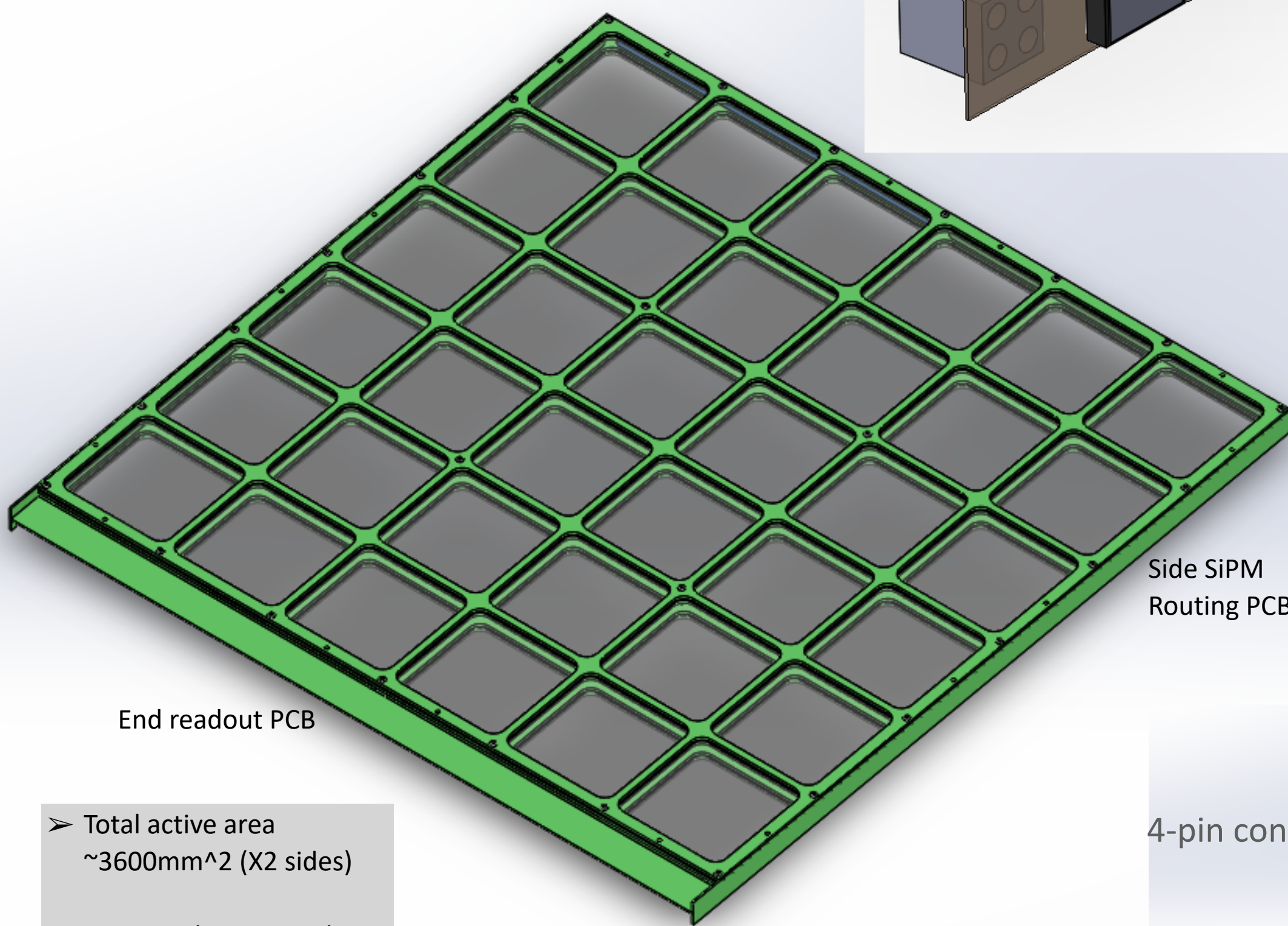
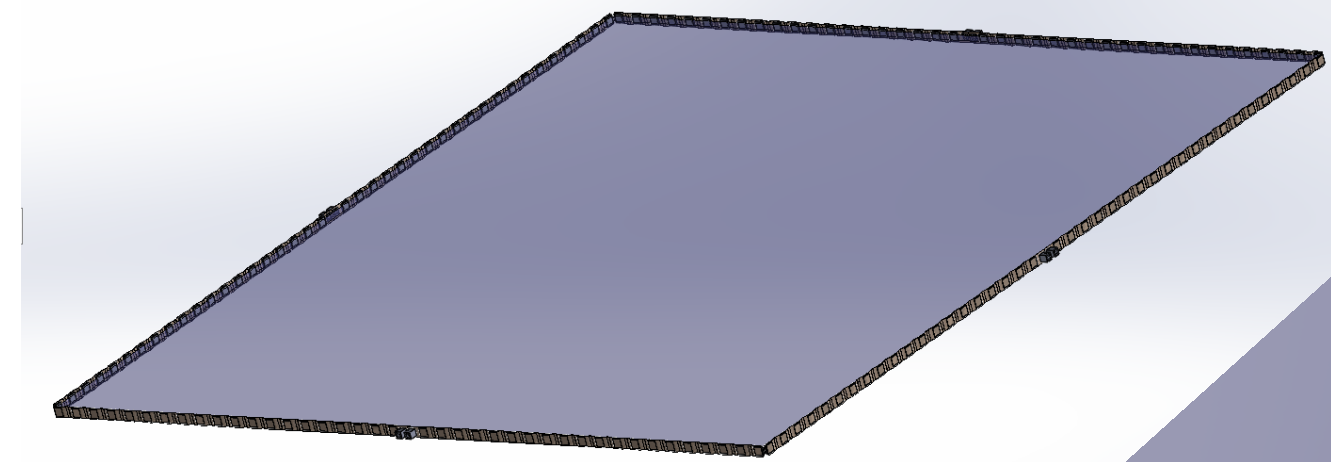
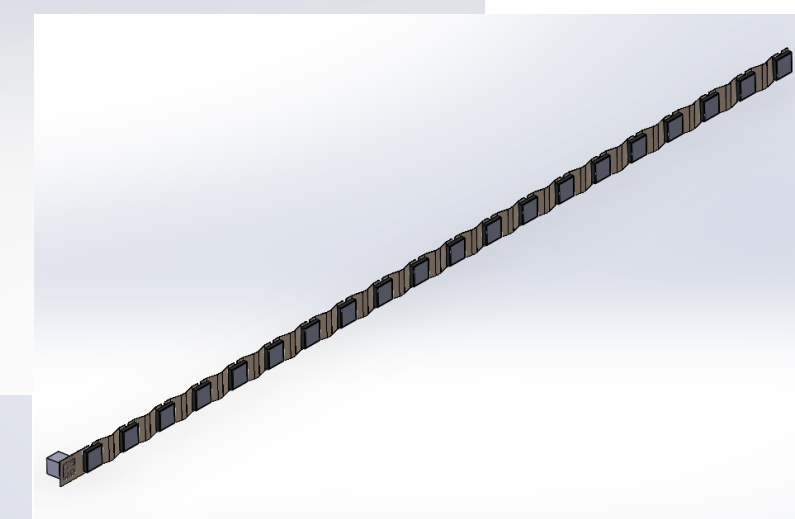
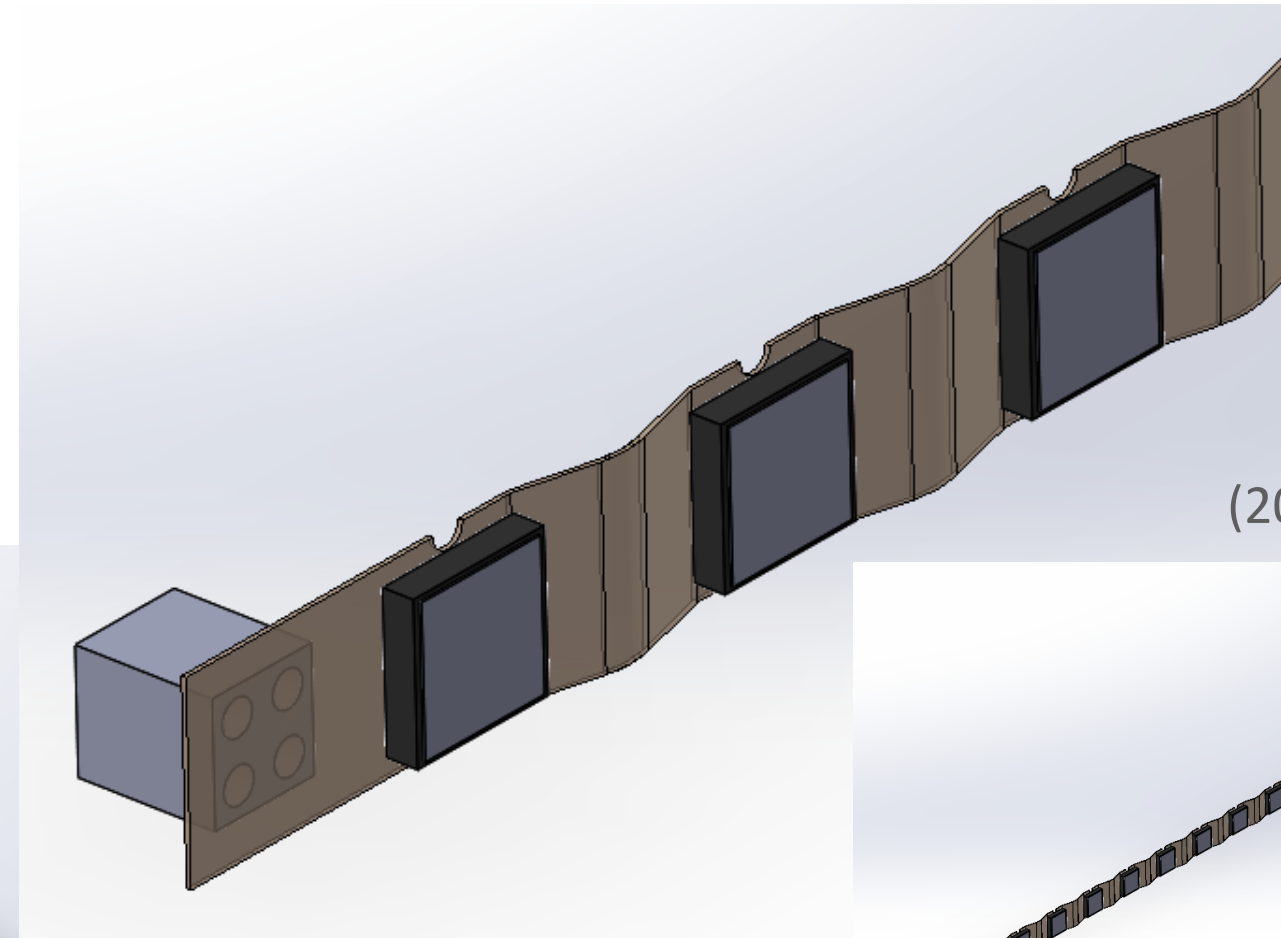
Power over Fiber System



xARAPUCA Tile (new generation)

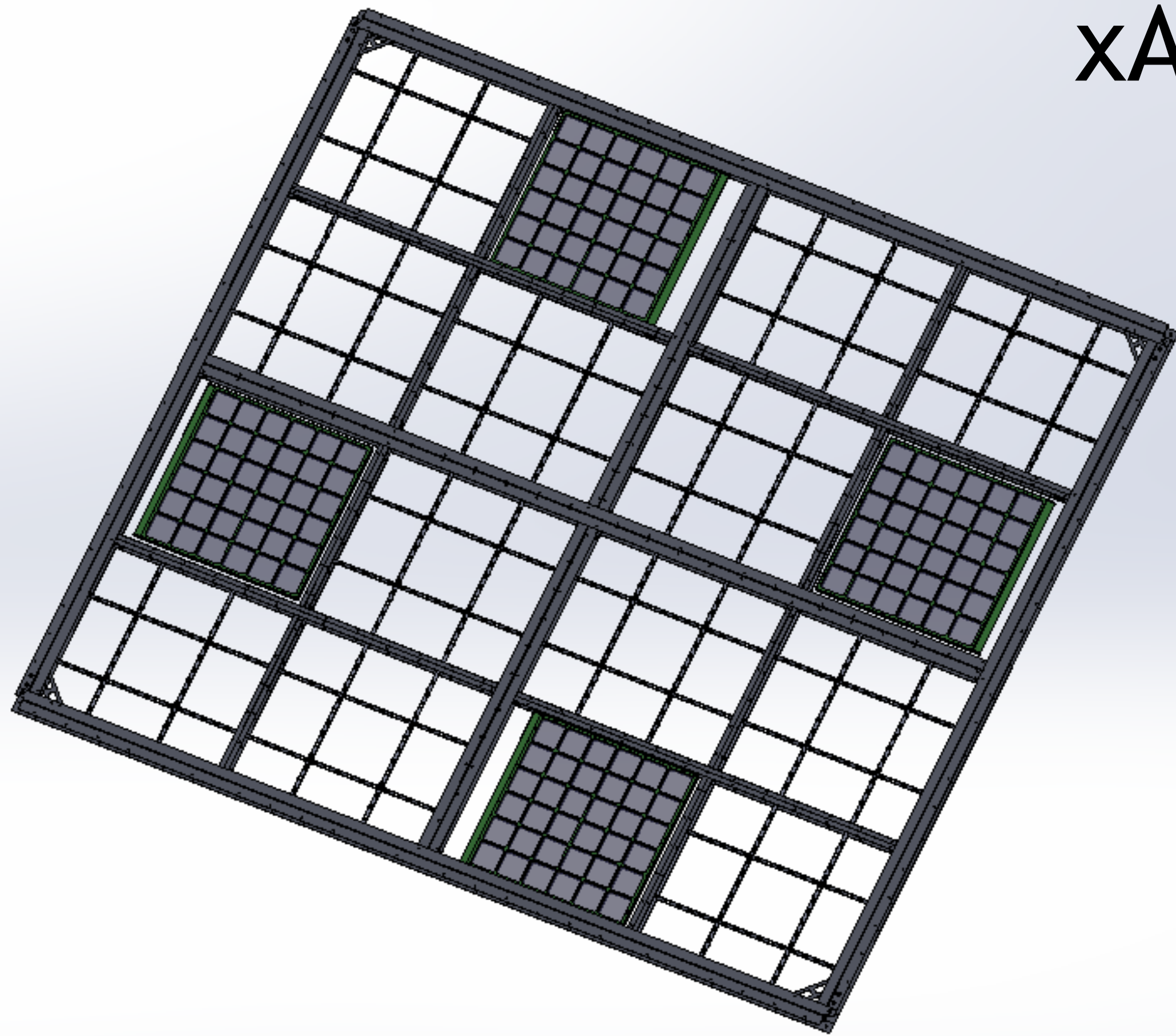
- 160 SiPMs (40 per side)
 - Glued to WLS Bar for improved performance
- SiPMs mounted on Kapton flexi-PCB
 - Addresses relative thermal contraction of WLS plate/frame.
- Power-to-Glass FB-118 WLS plate (Milano)

(new) xARAPUCA Tile design for VD PDS

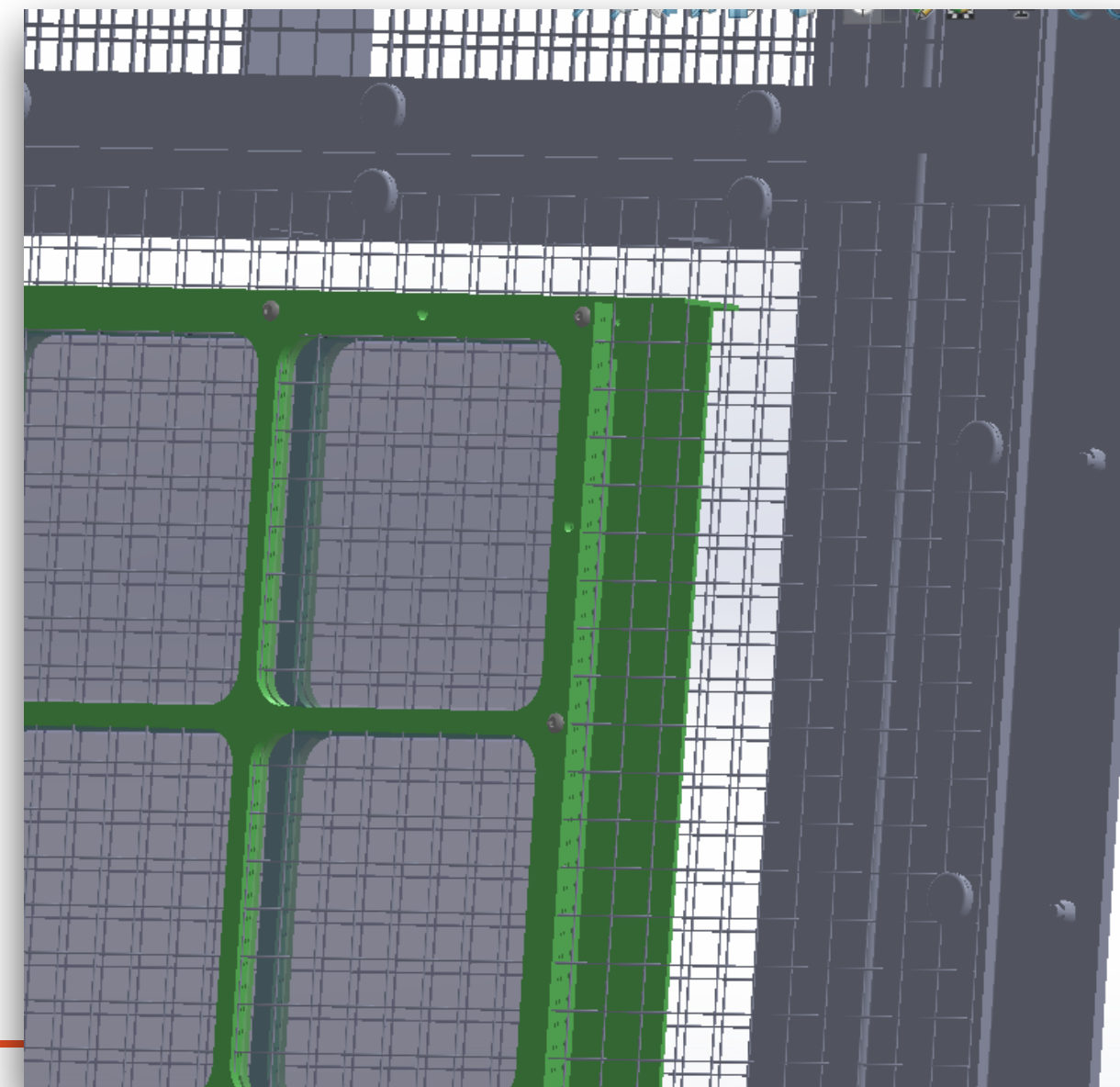
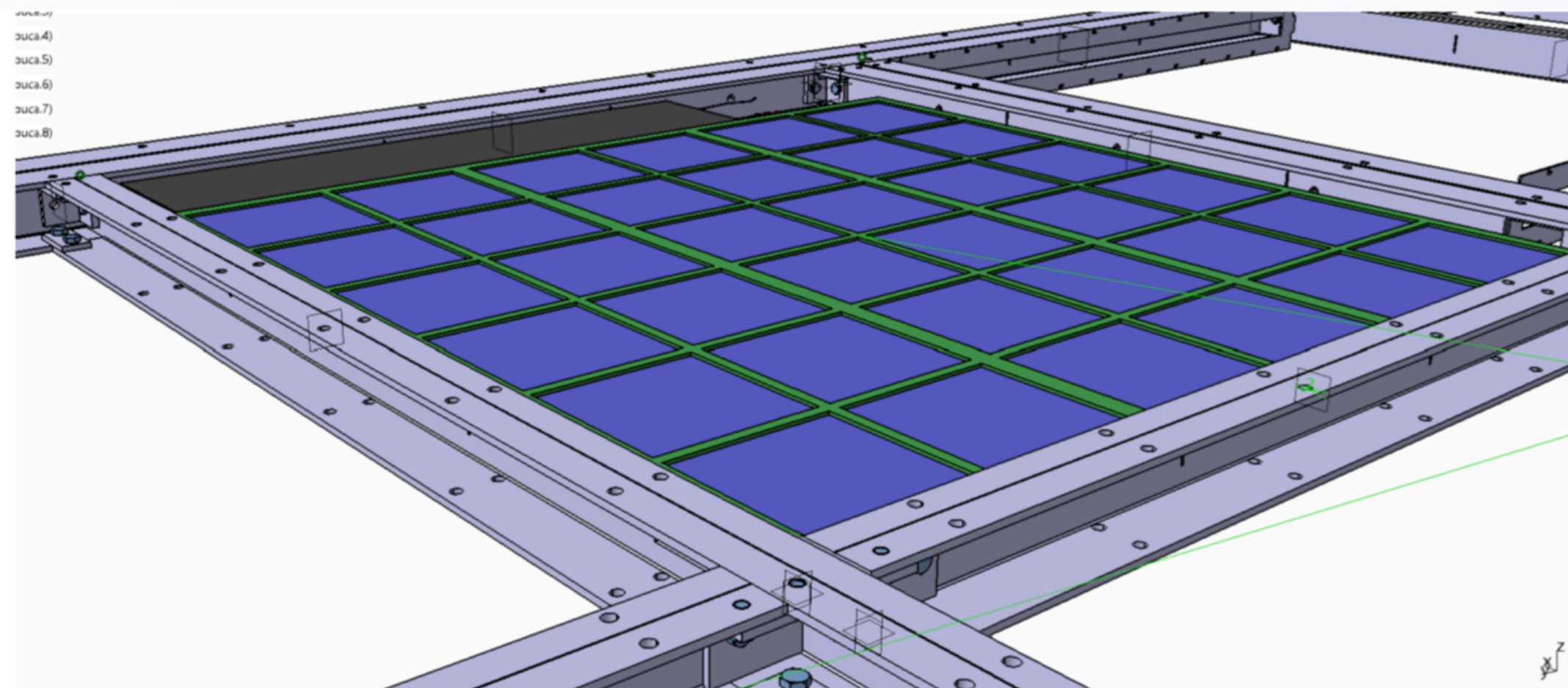
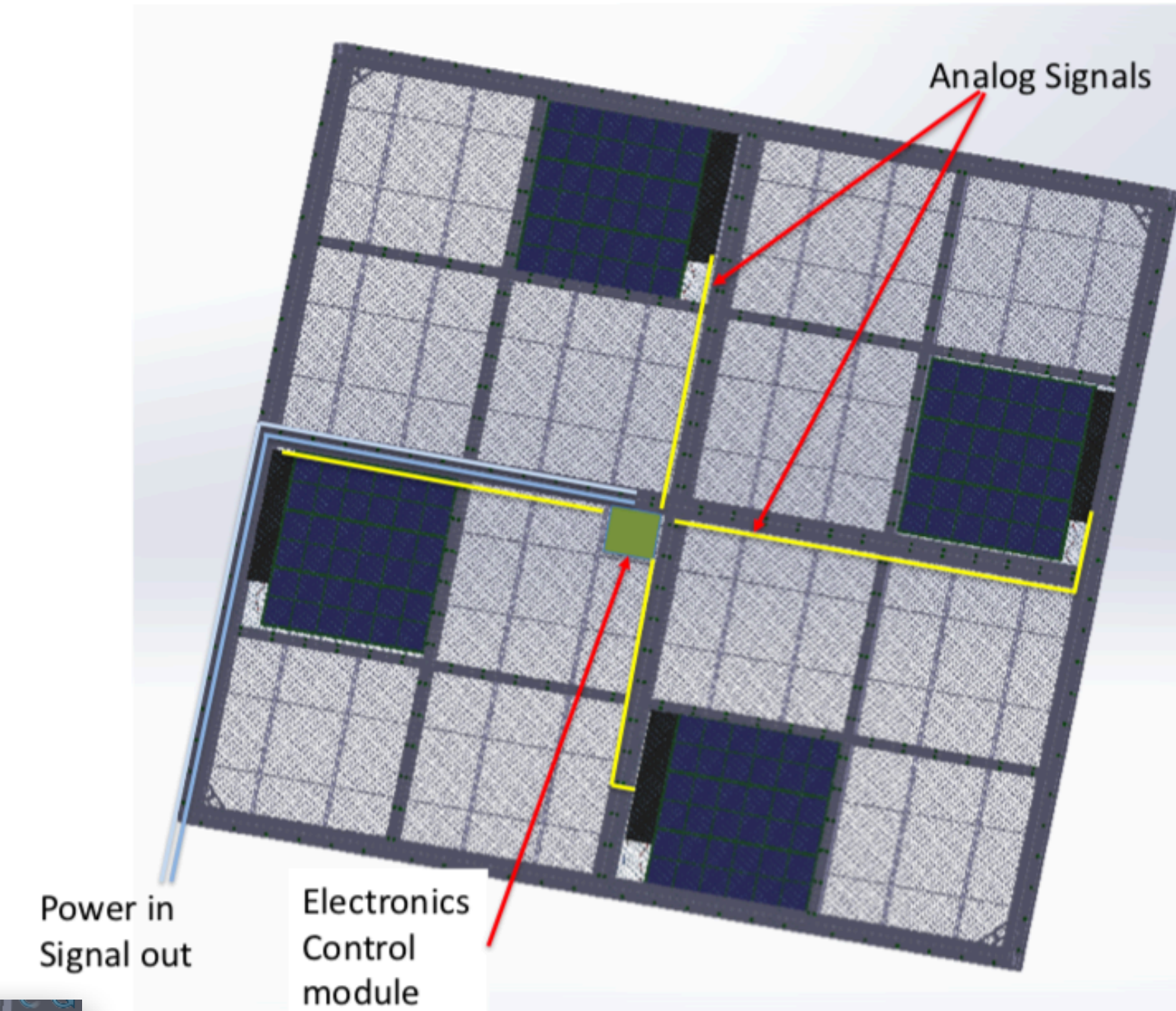


- Total active area ~3600mm² (X2 sides)
- Estimated mass ~5.5kg per tile
- 160 SiPMs (40 per side)
- FR-4 G-10 Frame components

xARAPUCA - Cathode Integration

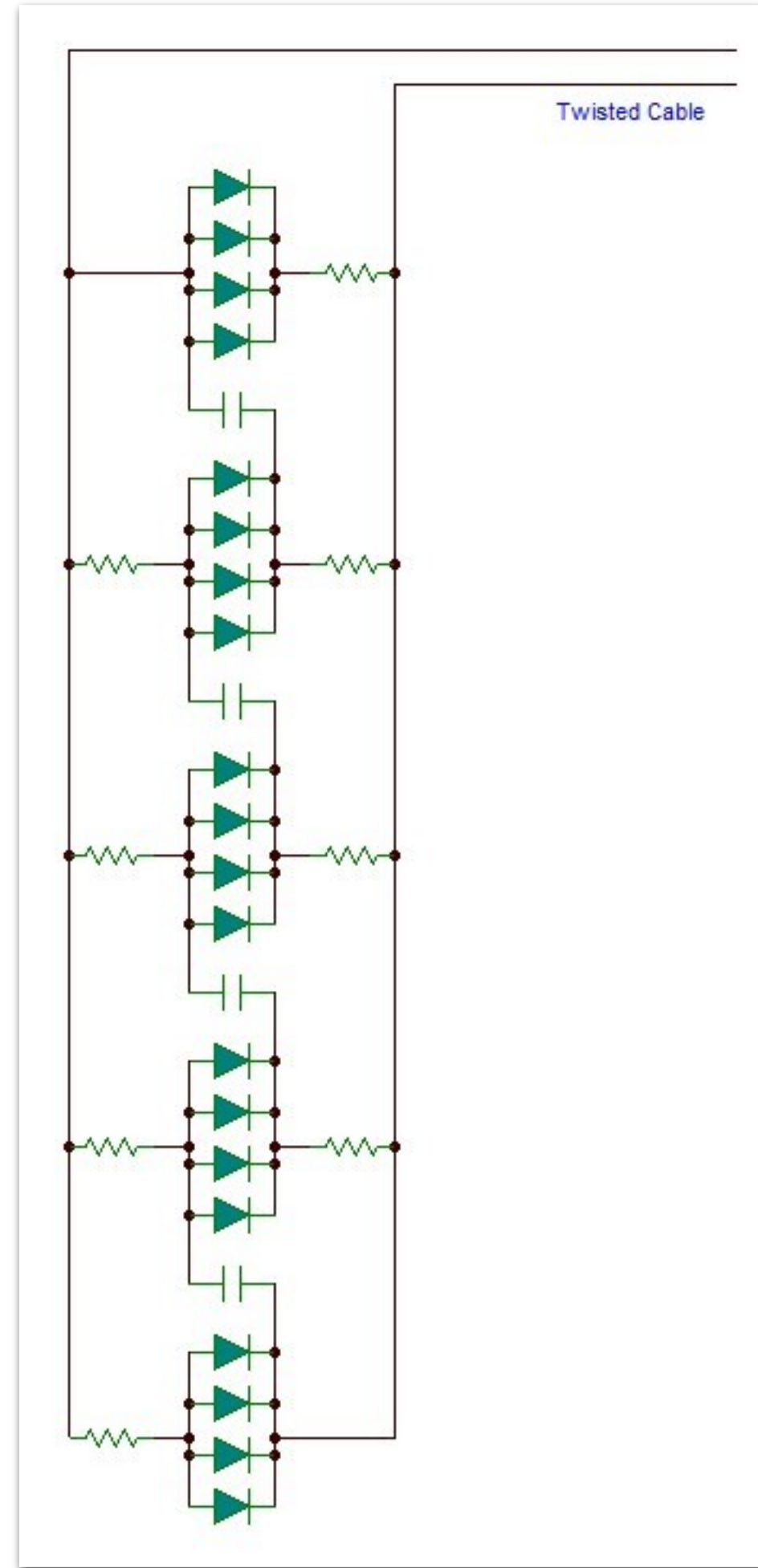


- 4 modules per cathode module
- One readout electronics assembly per module
 - ~200mm²
 - Two PCBs in vertical stack: One analog board with amplifiers, (4 ADCs?) one digital board with signal readout, power, slow control



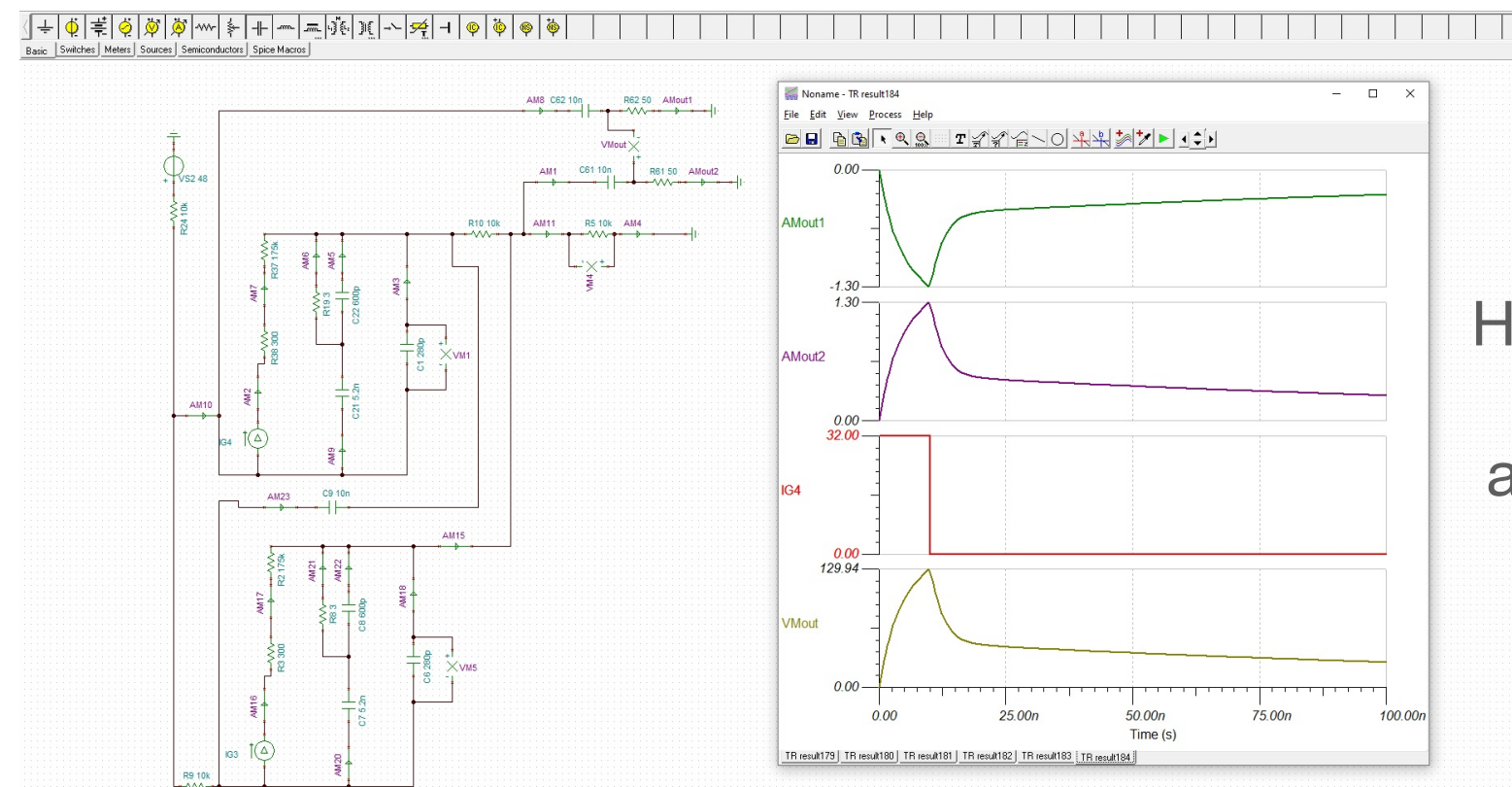
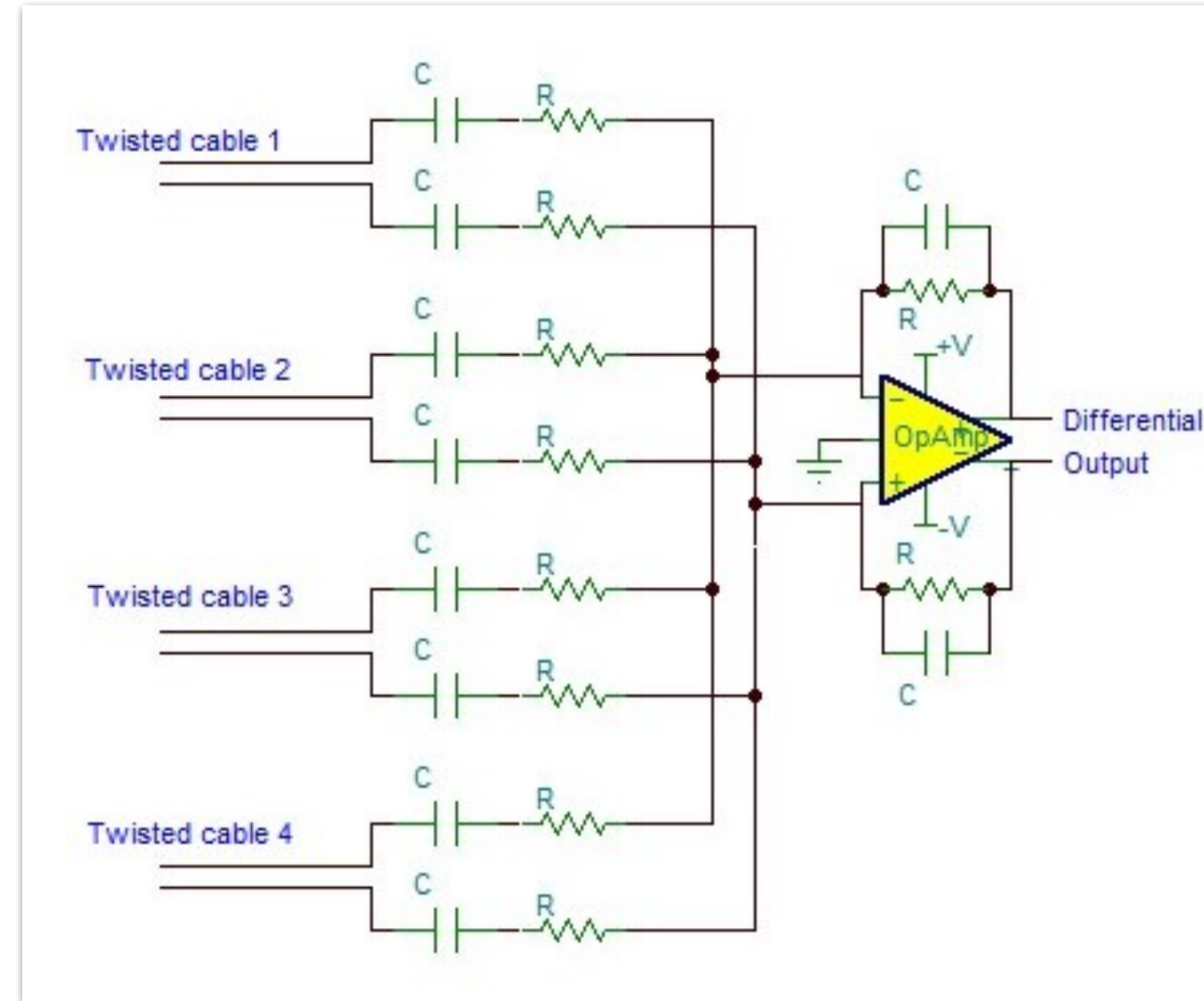
Passive and Active Ganging - SiPM CE Stage 1- Stage 2

(20 SiPM) - Hybrid Passive Ganging Stage
Flex Kapton PCB

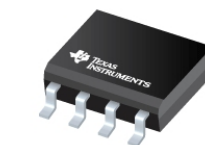


Test board in production

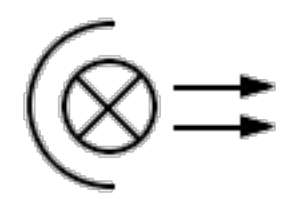
Active ganging + Ampli Stage
Analog CE PCB



Hybrid Passive Ganging
(4x5 SiPM)
analyzed and validated
by SPICE simulation

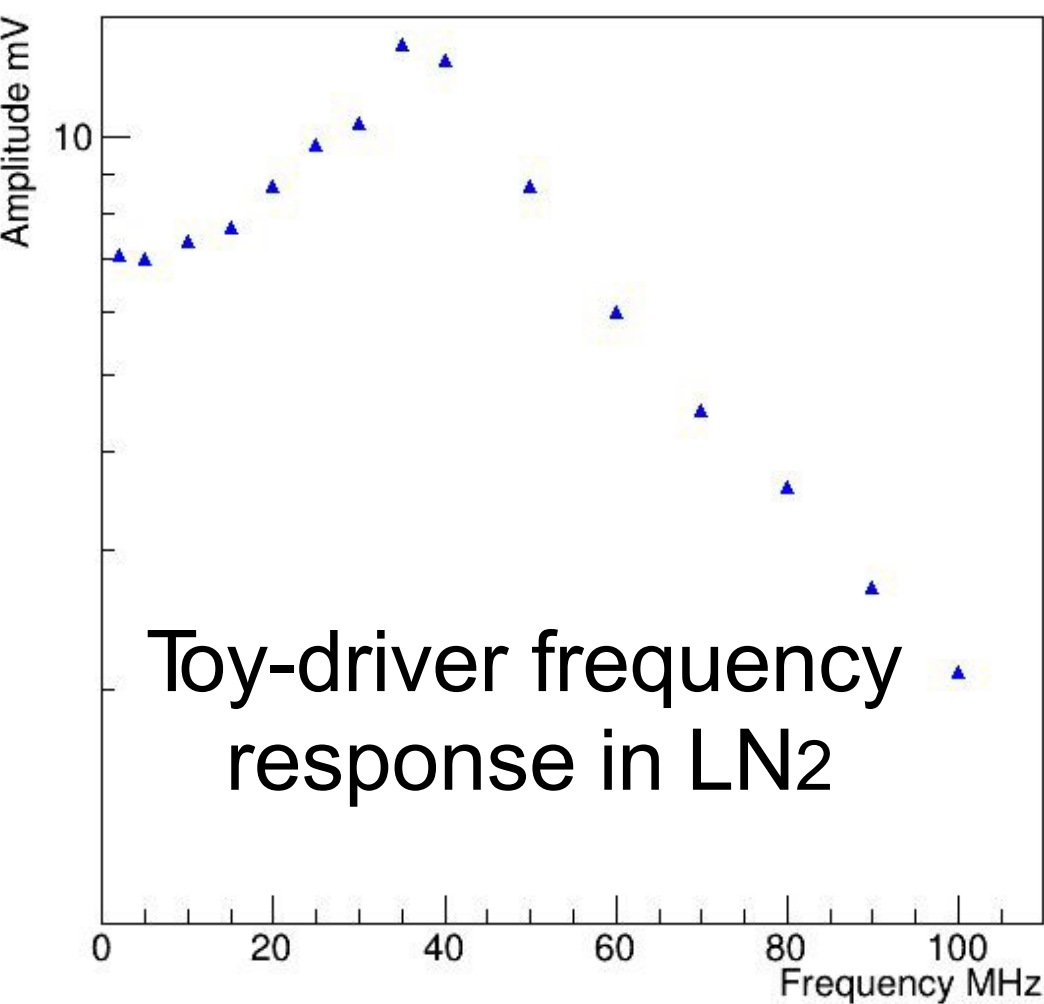


COTS OpAMP
selected and
Validated in Cold
(different options available)

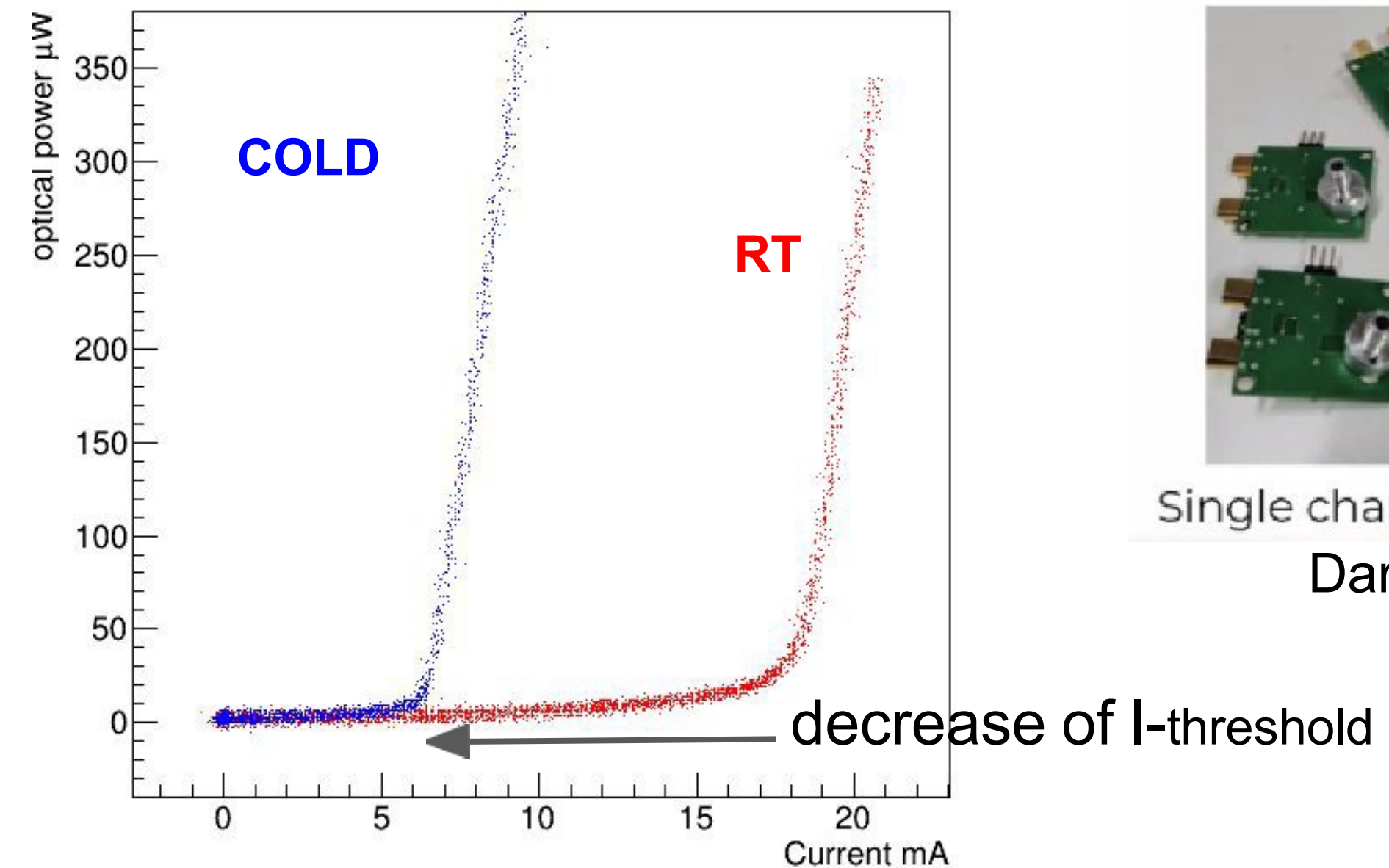
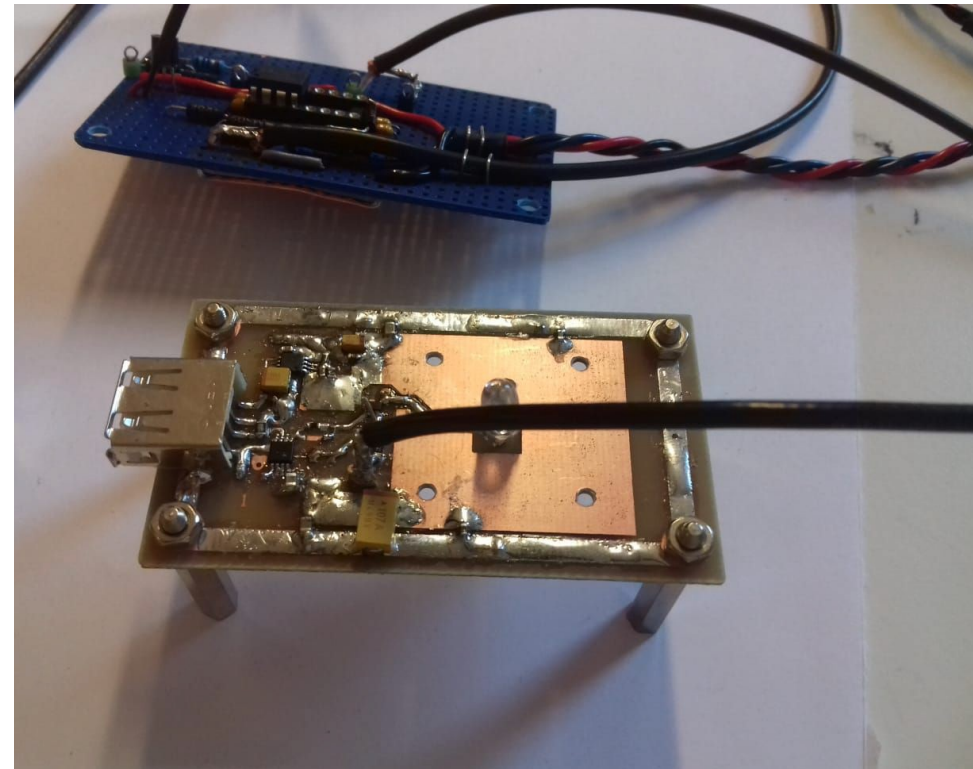


Analog Optical Transmitter

- Previous investigations show encouraging results
- The DarkSide experiment already has developed a well-functioning single channel prototype
 - it does not meet DS's radiopurity requirement yet but performance in cold matches technical requirements
 - Collaboration with DS (on analog Transmission R&D) is providing valuable inputs for our design



test board

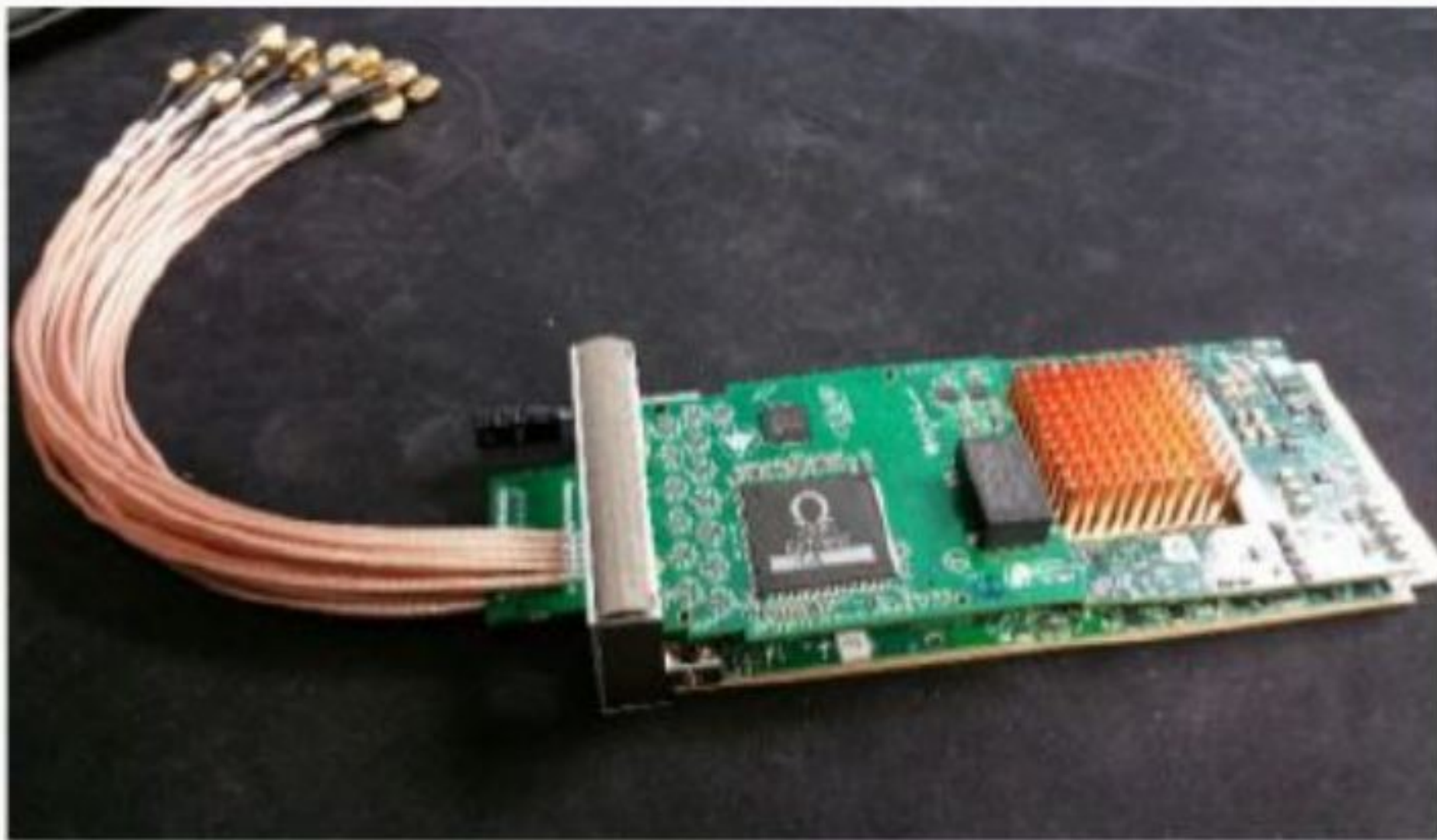


Single channel prototypes
DarkSide

- Laser driver:
 - in-house design, functioning at cryo-temperatures (LN2) - bandwidths of ~ 50 MHz in cold
 - evaluation of components in test-board with a simple driver circuit \rightarrow promising components identified
 - non-linear adaptation to reach larger dynamic range to be developed
- Light source and optical coupling
 - lasers show linear behavior and lower threshold current in cold \rightarrow investigating 1310nm candidates
 - coupling to fiber is the challenge of ongoing development
 - \rightarrow commercial solution (pigtail) or DS-style connector

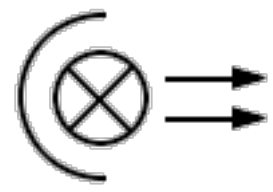
Analog Optical Receiver and Digitization

- First tests done with an off-the-shelf Femto receiver
 - now developing an in-house receiver with an InGas pin-diode and fast amplification
 - using off-the shelf Femto for coldbox test is an option
 - 200 MHz and ~20mVpp noise level



Previous development for Dual Phase

- Digitization at warm could be done using either DAPHNE or the PDS readout developed for DualPhase:
 - ➔ μ TCA standard
 - ➔ commercial motherboard with a StratixIV FPGA
 - ➔ custom daughter board:
 - ➔ 14 bit ADC chosen (AD LTC2155-14)



Digital Optical Links

Test Program at 295 K and 77 K

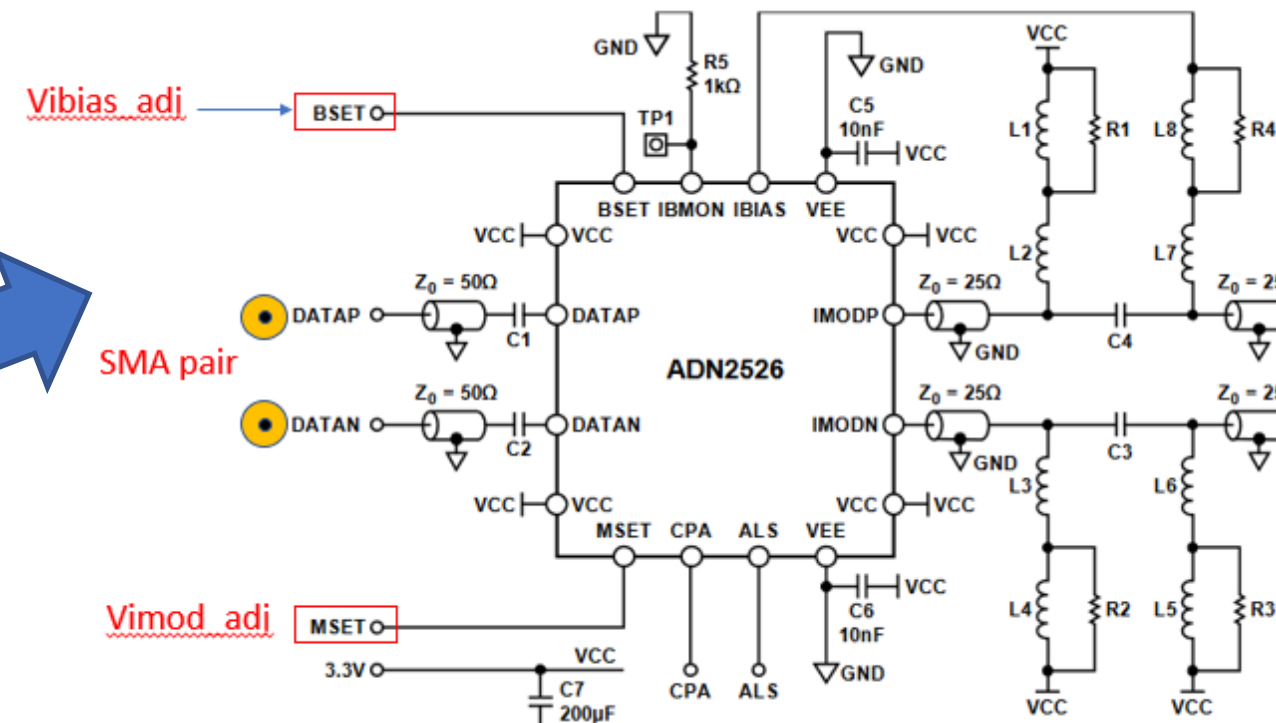
COTS SFP+ Transceivers



Laser Driver Selection

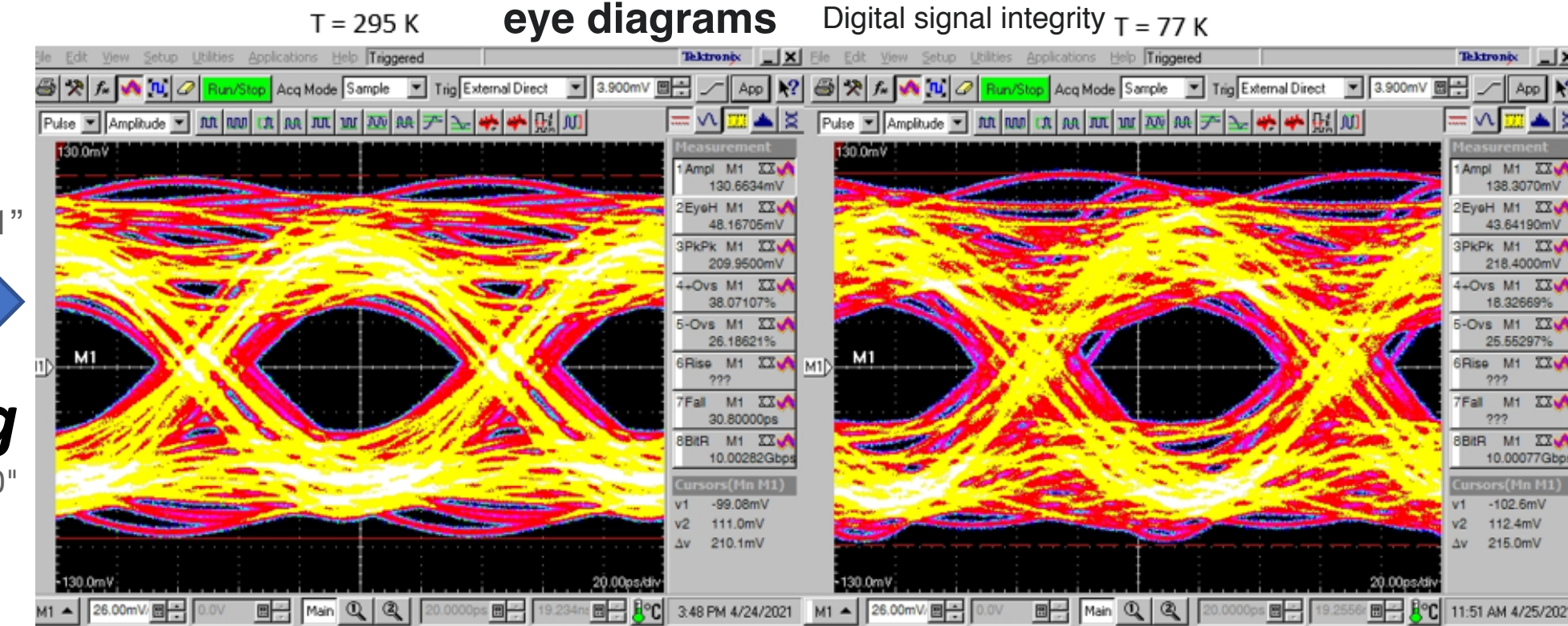
Selection

Laser Diode Selection



COTS Laser Driver ICs

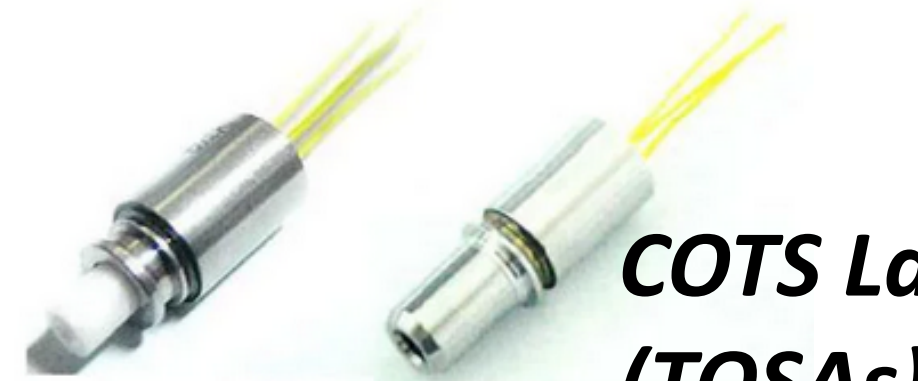
Binary "1"
Driver Testing
Binary "0"



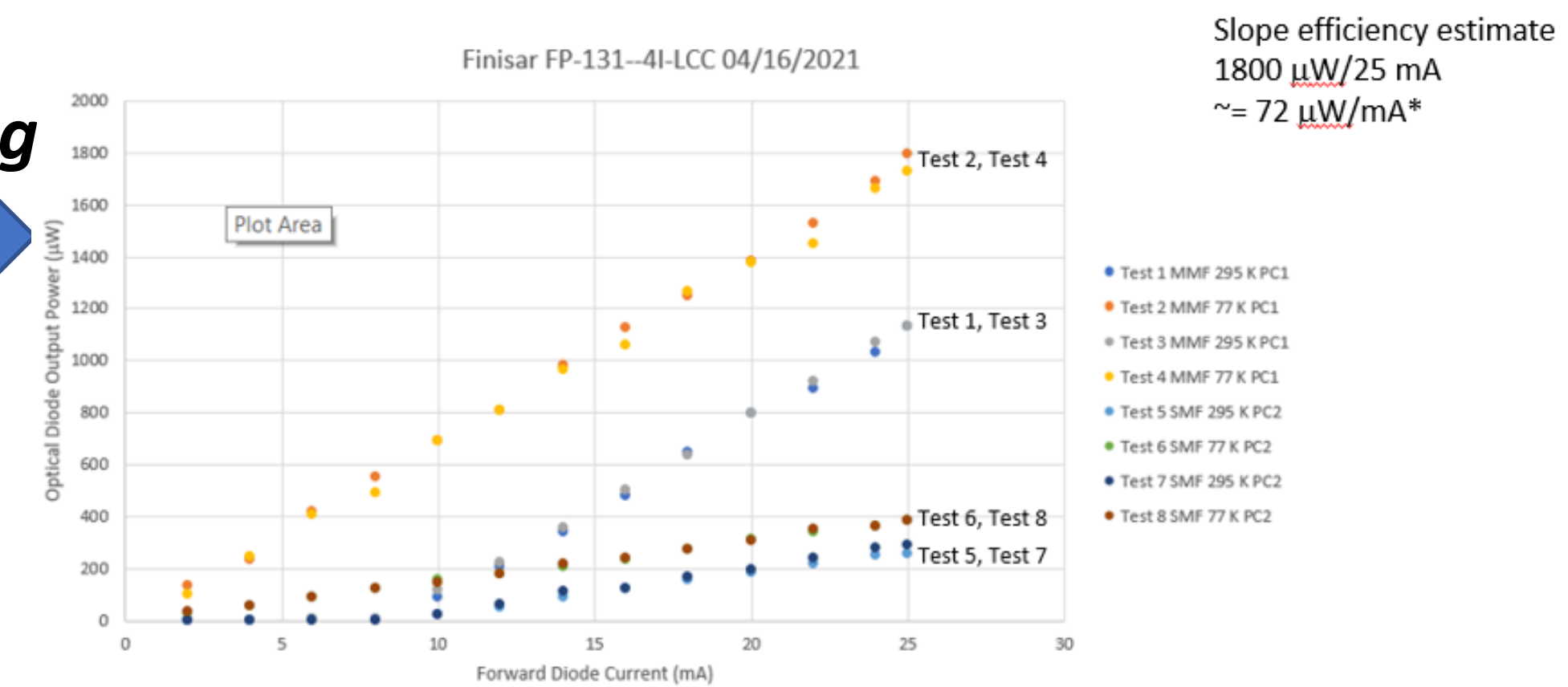
Peak to Peak = 210 mV (cursors)

Peak to Peak = 215 mV (cursors)

Diode Testing

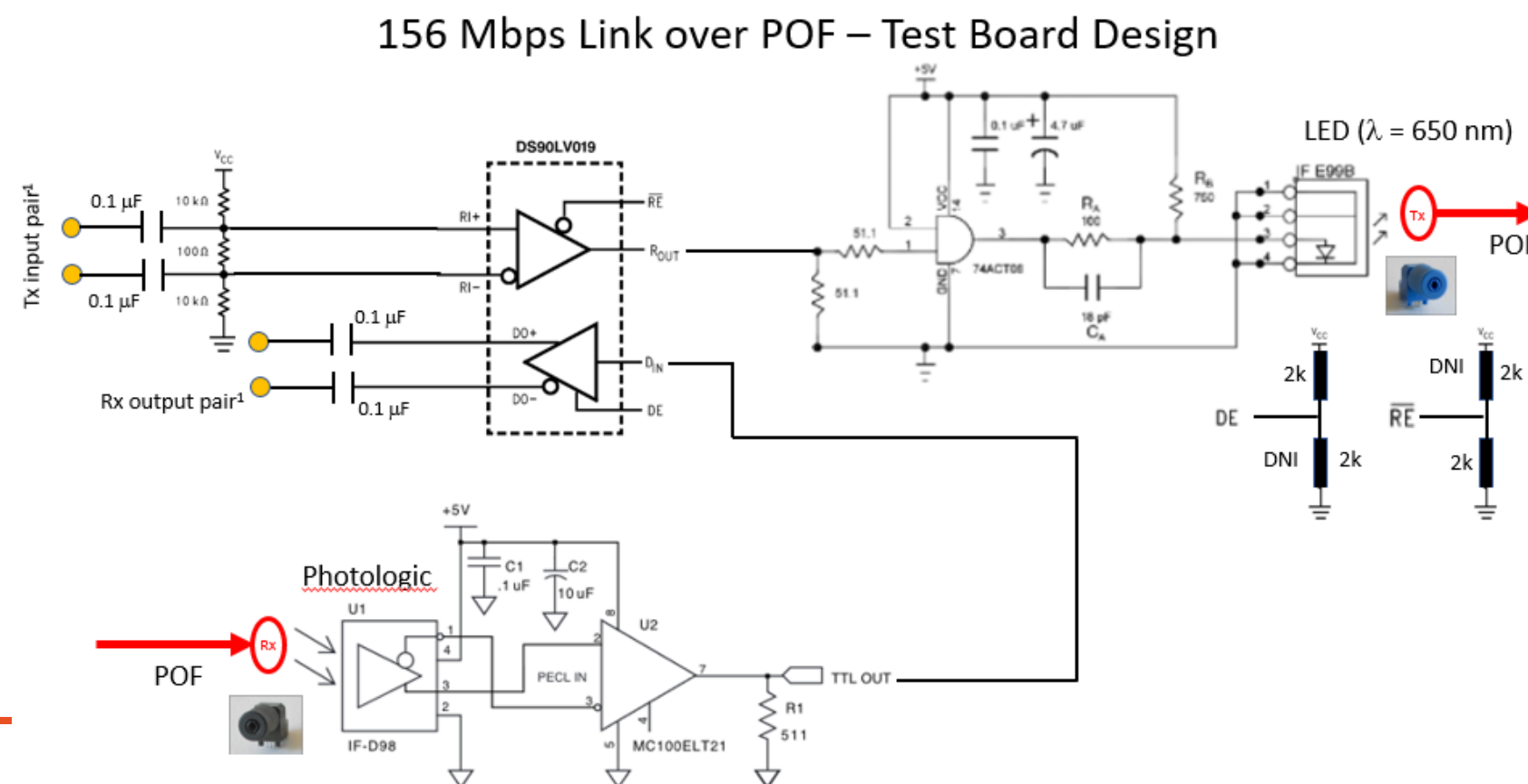


COTS Laser Diode (TOSAs)



Slope efficiency estimate
1800 µW/25 mA
~ 72 µW/mA*

Alternative Approach:
LED/Photologic Pair
Over Plastic Optical Fiber

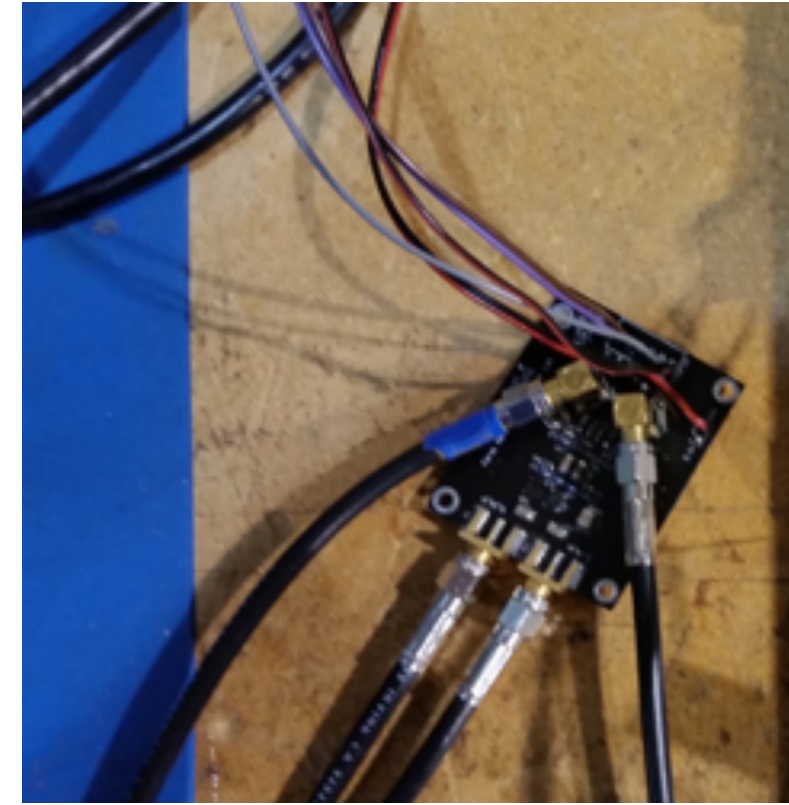


Brought Together for
Custom Transmitter (next slide)

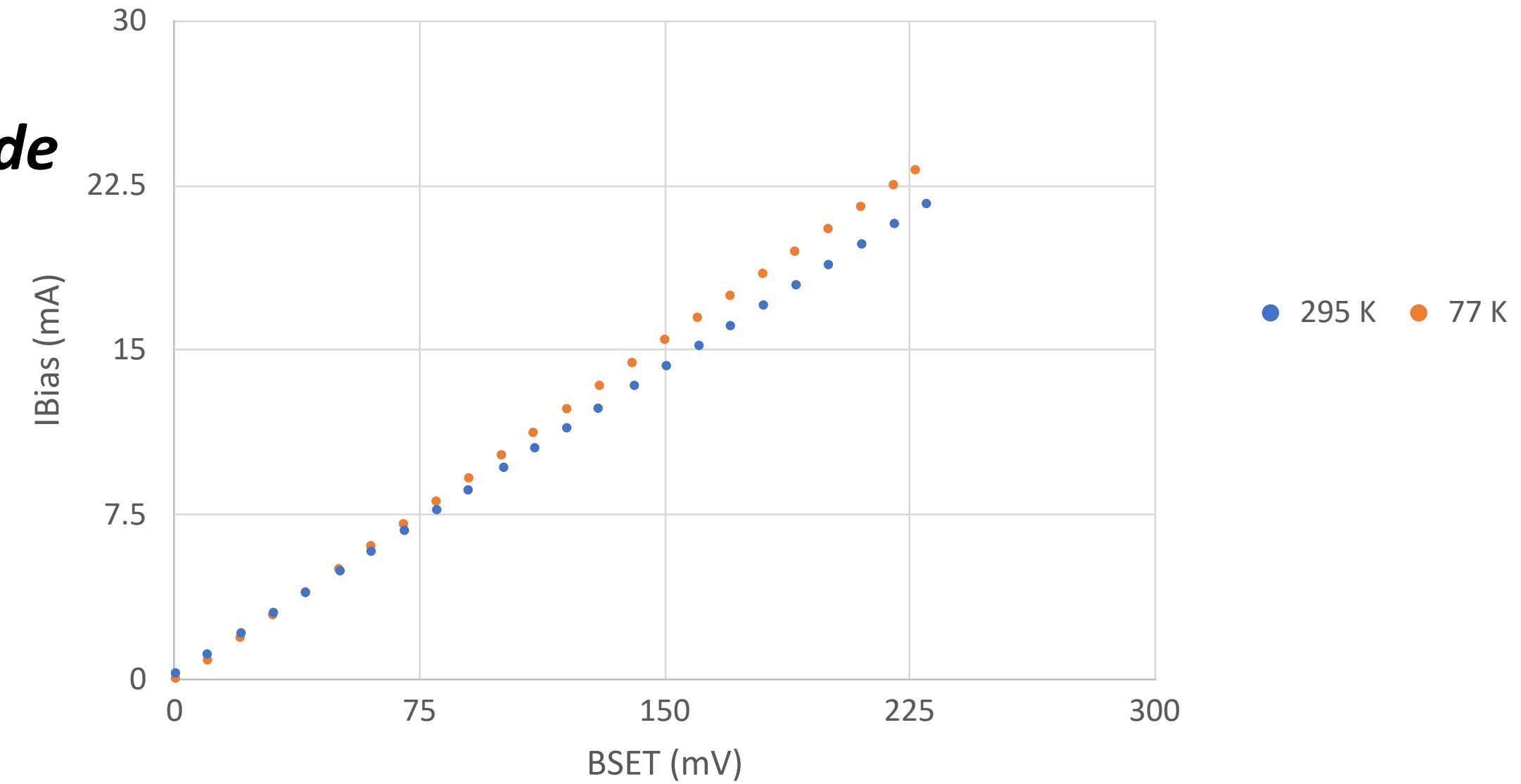
Laser Driver/Laser Diode Test Program

295 K and 77 K

**Custom Test PCB
For Laser Driver/Laser Diode**



IBMON Current vs BSET



eye diagrams

MSET =
50 mV

MSET =
75 mV

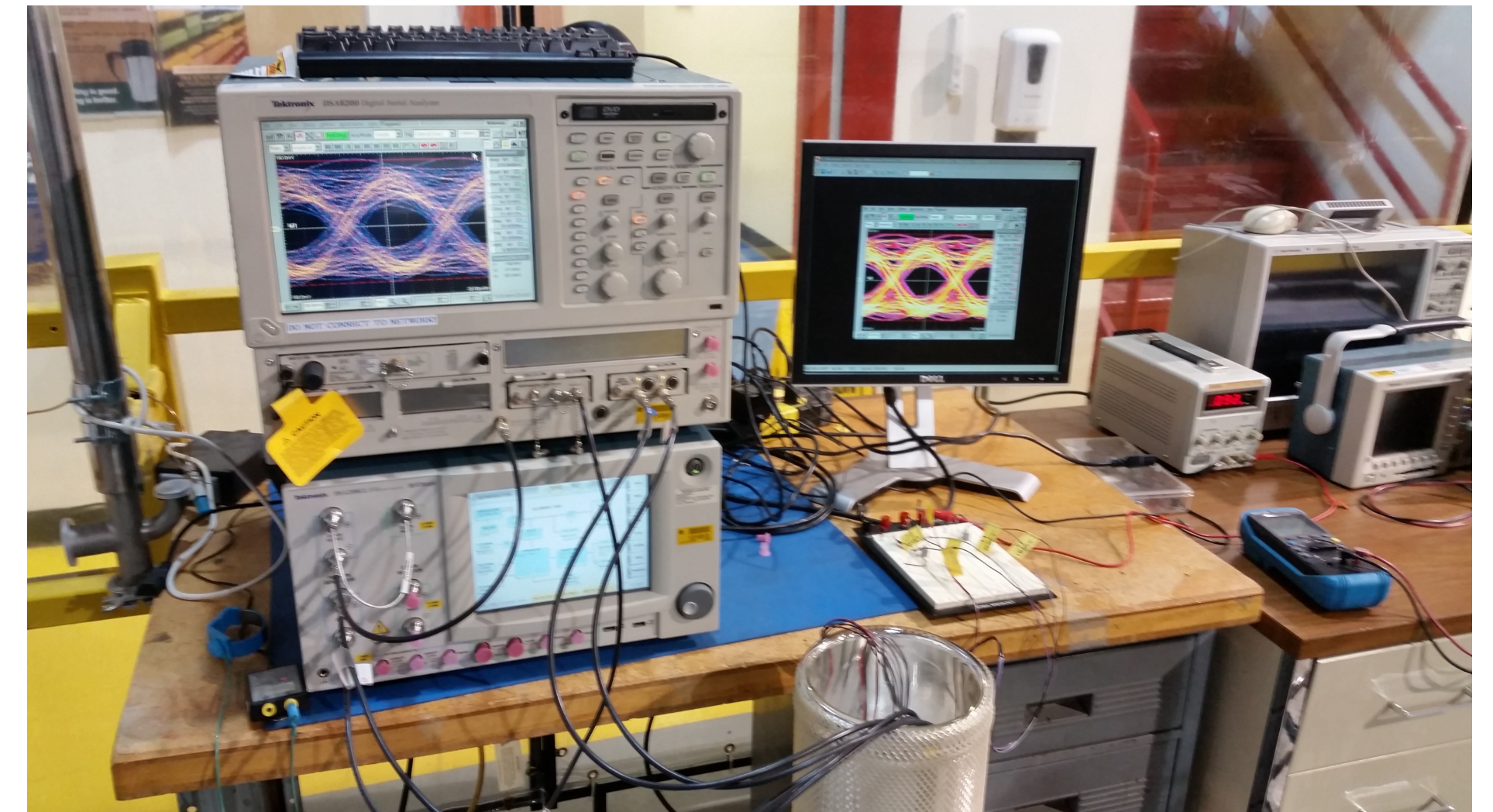
Digital signal integrity in Cold - Demonstrated

MSET =
100 mV

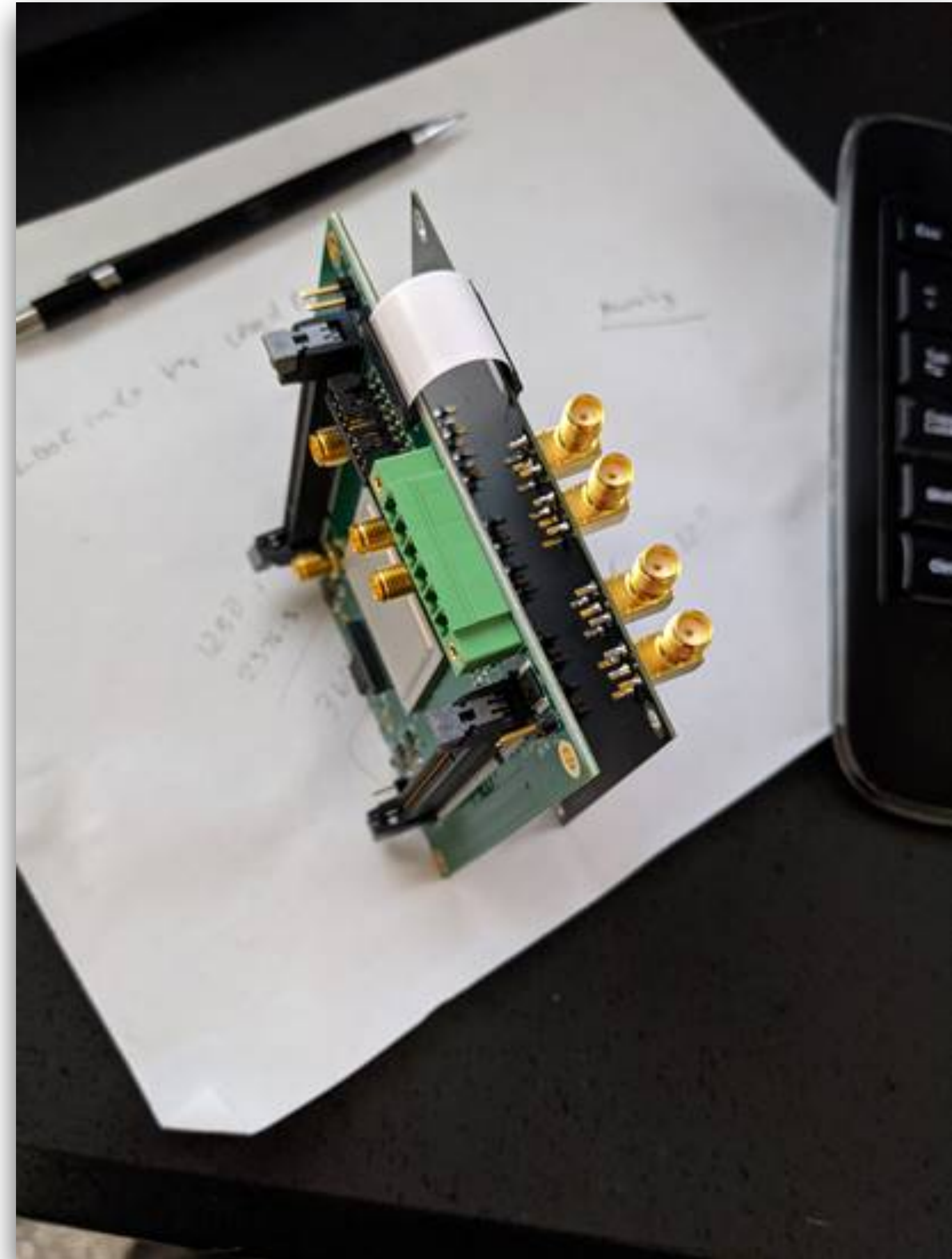
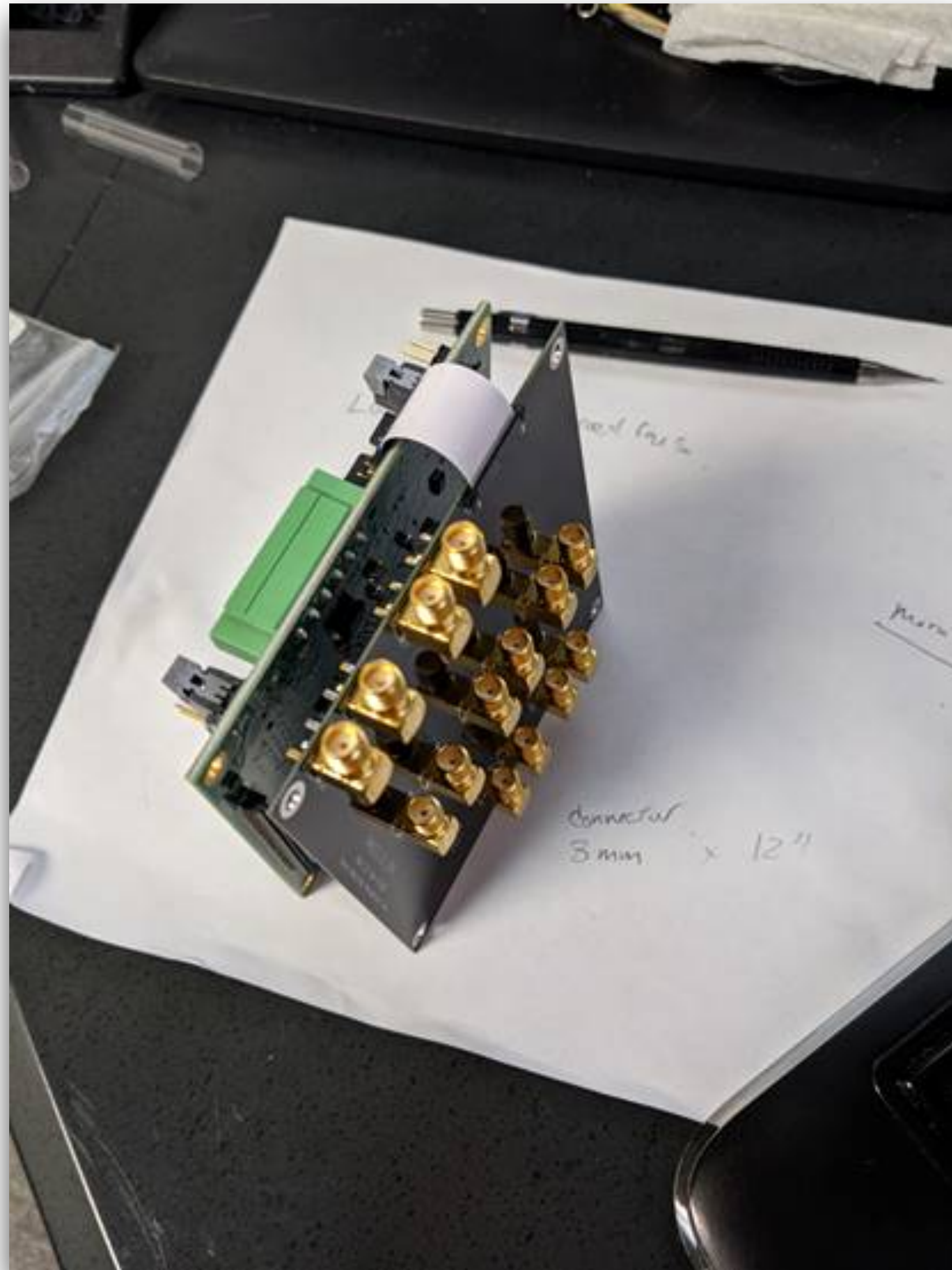
MSET =
125 mV

**IBIAS = 20 mA
PRBS7 @ 10 Gbps**

Test Stand At PAB



CE+Transmission Integration: Stacking concept



2021 R&D Strategy

Target **two** xARAPUCA prototype detector tiles for CERN cold box test:

Each 160 SiPMs 60x60cm²; one SiPM vendor for each

Target **two** prototype cold-electronics approaches:

1. “**Cold analog**” approach

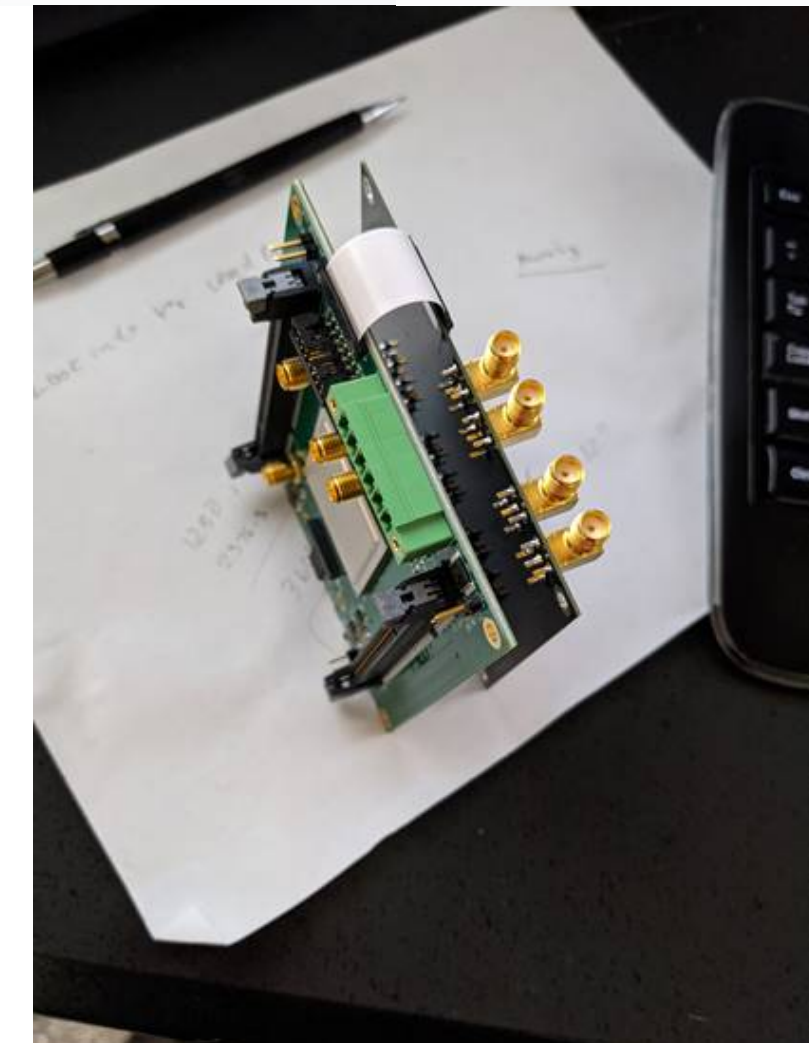
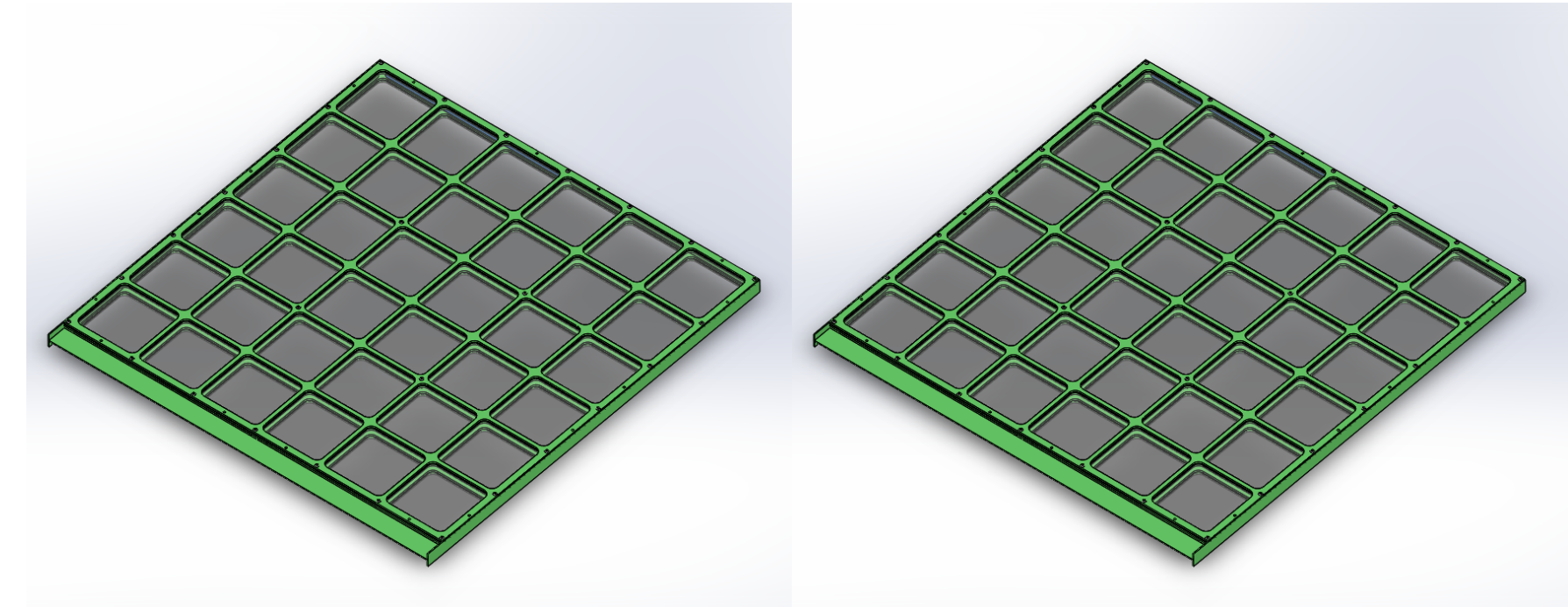
- 160 SiPMs passive-ganging => 1 active-ganged analog waveforms

2. “**Cold digital**” approach

- 80 SiPMs passive-ganging => 2 active-ganged digitized waveforms
- 14-bits @ 80Msps

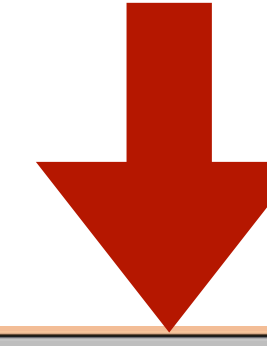
Also considering a 3rd prototype “**Insulated digital**” approach

- 80 SiPMs passive-ganging => 2 active-ganged digitized waveforms
- 280K thermostat. 14-bits @ 80Msps

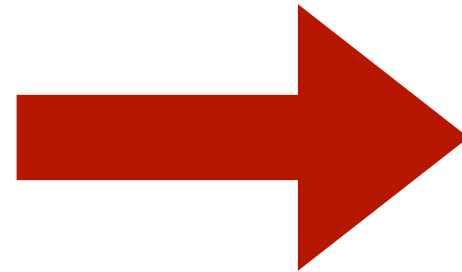


2021 R&D Milestone Timeline

From  Project WBS



Activity			FY21							FY22				
Subsystem or Task	Activity	Notes	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan
Project Management														
==>	Minor Milestone:	Select Control Rx Phase 1 candidate(s). Target 1 candidate.			X									
==>	Minor Milestone:	Select Control Rx Phase 2 candidate(s). Target 1 candidate.				X								
==>	Minor Milestone:	Select Control Rx Phase 3 candidate(s). Target 1 candidate.					X							
==>	Milestone:	Select Control Rx Prototype final candidate.					X							
==>	Minor Milestone:	Select Sync Distribution Phase 1 candidate(s). Target 1 candidate.				X								
==>	Minor Milestone:	Select Sync Distribution Phase 2 candidate(s). Target 1 candidate.					X							
==>	Minor Milestone:	Select Sync Distribution Phase 3 candidate(s). Target 1 candidate.						X						
==>	Milestone:	Select Sync Distribution Prototype final candidate.						X						
==>	Minor Milestone:	Select Analog/Digital Waveform Optical Tx Phase 1 candidate(s). Target 1 candidate.		X										
==>	Minor Milestone:	Select Analog/Digital Waveform Optical Tx Phase 2 candidate(s). Target 1 candidate.			X									
==>	Minor Milestone:	Select Analog/Digital Waveform Optical Tx Phase 3 candidate(s). Target 1 candidate.				X								
==>	Minor Milestone:	Select SERDES Phase 1 candidate(s). Target 1 candidate.		X										
==>	Minor Milestone:	Select SERDES Phase 2 candidate(s). Target 1 candidate.			X									
==>	Minor Milestone:	Select SERDES Phase 3 candidate(s). Target 1 candidate.				X								
==>	Minor Milestone:	Select ADC Phase 1 candidate(s). Target 1 candidate.		X										
==>	Minor Milestone:	Select ADC Phase 2 candidate(s). Target 1 candidate.			X									
==>	Minor Milestone:	Select ADC Phase 3 candidate(s). Target 1 candidate.				X								
==>	Major Milestone:	Pair-wise integration of most promising phase 1 candidate components and Power-over-fiber.				X								
==>	Milestone:	Analog Front-end integration Prototype in cold validated.					X							
==>	Milestone:	SERDES Tx integration Prototype in cold validated.					X							
==>	Milestone:	SERDES Rx integration Prototype in cold validated.					X							
==>	Major Milestone:	Downselect ADC/SERDES/digital Tx or analog Tx Prototype final candidate.					X							
==>	Major Milestone:	ADC+SERDES+Optical Rx/Tx integration Prototype OR Analog Optical Tx integration Prototype in cold validated.						X						
==>	Milestone:	1-channel waveform readout integration Prototype in cold validated.						X						
==>	Major Milestone:	Full modules waveform readout integration Prototype in cold validated.							X					
==>	Major Milestone:	Two synchronized integration Prototype modules in cold validated.							X					
==>	Milestone:	Two synchronized integration Prototype modules in cold <10KV plane validated. Or documented as not needed.							X					
==>	Major Milestone:	Two Prototype v1 modules installed at CERN Cold Box Test Part-A.								X				
==>	Major Milestone:	Two Prototype v2 modules installed at CERN Cold Box Test Part-B.										X		
==>	Major Milestone:	Synchronized waveform readout of two Prototype modes in CERN Cold Box Test.											X	



R&D Group: Cold Electronics and Transmission, Prototype Detector, Prototype Performance Simulation&Requirements Study

- Participating Institutions:

FNAL-AD, -PPD, -SCD (EE Dep.t's) and -ND, CSU, UCSB, APC-Paris, SMU, U. Mi-Bicocca, INFN-Mi, BNL, UNICAMP, UFSC, UFABC, UTFPR, UNIFAL, CERN

- Expressing interest to join:

ANL, Syracuse U., U of Iowa, CIEMAT, IFIC-Valencia, U. Of Indiana, U. of Illinois-UC, INFN-Napoli, Edinburgh, RAL, FZU-Prague,

R&D Activity: 2 weekly Meetings
with Technical Information Repository

The screenshot shows the Indico website interface for the 'VD PhDet PoF&CE' group. The top navigation bar includes 'Home', 'Create event', 'Room booking', and 'My profile'. The main content area displays a calendar view of meetings from April 2021 back to November 2020. The meetings are organized by month, with the most recent meeting on April 21, 2021, marked as 'NEW'. The sidebar on the right lists 'Managers' (including Alan Prosser, Dante Totani, etc.) and 'Materials' (including various PDF documents and images related to the project).

Achievements from R&D in Progress

⇒ **PoF for SiPM demonstrated (optimization in progress), PoF for CE in progress (easier for Analog CE option)**

⇒ **xARAPUCA tile (new design) ⊕ ANALOG CE/Transmission: prototype#1 seems achievable in time for ColdBox test (Fall 2021)**

⇒ **Digital CE/Transmission (prototype#2) - validation in Cold in progress (fast development w/ very encouraging results):
prototype#2 for ColdBox in the plan**

Boundary Conditions are met

⇒ **PoF for PD CE and SiPMs: estimated Power budget is within limits for power dissipation in LAr**

⇒ **Cost envelop for VD PD for both Reference and Backup solutions within current limits for the US project. Resources from
International expected (under negotiations w/ funding agencies)**

⇒ **VD PD core-group from US, EU and International created and included within the existing DUNE PD Consortium.
Existing Groups are growing with new highly qualified resources, and new Groups are showing interest to join**

The R&D path and achievements so far

xARAPUCA: from HD Bar to VD Tile

New generation xARAPUCA technology - Large Tile (60x60 cm²) - 160 SiPM (40 SiPM/side - all 4 sides) in single Channel (MegaCell): design fully developed [CSU: mockup in production], validated by dedicated MC study (efficiency-Brz Grp.s), optimized with new HQE WLS plates (Mi-Bicocca) + improved SiPM-WLS Optical contact (Flex Kapton PCB mounted SiPM - Mi-Bicocca and CSU)

- Improvement: projected efficiency $\geq 3.5\%$

SiPM Passive ganging Stage

8 Groups of 20 SiPM in a (new) hybrid (4 Parallel x 5 Series) ganging [FNAL, UCSB], lower capacitance (compared w/ traditional passive ganging), signal fall time shorter, signal amplitude larger - at common Bias V for single SiPM, validated by SPICE simulation [Mi, FNAL], test board in production [FNAL-SCD, BNL], Flex PCB integrated on xARAPUCA frame.

- Improvement: projected S/N > 5 , 20 SiPM passively ganged.

Active ganging + Ampli Stage

Analog F/E - Cold OpAmp validated in cold [different options available] - goal: 8 groups of 20SiPM summed into one channel (OpAmp), test board in preparation with selectable n. of groups (up to 8). Additional Cold OpAmp options can be considered before final selection.

- Improvement: projected $\sum 160$ SiPM (8 x 20) \rightarrow single channel

OR

Analog Signal Transmission

AnalogDriver + LightSource + Opt.Coupling to Fiber

COTS Laser Diode validated in Cold, in-house made AnalogDriver tested ok in Cold, Opt.Coupling under development (DS-style connector) [APC-Paris + support from DS, + support from FNAL]

- Analog Transmission: full-chain Validation in Cold expected by May/June.

Clock

Digital Conversion Stage and Data Aggregation

COTS ADC selection, tests and validation in Cold [different options available, 14 bits, 80 MSPS], test board OpAmp+ADC in preparation/in production, FPGAs selection and test in cold, compression algorithms, insulating techniques, transmission cold qualification (input from BNL, STFC UKRI, LBL, FNAL)

Digital Signal Transmission

DigitalDriver + LightSource + Opt.Coupling to Fiber

COTS Laser Diodes selection, tests and validation in Cold, modified COTS DigitalDriver 10 GBPS ADN2526 first test in Cold OK, Opt.Coupling & Fiber selection in progress [FNAL & SMU + support by Versatile Link Plus Collaboration @ CERN]

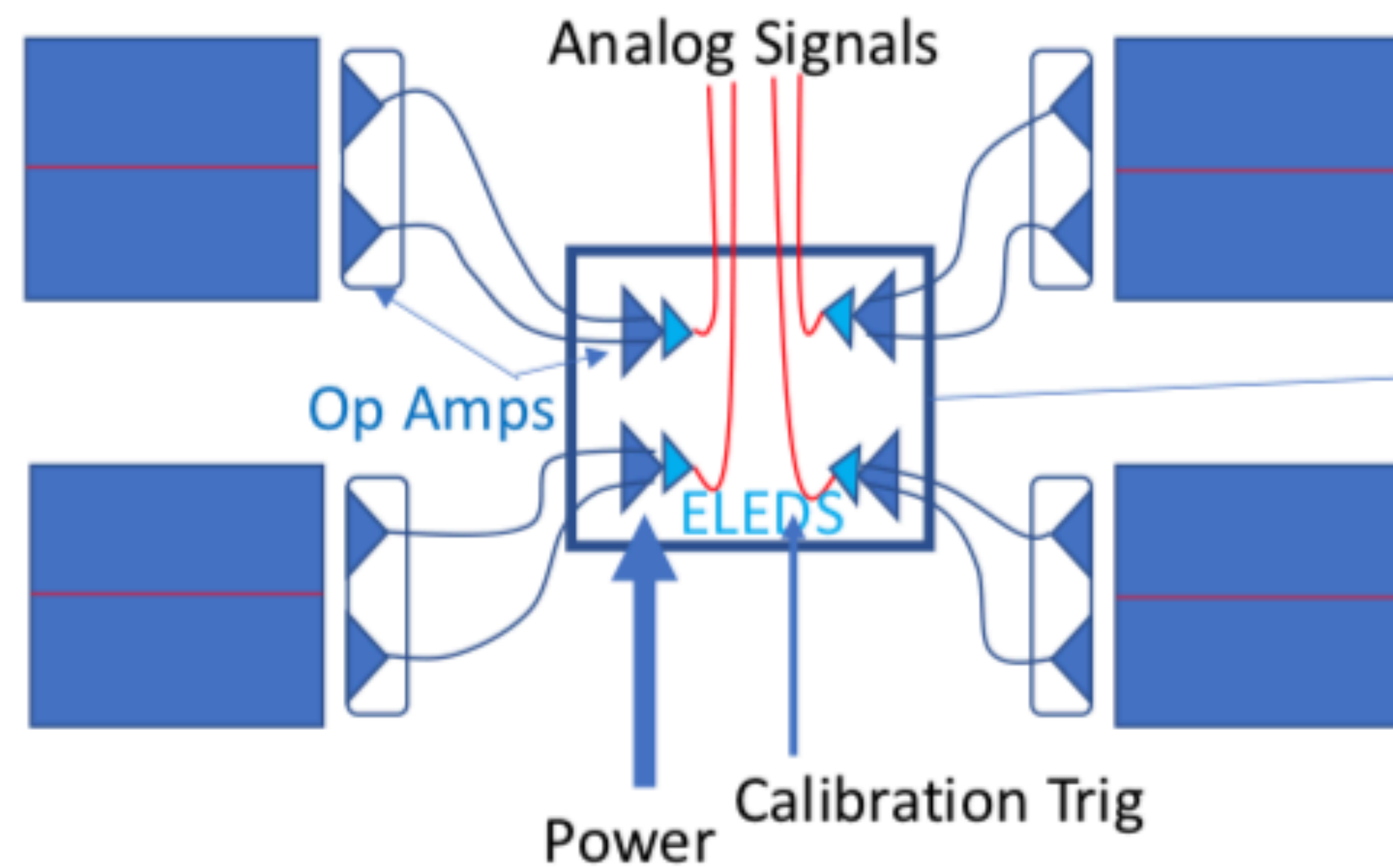
- Digital Transmission: full-chain in progress, Validation in Cold expected by June/July.

BACKUP

● PD Reference design for the VD LAr Volume

	Detector Component/Feature	Parameter	Demonstration
Technical Requirements	Scintillation medium composition	Ar+Xe(10 ppm) (Ar Slow-component full transfer to Xe)	<i>protoDUNE</i>
	X-ARAPUCA Technology Choice SiPM + Electronics read-out X-ARAPUCA efficiency PoF - Power Transmission PoF - Signal Transmission	S/N ≥ 5 $\epsilon_D=3\%$ Conversion Effic. 22% Usable Pwr: 4 W/PoF-Unit stability, noise at $V_{out} \sim 50V$	<i>protoDUNE + prototype Tests</i> <i>protoDUNE + prototype Tests</i> <i>prototype Tests - FNAL</i> <i>prototype Tests - FNAL, CERN</i> <i>prototype tests - ongoing CERN</i> <i>prototype tests - planned</i>
	PDS Light Yield	$\langle LY \rangle \simeq 60$ $LY_{min} \simeq 30$	<i>from MC study</i> <i>from MC study</i>
Expected Performance	Spatial resolution Energy resolution Time resolution	$\sigma_r \leq 0.7 \text{ m}$ ($E_{dep} \geq 5 \text{ MeV}$) $\sigma_E/E \leq 10\%$ ($E_{dep} \geq 5 \text{ MeV}$) $\leq 200 \text{ ns}$ (to be confirmed)	<i>from MC study</i> <i>from MC study</i> MC study - ongoing

Electronics Box



- Each Arapuca transmits two analog signals to the electronics box
- A summing amp combines both analog signals
- An analog transmitter, Tx (and conditioning electronics) transmits
- A calibration circuit (receives an ext. trig and plays a ramp into Tx)

This configuration will require 320 ELEDs/Cables - Verses 640 if each channel has a analog transmitter
Power for the op amps near the Arapuca may come from SiPM power units
Power for op amps and transmitters in the electronic box will come from power voltage fanout

Vertical drift single phase LArTPC:

the Photon Detector Project

Project High Level Activity Plan

From  Project WBS

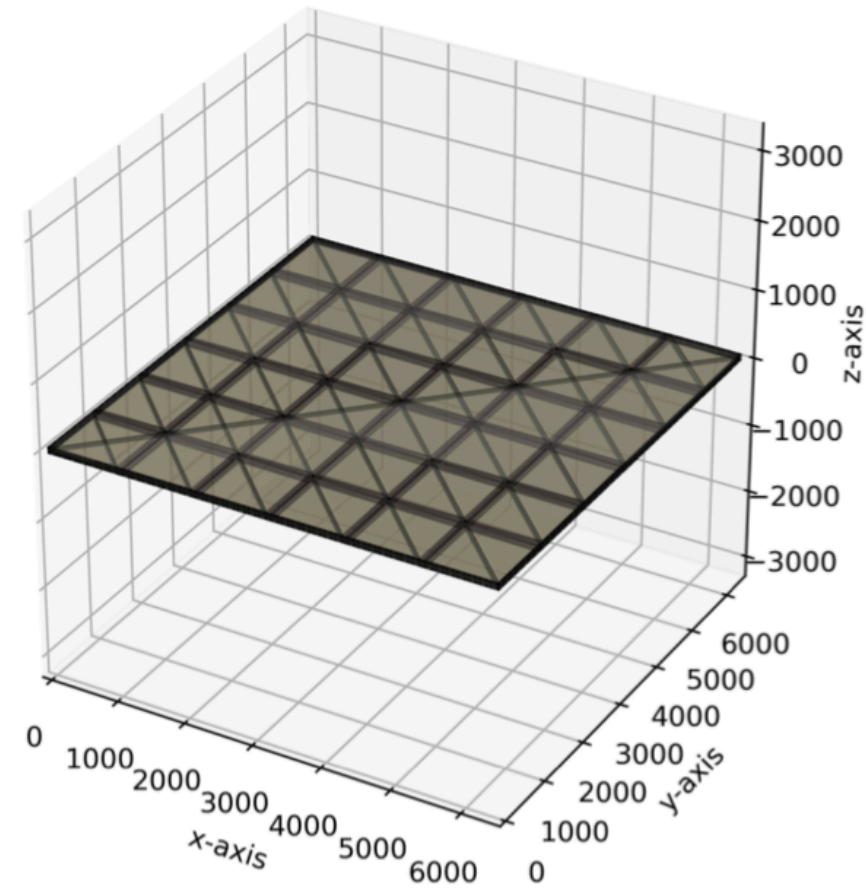
Date Range	High Level Activity
FY21	Prototype design R&D and prototype v1/v2
October 2021	Project Conceptual Design Report (CD-1)
End-of-2021	Subsystem Preliminary Design Review (60% design)
FY22-23	Long-term Cold Studies and prototype v3/v4
January 2023	Final Design Review (90% design)
Summer 2023	Characterize 1/20 th pilot “module 0” at ProtoDUNE2
End-of-2023	Production Readiness Review
FY24-26	Production phase
FY27	Installation begins
FY28	Installation complete
FY29	Commissioning detector

ProtoDUNE2 and Production Milestones

Baseline Date	Milestone
Summer 2023	T4 Milestone: 1/20 th scale ProtoDUNE2 pilot system commissioned.
End-of-2023	T4 Milestone: Vertical Slice Test complete
October 2023	T4 Milestone: All Production Readiness Reviews complete
January 2027	T4 Milestone: 50% of Production Tile Assemblies constructed.
January 2028	T4 Milestone: 100% of Production Tile Assemblies constructed.
Spring 2027	T4 Milestone: 50% of Production Tile Assemblies shipped to US Reception Facility.
Spring 2028	T4 Milestone: 100% of Production Tile Assemblies shipped to US Reception Facility.
Summer 2027	T4 Milestone: 50% of Production Tile Assemblies installed.
Spring 2028	T4 Milestone: 100% of Production Tile Assemblies installed.
Winter 2027	T4 Milestone: 50% of Production Tile Assemblies integrated.
Summer 2028	T4 Milestone: 100% of Production Tile Assemblies integrated.
Summer 2028	T4 Milestone: Cathode PDS commissioned
Summer 2028	T4 Milestone: Membrane PDS commissioned
Fall 2028	T4 Milestone: FD-2 PDS commissioned.

METTERE IN BACK-UP?

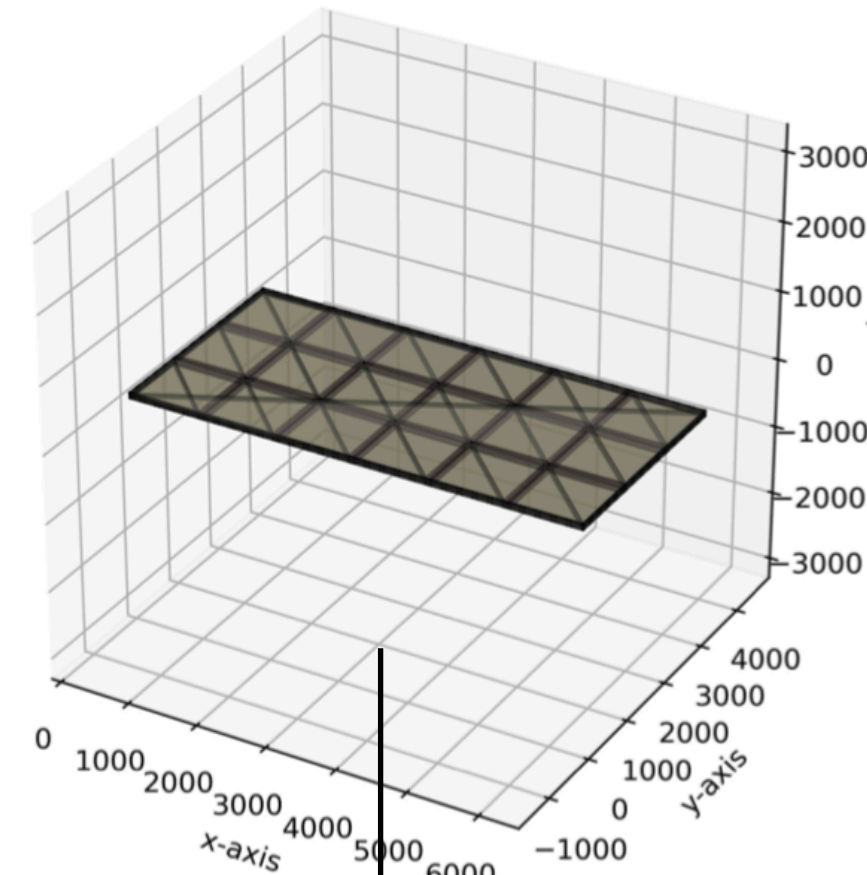
36 Filters with 144 SiPMs. $\delta = 0.6 \frac{\text{SiPM}}{\text{cm}}$, 36 SiPM/side.



Efficiency: 36,51%

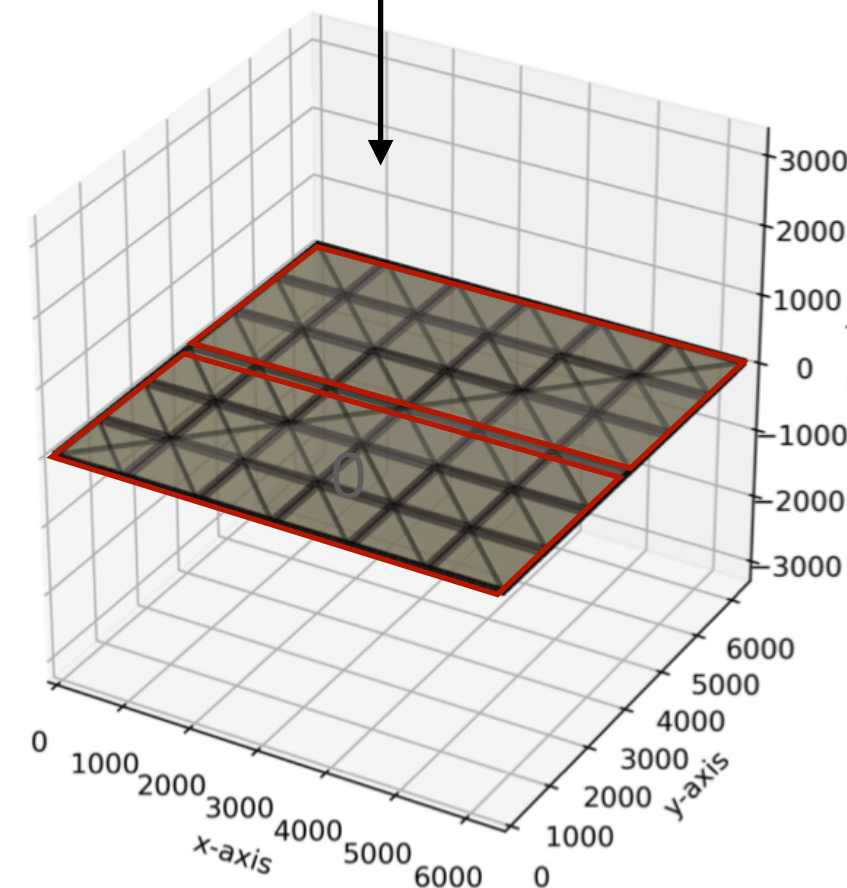
Dichroic Filters 10cm x 10cm
60cm x 60cm x 0.4cm thick light-guide
SiPMs around Perimeter

18 Filters with 108 SiPMs. $\delta = 0.6 \frac{\text{SiPM}}{\text{cm}}$, 36 SiPM/L-side, 18 SiPM/S-side.



Efficiency: 40,5 %

x 2



108 SiPM x 2 = 216 SiPMs (per 60x60 cm tile)

Relative Increase N. SiPMs $(\frac{N_2 - N_1}{N_1})$: +50%

Relative Efficiency $\frac{(\epsilon_2 - \epsilon_1)}{\epsilon_1}$: + 10%

(ϵ_D) does **not** go linearly with the number of SiPMs)

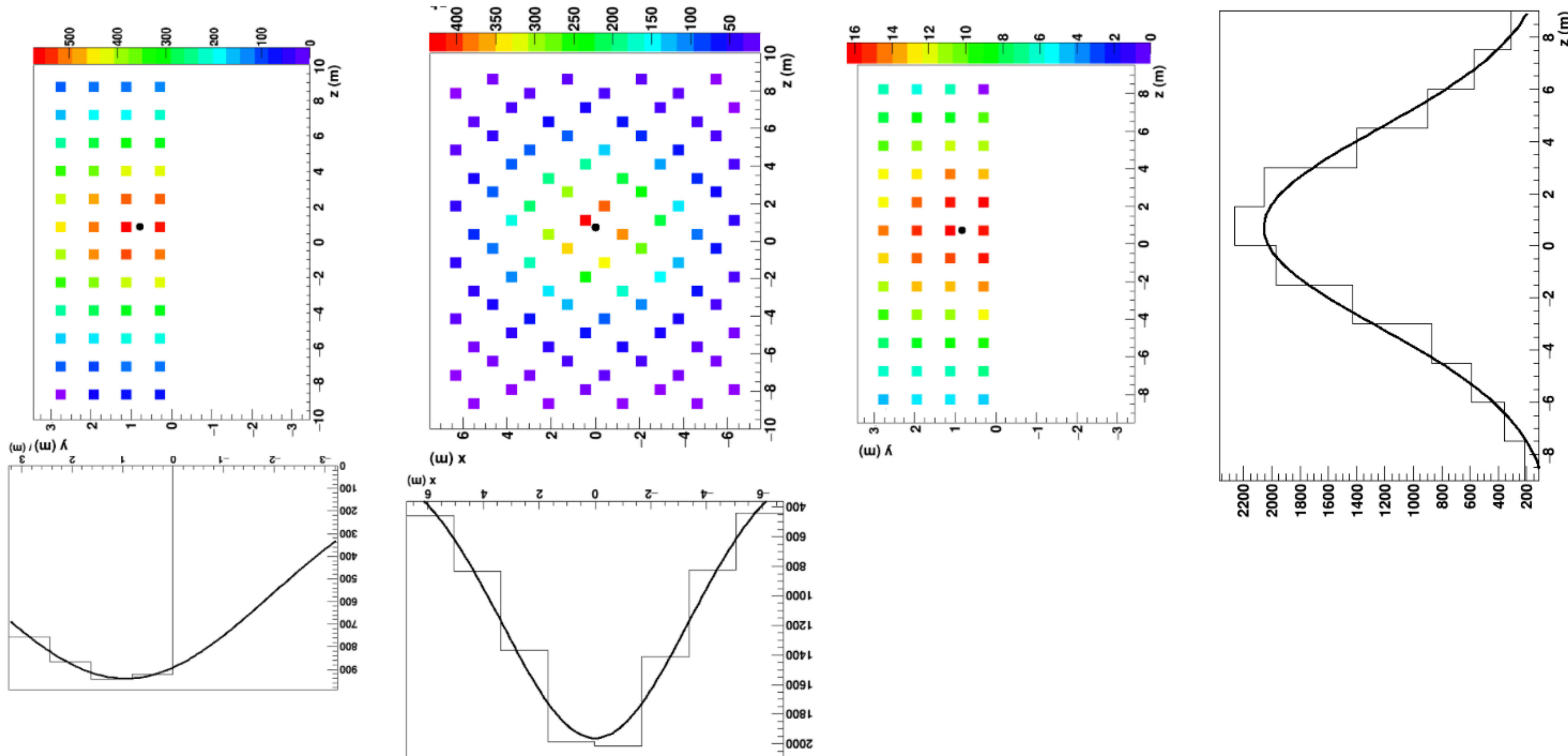
Note: If keep same N. of SiPM (144), effic. drops by 11%

Simulations

Preview of main goals and current implementations

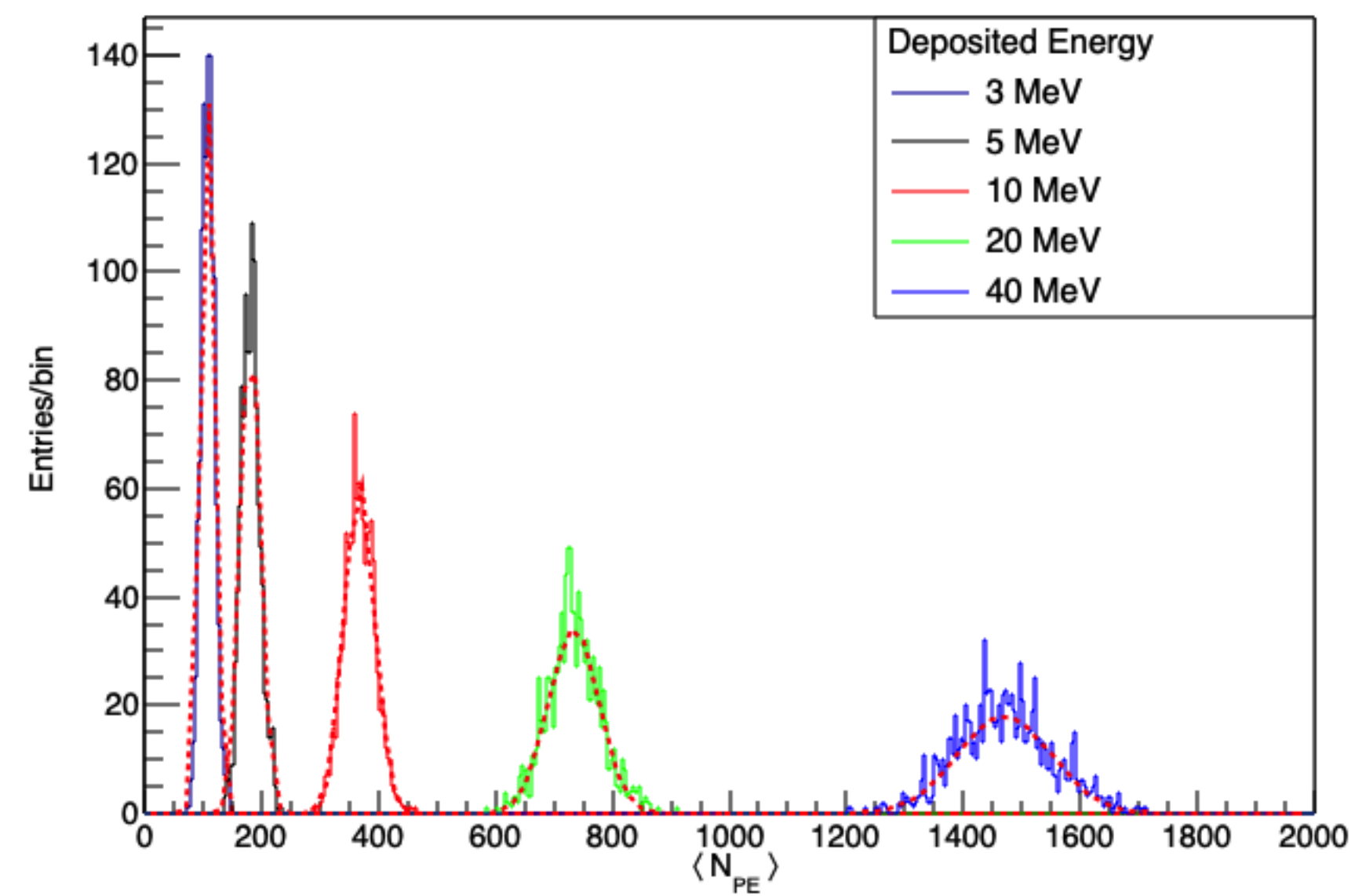
Position reconstruction from barycenter

Position taking from analysing the pe seen by each line/row of PDs on the three planes and the point from where we shot the photons. What is shown is the pe map on each plane and the integrated values over x, y and z. Assuming 3% PD efficiency.

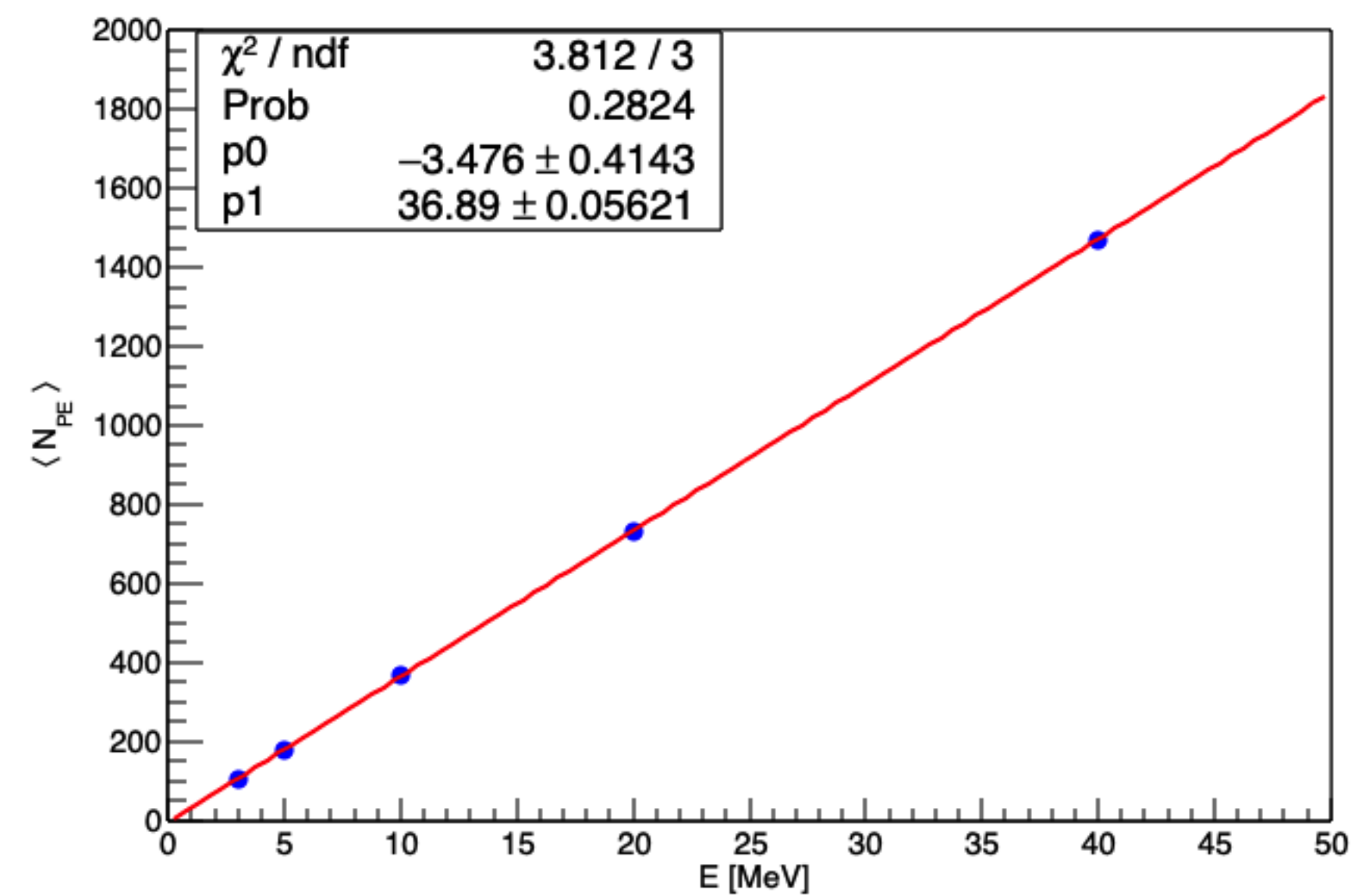


Energy Reconstruction and Resolution

Simulated Photon Detected



PD Energy Response



Requirements:

- Comparison w/ Horiz. Drift (Light Yield, E resolution for HD and direct comparison for VD-Reference option and fall-back option)
- Additional timing resolution requirement based on vertexing?
- Digitizer requirements (dynamic range, sampling freq., bandwidth)

Detector parameters open to optimization:

- Detection of Ar (only), Ar+Xe, Xe-only Light
- 1-sided vs. 3- sided vs 5-sided
- w/ or w/o reflections from the Anode
- Transparent Cathode vs Opaque or Reflective Cathode

Simulation Development (LArSoft): *PARTIALLY DONE*

- VD geometry --> DONE
- Fast simulation --> ON THE WAY
- Xe timing parameterization --> DONE (adjustable parameters, including N2 in progress)

Plan for this year

- LArSoft simulation available
- PD Trigger (and prompt Bckgd Rejection) Strategy combined with existing TPC Trigger Strategies
- Goals for SNe and p-decay detection w/ PD:
 - minimum (t0)
 - enhanced physics (supernova neutrino background, NS cooling, ...)
- Backgrounds
- ~~Other Low En UG Physics (eg Solar neutrinos)~~