Test results for ADCs and FPGA in LN2

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DUNE Collaboration Meeting

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ADC selection

We checked different evaluation boards that were easy to test and available in the market.
Key elements were:

- Low power
- 12-16 bit (Goal: 14-bit)
- 65-125 Msps (Goal: 80 Msps)
- Low jitter

Test performed

We used 2 different adc evaluation boards:

- DC1620A-G from Analog Devices that uses LTC2145-14   (2-ch, 14-bit)
- ADC3244EVM from Texas Instruments that uses ADC3244   (2-ch, 14-bit)

We checked for operation on LN2 by using an external 100 MHz clock and a sinusoidal analog input signal of 10 MHz and 1 Vpp amplitude.

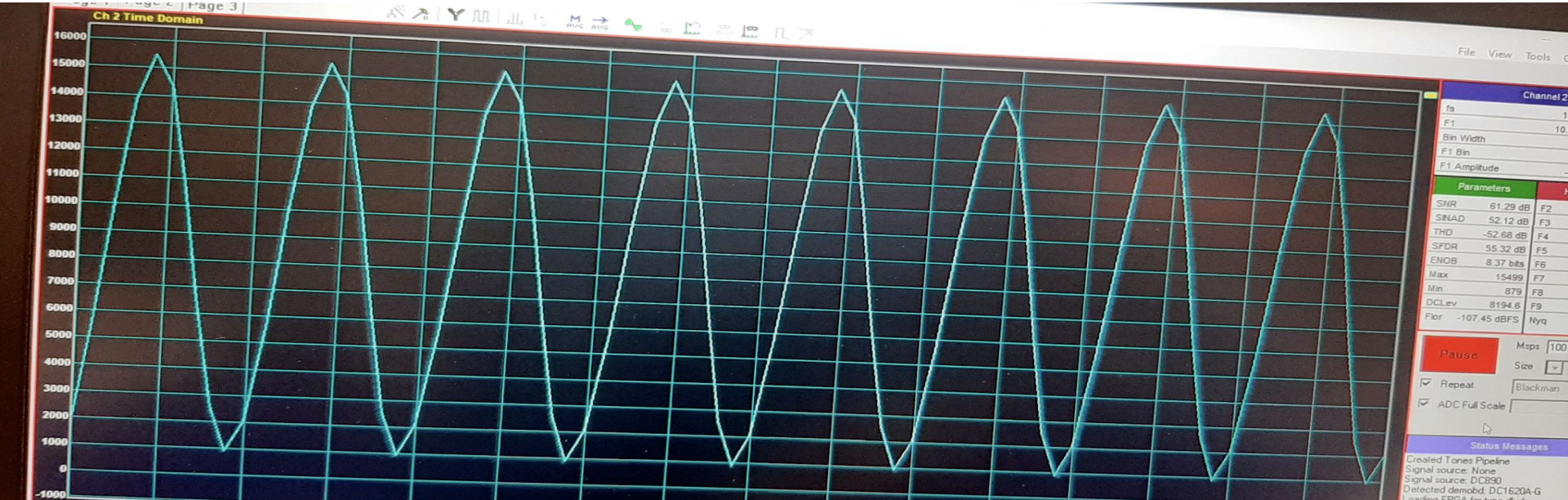Power consumption was also registered for cold and warm operations.

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Test for DC1620A-G from Analog Devices

As the picture shows, only the lower section of the board was put into LN2, most notably the LTC2145-14 ADC.

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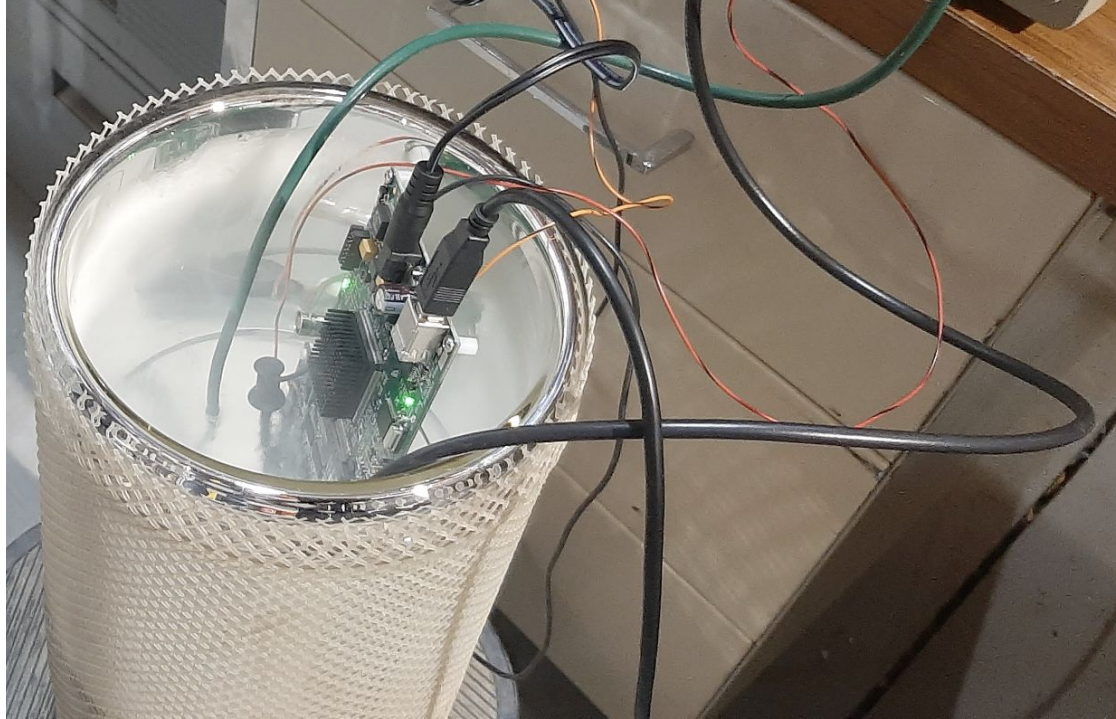
Test for DC1620A-G from Analog Devices

LTC2145-14 ADC functioned in the cold (tested for an hour) and survived power cycling.

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Test for DC1620A-G from Analog Devices

We had to bypass evaluation board LDOs to get this signal, so we obtained two different current values from two separate power supplies as shown in the following table (standard values shown):

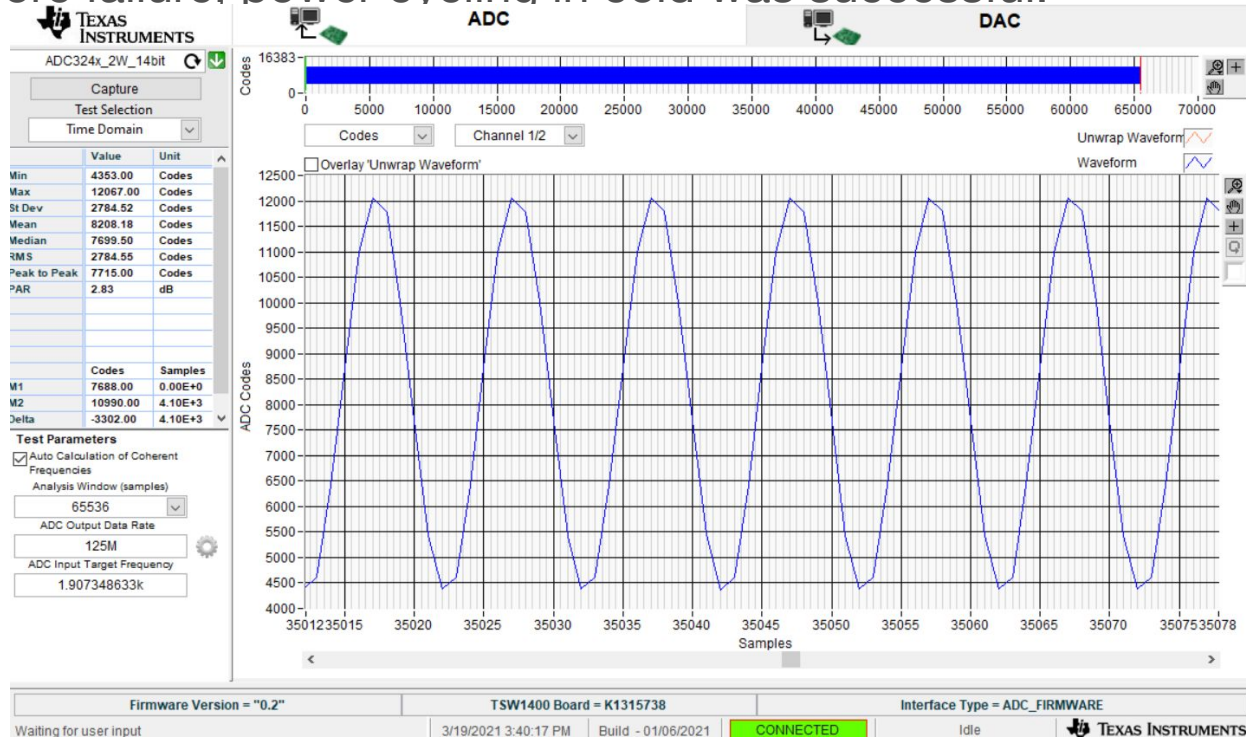|	Warm condition	Cold condition
Voltage supply		
3,3 V	32 mA	30 mA
1,8 V	128 mA	116 mA
Total power consumed	0.34 W	0.31 W

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Test for ADC3244EVM from Texas Instruments

Again, LN2 did not cover all of the evaluation board.

Test for ADC3244EVM from Texas Instruments

ADC3244 ADC functioned for ~30 minutes, then the main evaluation board stopped working. Before failure, power cycling in cold was successful.

Test for ADC3244EVM from Texas Instruments

We had to bypass LDOs to get this signal, so we obtained two different current values from two separate power supplies as shown in the following table (standard values shown):
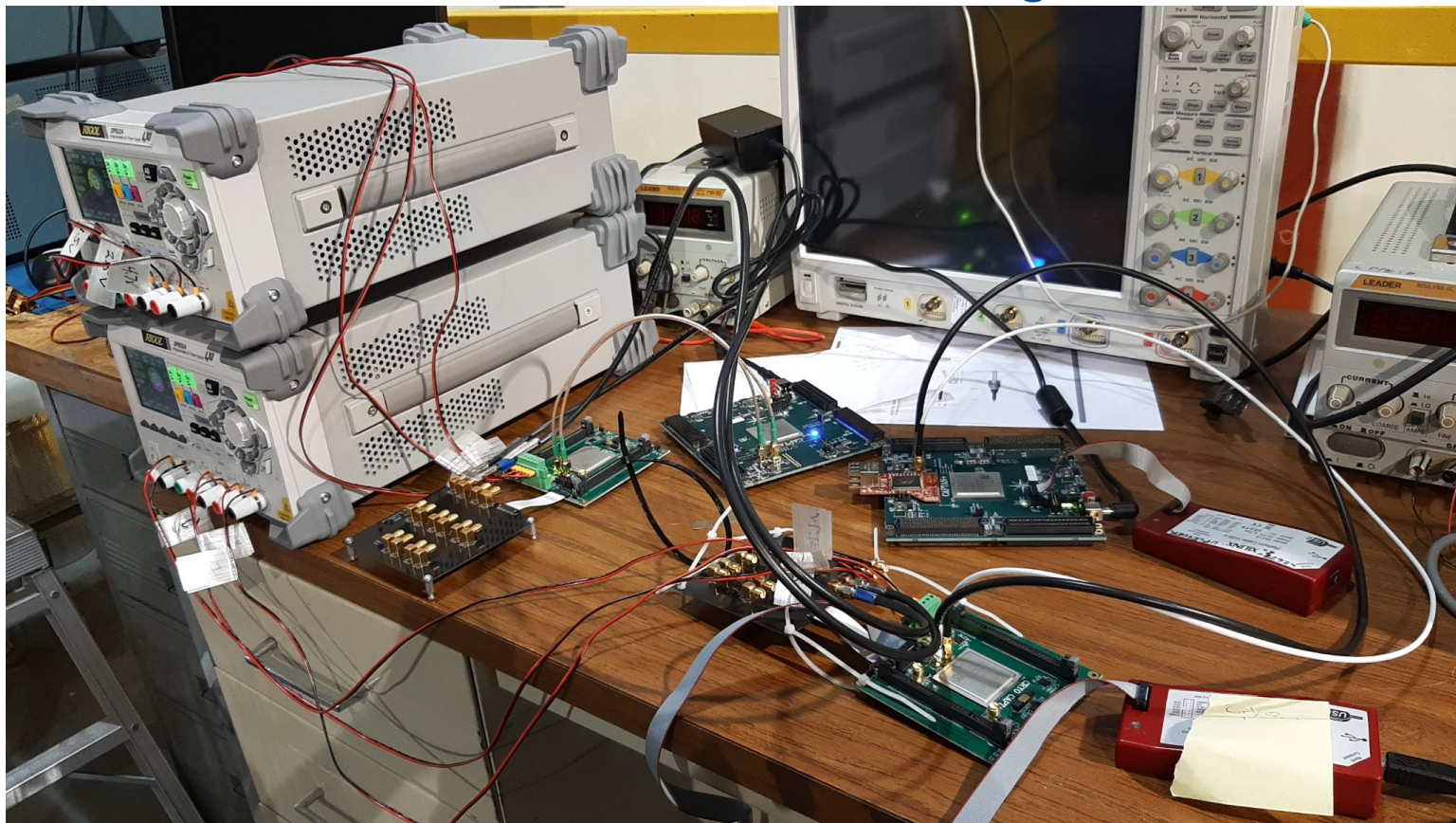
	Warm condition	Cold condition
Voltage supply		
3,3 V	25 mA	22 mA
1,8 V	114 mA	106 mA
Total power consumed	0.29 W	0.26 W

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FPGA Test in LN2

Tested CryoCAPTAN in LN2. CryoCAPTAN is custom FPGA card developed at Fermilab based on Xilinx Artix-7 FPGA and SODIMM daughter card connectors. BNL has used it at 4 K.

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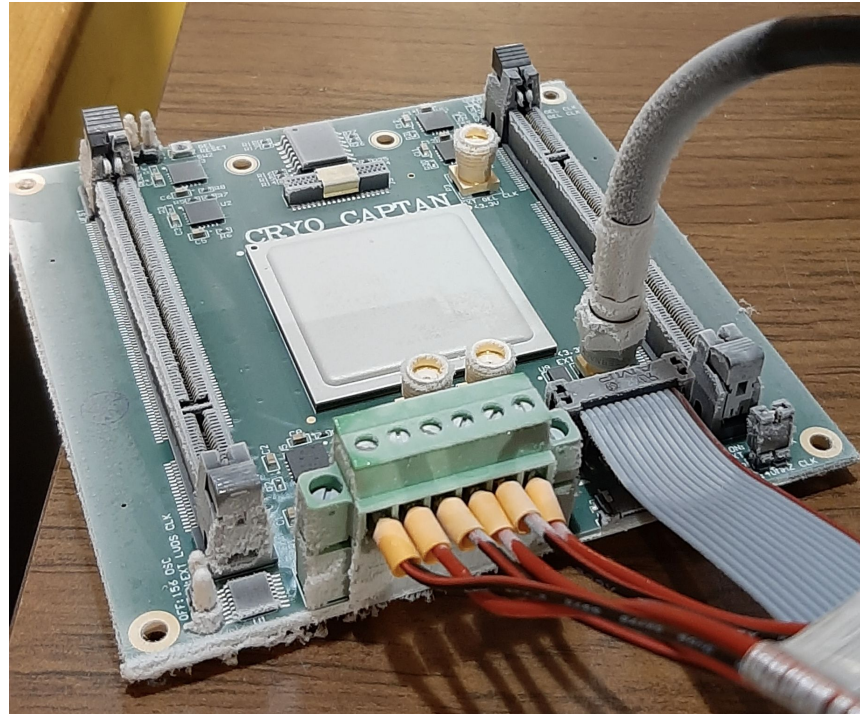
Tested transmission in LN2 using SERDES

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Test performed

- Transmission from LN2, reception in warm conditions.
- Used two CryoCAPTANs with the same firmware using ch-0 high-speed SERDES pins.
- Checked number of errors with three different frequencies.
- Ran some Eye tests with different dwell Bit Error Rates (BER)
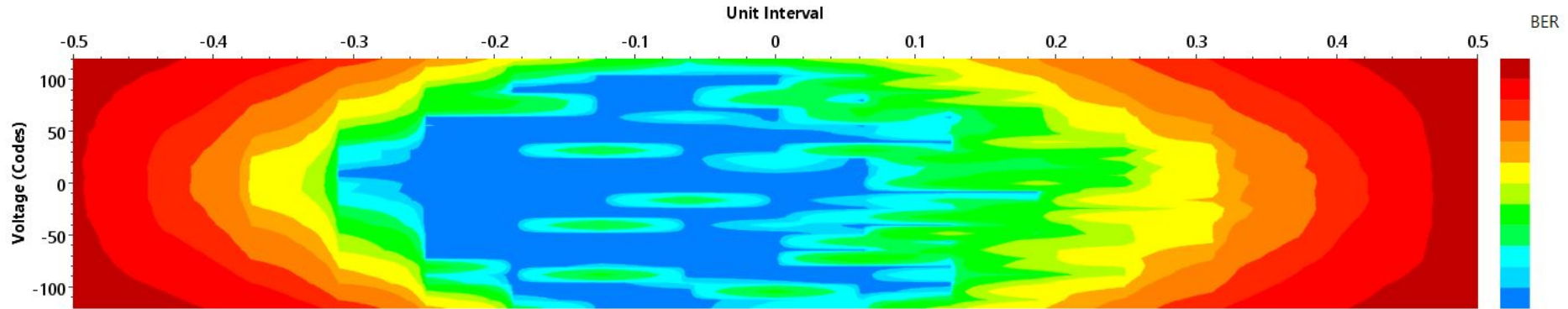
🐝 **Fermilab**
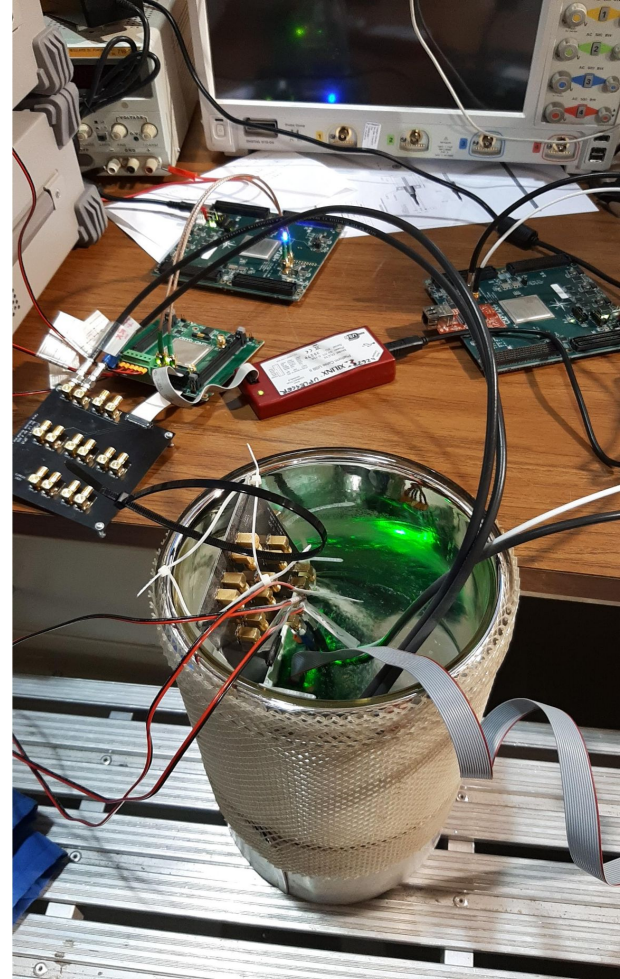
Power consumption

This FPGA needs 3 different power supplies, so electrical current for each one was measured and shown in this table. Transmission speed: 3.125 GHz.

	Warm condition	Cold condition
Voltage supply		
4,7 V	280 mA	224 mA
2,5 V	110 mA	115 mA
1,5 V	985 mA	746 mA
Total power consumed	3.07 W	2.46 W

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First test
3.125 Gbps

Dwell BER of 1 e -11, however we only got portions where BER was 1e -6 or higher.

Summary		Metrics		Settings	
Name:	SCAN_0	Open area:	6528	Link settings:	N/A
Description:	Scan 0	Open UI %:	29.41	Horizontal increment:	8
Started:	2021-May-10 14:39:33			Horizontal range:	-0.500 UI to 0.500 UI
Ended:	2021-May-10 14:39:50			Vertical increment:	8
				Vertical range:	100%

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Second test
6.25 Gbps

Dwell BER of 1 e -5, however we only got portions where BER was 1e -3 or higher.
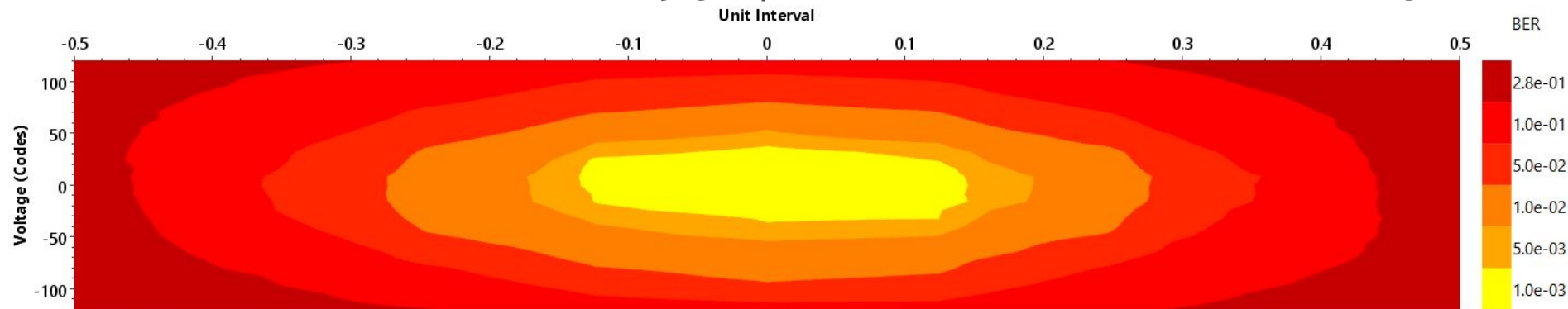
Summary		Metrics		Settings	
Name:	SCAN_1	Open area:	0	Link settings:	N/A
Description:	Scan 1	Open UI %:	0.00	Horizontal increment:	8
Started:	2021-May-10 15:11:37			Horizontal range:	-0.500 UI to 0.500 UI
Ended:	2021-May-10 15:11:44			Vertical increment:	8
				Vertical range:	100%

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Third test
1.25 Gbps

Dwell BER of 1 e -10.

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Third test
1.25 Gbps

Dwell BER of 1 e -10.

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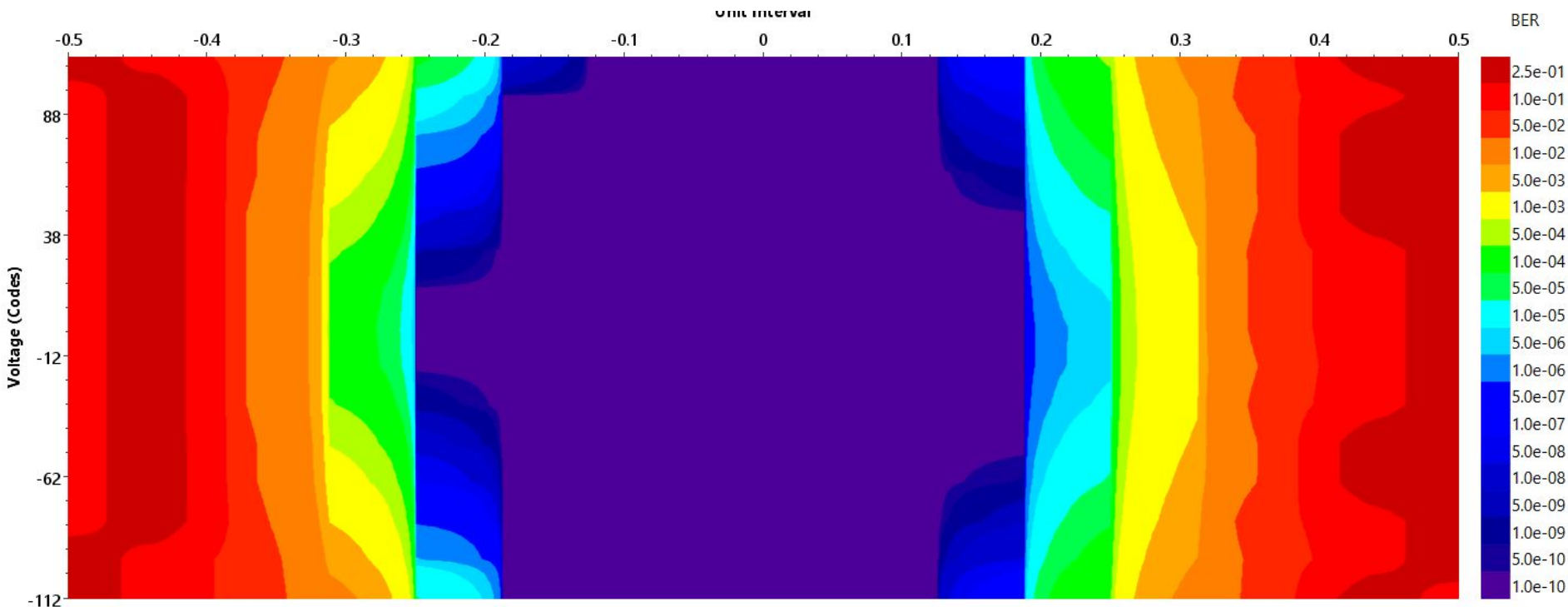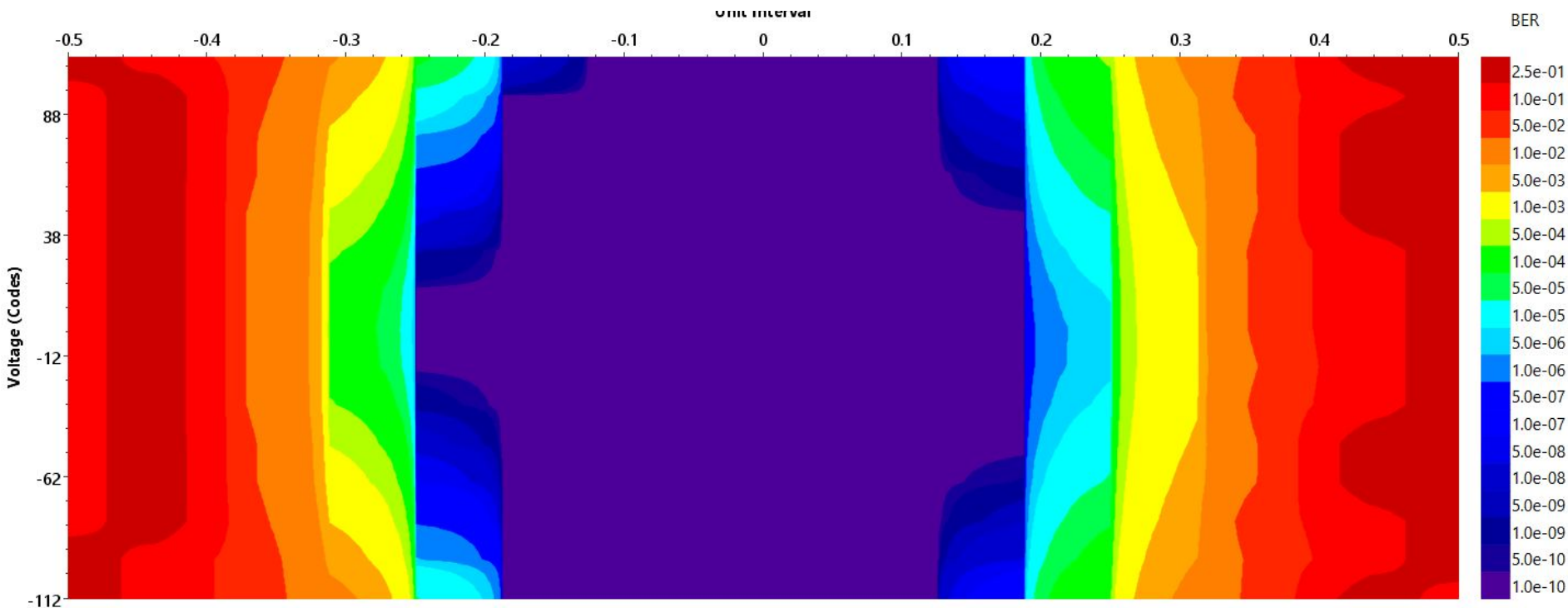
Cold electrical Rx test

Still investigation, no successful transmission yet.

We tried to receive a signal in cold at 6G, 3.125G, 1.25G, 0.625G with no success.

	Tcl Console	Messages	**Serial I/O Links**	×	Serial I/O Scans	

Name	TX	RX	Status	Bits	Errors	BER
📁 Ungrouped Links (0)						
∨ 🔗 Link Group 0 (1)						
🔗 Link 0	MGT_X1Y3/TX	MGT_X1Y3/RX	0.401 Gbps	1.884E10	2.441E9	1.296E-1

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Conclusions

- Seems likely some combination of ProtoDUNE2 CycloneIV and CryoCAPTAN could form FD2 PDS FPGA and peripherals solution. Avoid dependence on flash memory and oscillators.
  - Along with ADCs in same family as tested (and also leveraging validation by collaborators).
- Cold SERDES Tx on Artix-7 seems to work.
- Cold SERDES Rx on Artix-7 seems to fail.
- Next Steps:
  - Fabricate two ADC daughter card types for CryoCAPTAN.
  - Get familiarity with testing ProtoDUNE2 Altera CycloneIV (have one at FNAL from BNL)
    - Explore cold SERDES and GPIO
  - Try GPIO cold Rx and Tx of CryoCAPTAN
    - Readout of ADC and general data transmission (Target 100Mbps cold Rx and 1Gbpscold Tx)

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