DUNE FD-2 PDS R&D

Integrated Cold Electronics Readout Scheme and Redundancy Concepts

20 May 2021

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Outline

- Cold Electronics Integration R&D Path to Prototype
- Surviving 30 years

2021 R&D Path to Prototype Strategy

1. Launch small working groups (i.e., one or two experts) for each component in the system to find a viable candidate.
2. Pair-wise integration of viable candidates:
   - E.g., pair power-over-fiber with component
   - E.g., pair SiPMs with passive and active ganging
   - E.g., pair active ganging with analog transmitter
3. Time permitting, consider other viable candidates and optimization (i.e., small working groups continue in parallel)
4. Demonstrate two synchronized prototype detector tiles with readout at CERN Cold Box Test in October.
5. Demonstration sets the stage for December DOE reviews and any desired baseline changes leading into 2022.

Cold Component List

Component	Who
xARAPUCA	Milano/Madrid/Prague, Maura S, Francesco T, Hucheng C
Detector Tile Form-factor	Dave W (w/CSU), Carla C, Bill P, Gustavo C, Dante T, Dave C
Passive/Active Ganging	Dante T, Gustavo C, Dave C
Digital Tx	Alan P, Dave C
Analog Tx	Sabrina S, Jaime D
ADC	Andres QP, Divya S, Jonathan E, Dave N (UK), Hucheng C (BNL)
SERDES/FPGA	Andres QP, Divya S, Jonathan E, Dave N (UK), Hucheng C (BNL)
Optical Rx	Alan P, Divya S
Sync Distribution	Jonathan E
Power Solutions	Bill P, UIUC

- Actively looking to engage additional collaborators in component working groups!
  - Especially where names are repeated and less than 3

R&D Path to Prototype Milestones

Baseline Date	Activities/Milestone
May 2021	T4 Milestone: Pair-wise Short-term Cold Test Validation
June 2021	Launch pre-prototype PCB and CAD designs. Order long lead-time components.
July 2021	T4 Milestone: All-channel Detector + Waveform Transmission prototype validated in short-term cold test.
August 2021	T4 Milestone: Two synchronized tile electronics prototypes short-term validated in cold.
September 2021	T4 Milestone: Ready for CERN Cold Box Test
November 2021	T4 Milestone: CERN Cold Box Tests of two synchronized prototypes complete
January 2023	T4 Milestone: All components validated for 30-years in cold

- In 2022:
  - 2 to 4 additional CERN Cold Box runs
  - Optimize for power draw and redundancy
  - 30-year cold qualification studies

Surviving 30-years

- How do we give ourselves the best chance to survive?
  1. Peer-reviewed qualification results
     - Component-level (possible), System-level (not possible?)
     - Leverage ProtoDUNE and Horizontal Drift designs and expertise
  2. **Redundancy**

What are we worried about?

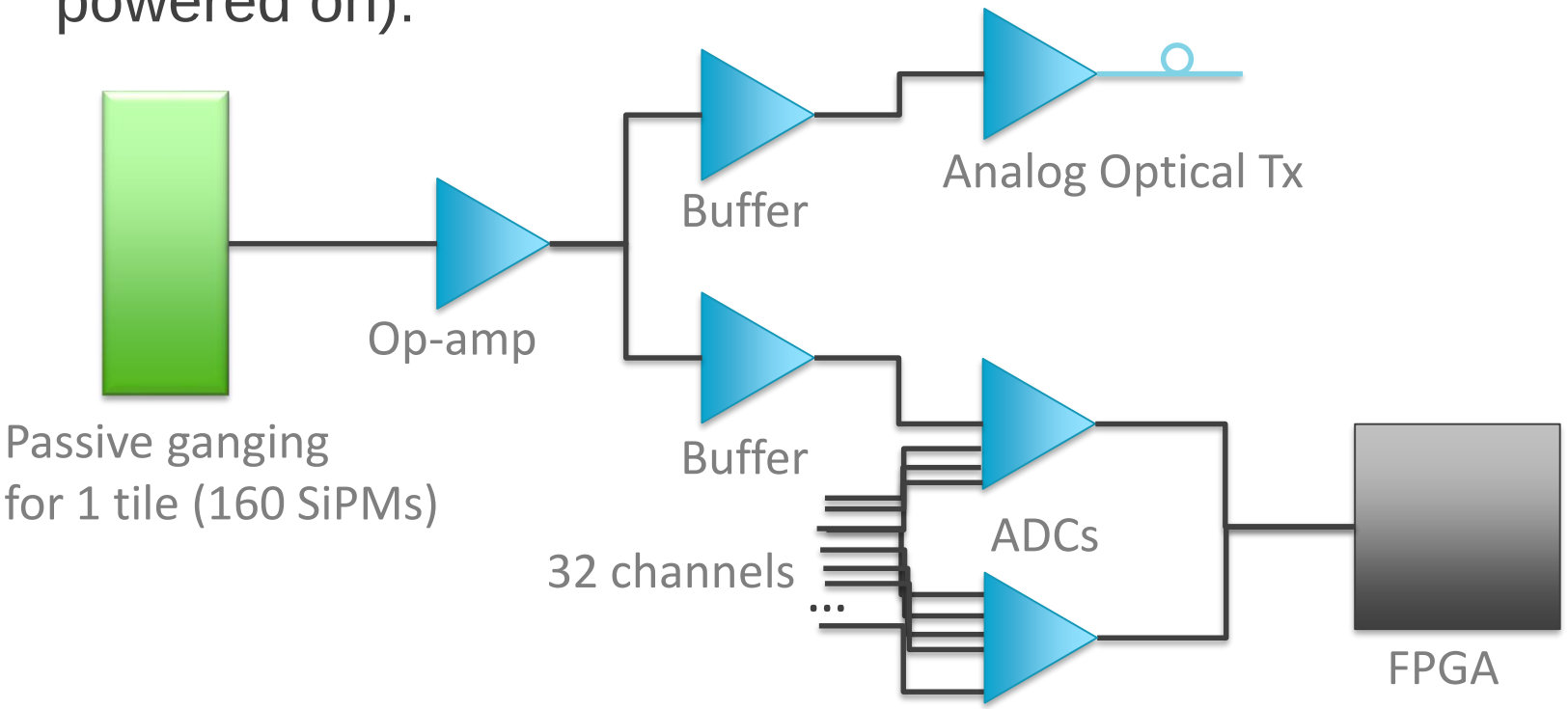
- Worried about NMOS (majority carriers are e^-), not PMOS
  - Kinetic energy acquired higher for e^- than holes for same E-field
- “Hot carrier” effects in CMOS
  - Only a problem when ON (conducting).. For digital only “conducting” is on clock edges/switching.
  - All FPGAs are CMOS
    - FPGA Fabric qualified with invertor ring oscillator and monitoring current draw and frequency variation (< 3%)
    - Smaller feature size seems less affected (but not obvious)
    - Prefer dipping voltage supply (not as easy for smaller feature size)
  - In general, components qualified by stressing supply voltage and monitoring key parameters.
- Not worried about Op-amps, if they work once.
- All bipolar transistors, if they work, they should keep working.

Redundancy Concepts

1. Detector signal handling
2. Digital data transmission
3. Clocking
4. Data reduction
5. SiPM ganging topology

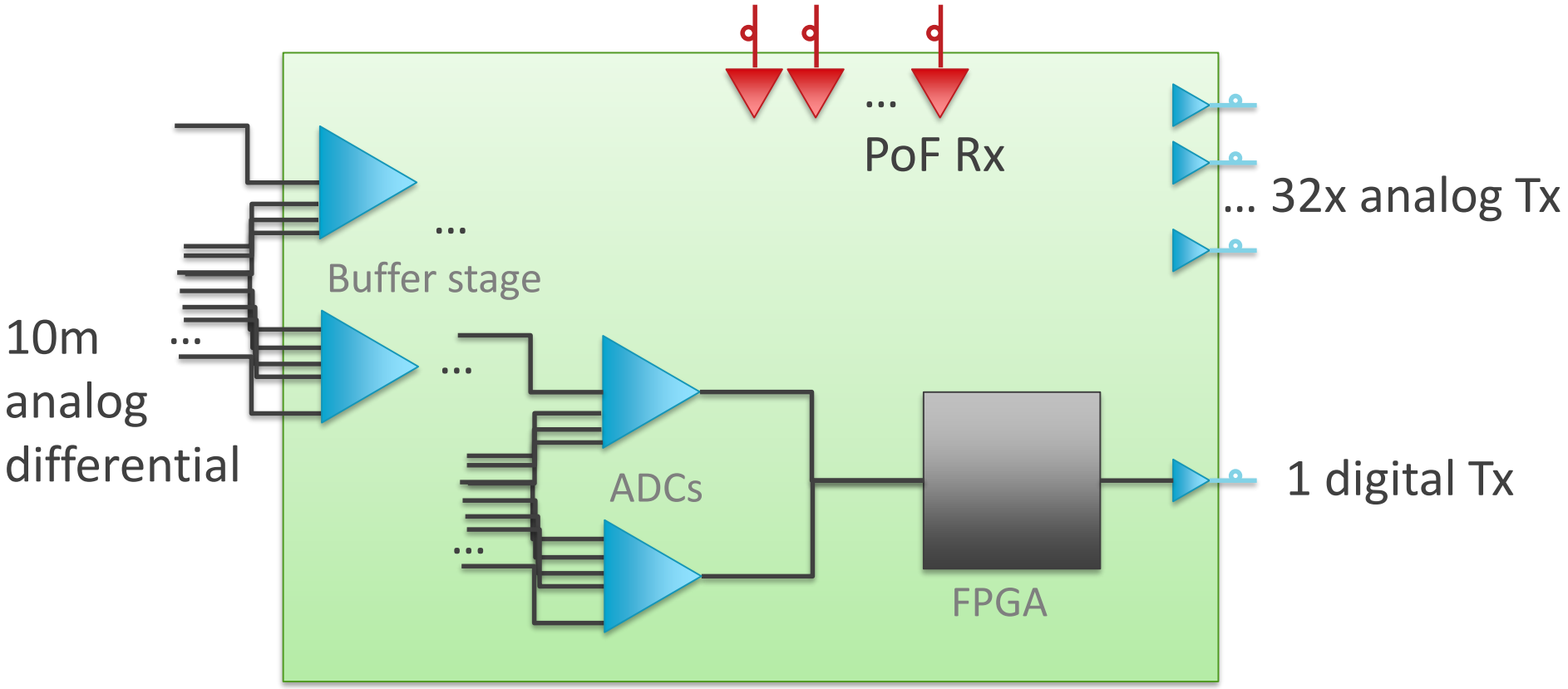
1. Redundant Detector Signal Handling

- Consider doing both analog and digital path (only one powered on):



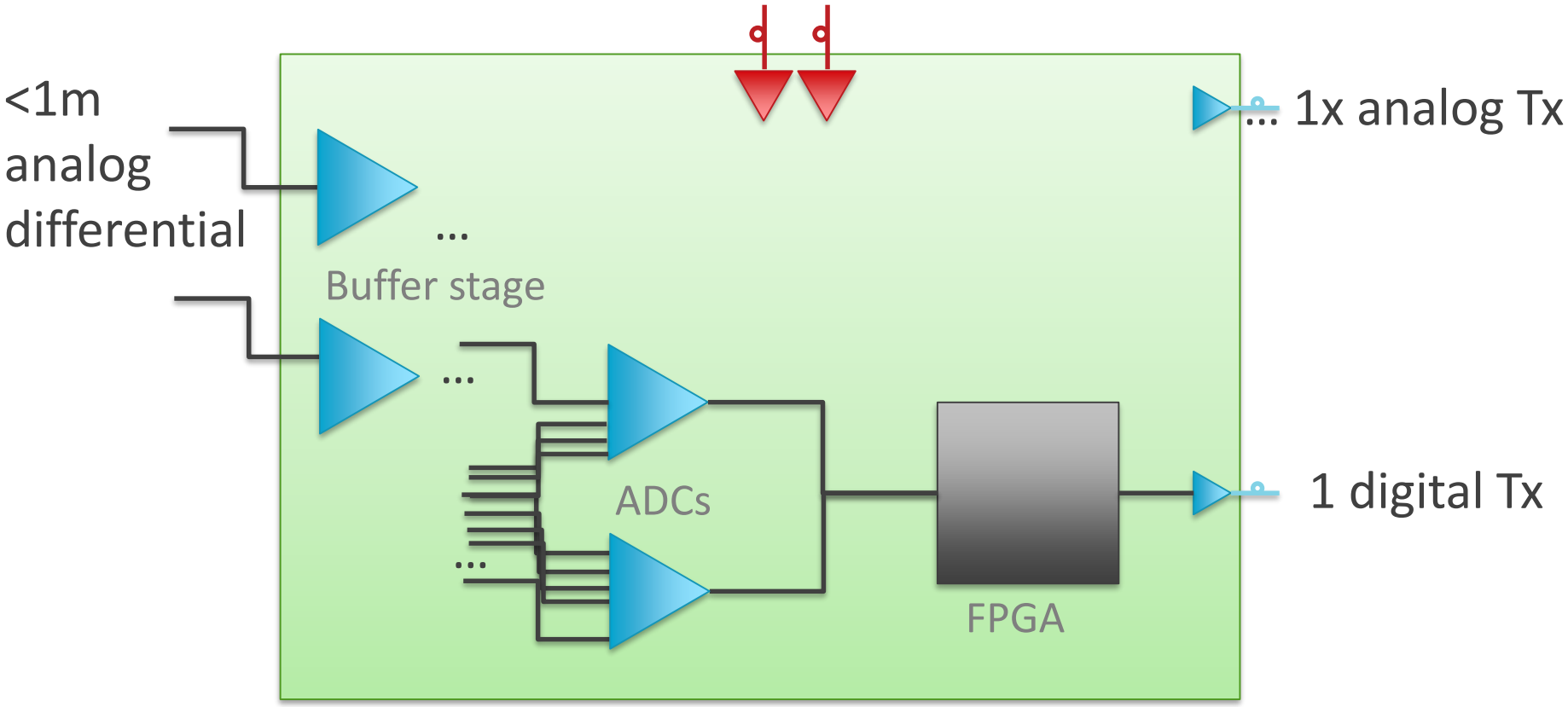
- One analog Tx per tile
- 32 tiles per FPGA (2x 16-channel ADS52J90 ADCs). 10 FPGAs for entire cathode.
  - Could double buffer for 32 tiles ➔ 64 ADC channels. Same power.

Possible 32-tile Cold Electronics Topology



- Do not need duplicate PoF, switch power between the two
  - Enough power for 32 analog transmitters roughly equivalent to 2 ADCs + FPGA?

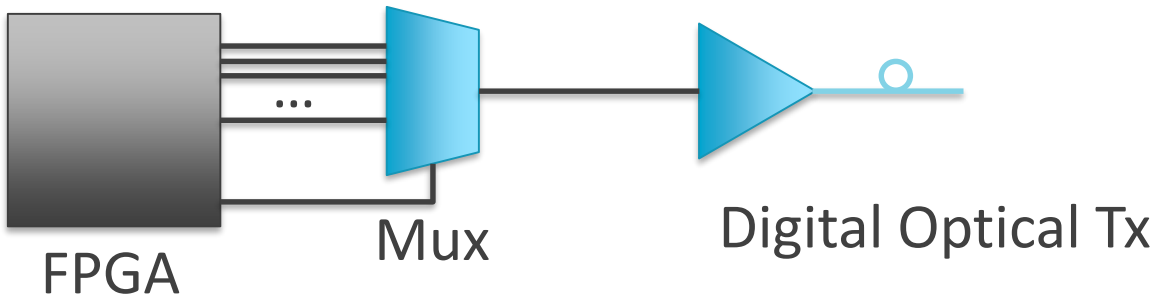
Possible 1-tile Cold Electronics Topology



- Further redundancy if can reduce power overhead of FPGA/ADC and use 1 per tile to not have replication costs blow up.
  - Tradeoffs of centralized vs distributed

2. Redundant Digital Data Transmission

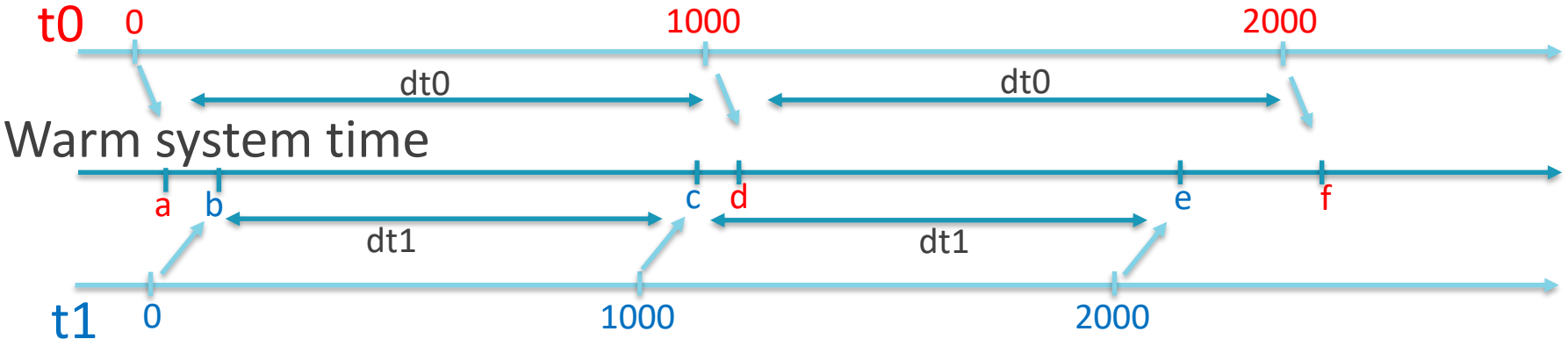
- Assuming it is hard to qualify dedicated circuitry for 30-years, avoid dedicated circuitry; (extreme) examples:
  - Fabric locations can be rotated to 30 spots within FPGA, fabric already qualified in ProtoDUNE for 1 year.
  - GPIO Tx can be rotated among 30 pins, GPIO already qualified in ProtoDUNE for 1 year.



- Hard to eliminate risk of unknown single points of failure for FPGA on 30-year timescale.

3. Clocking

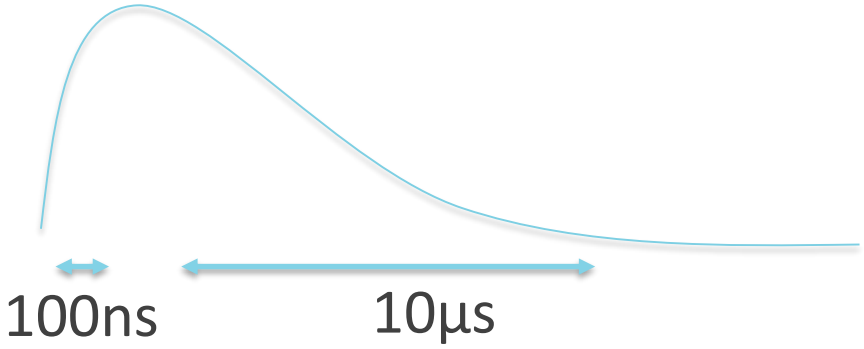
- If all else fails, can we run cold digitizers asynchronously?



- To synchronize data from two async sources (t0 and t1), do timestamp translation:
  - dt0 can be measured in units of warm system time, on average for more accuracy, and dt0 is used to get t0 timestamp step in warm system time.
  - dt0 = d – a ➔ t0 timestamp step = <dt0>/1000
- Same with t1: dt1 = c - b ➔ t1 timestamp step = <dt1>/1000
- In this way, the warm electronics can convert timestamps from multiple FPGA sources to a single warm system time.
- 1ns GPIO should be resolvable into Warm system time with <10ns resolution.
  - e.g. 8b10b K-char marker could be used every 1000 counts (5 characters for each 2ns)

4. Data Reduction

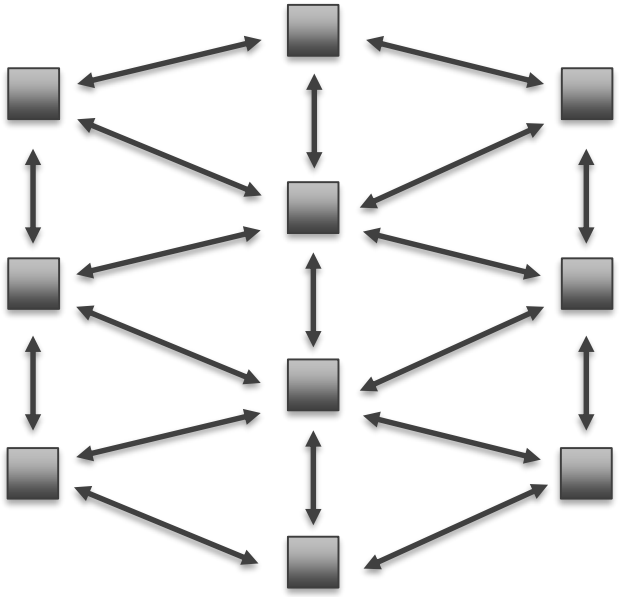
- Is 1 Gbps enough digital data transmission bandwidth?



- 1000 samples at 100MHz is likely enough for a sample window (10µs)
- 20b encoded sample ➔ 20Kb per sample window (can stack-up ~300 in BRAM)
- Sample rate?
  - 1KHz per tile ➔ 20Mbps per tile ➔ 50 tiles to get to 1 Gbps
  - ProtoDUNE saw single PE at <100KHz
  - Could neighbor FPGAs share threshold crossing for more individual higher threshold trigger?
  - Continuous readout would be 2 Gbps per channel (100Msps * 20b)

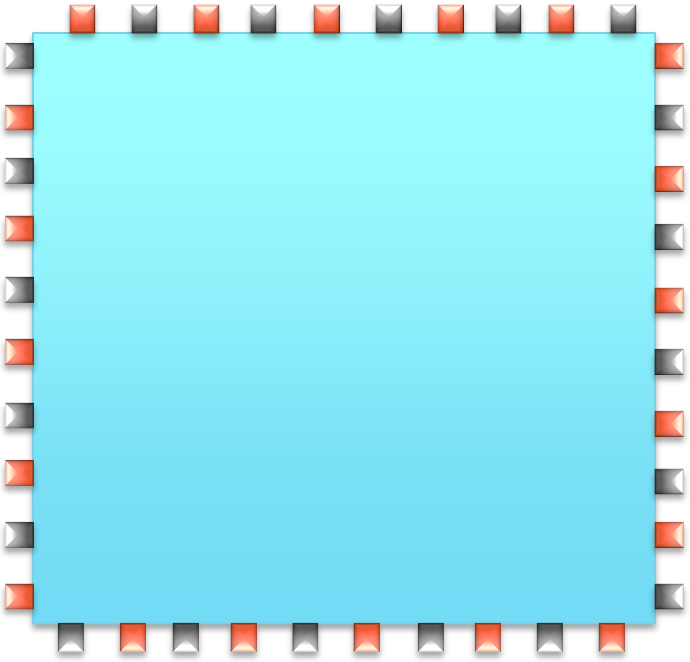
Cathode Neighbor Topology

- 10 FPGAs each handling 32 tiles, for example.
- Local group trigger
  - Share threshold crossing with neighbors
  - Allows for raising of global threshold
  - Use optical fiber to isolate from HV variation over large cathode distances



5. SiPM Ganging Topology

- Even/Odd xARAPUCA SiPM distribution to active ganging may be better than North/South half.



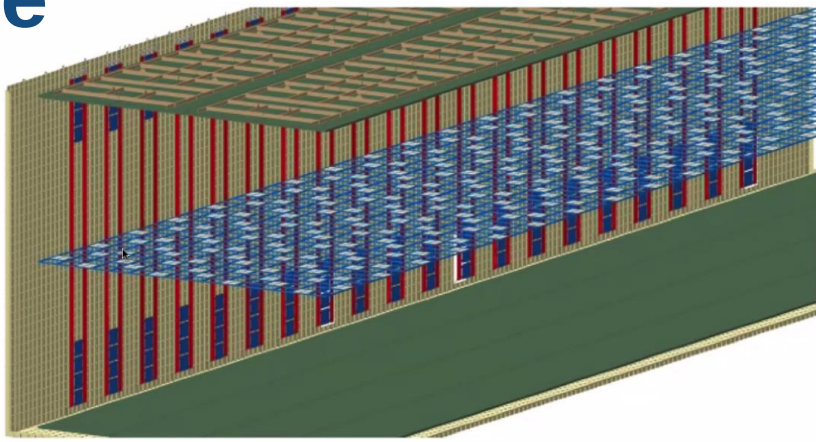
Conclusion

- Please reach out if interested in joining R&D effort
  - 2021: analog and digital prototypes
  - 2022: 30-year qualification and optimization
- Active engagement in interfaces for CERN Cold Box and ProtoDUNE2 is critical to leave open doors.
- Redundancy Concepts
  1. Detector signal handling
  2. Digital data transmission
  3. Clocking
  4. Data reduction
  5. SiPM ganging topology
  6. Any other ideas?

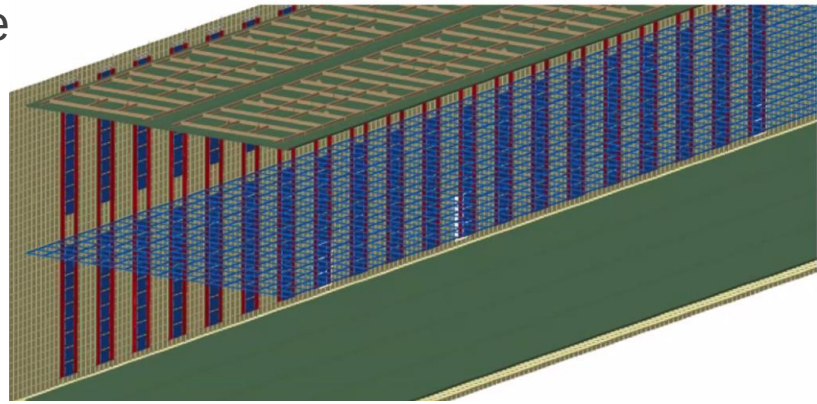
Backup

Establishing WBS Baseline

- **Baseline**:
  - 320 Cathode tiles & 320 Membrane tiles
  - Cold analog readout, warm digitizers, power-over-fiber
  - Requires **partial** 70% field-cage transparency for 40% membrane coverage

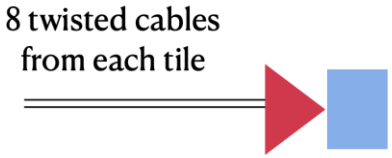


- **Fall-back Option**:
  - 720 Membrane-only tiles
  - Cold analog readout, warm digitizers, copper power supplies
  - Requires **full** 70% field-cage transparency



Active 2021 R&D Program

- Targeting two prototypes for end-of-year CERN Cold Box Test
  - analog readout prototype



  - digital readout prototype