FPGA Trigger for SpinQuest experiment

on behalf of the SpinQuest collaboration

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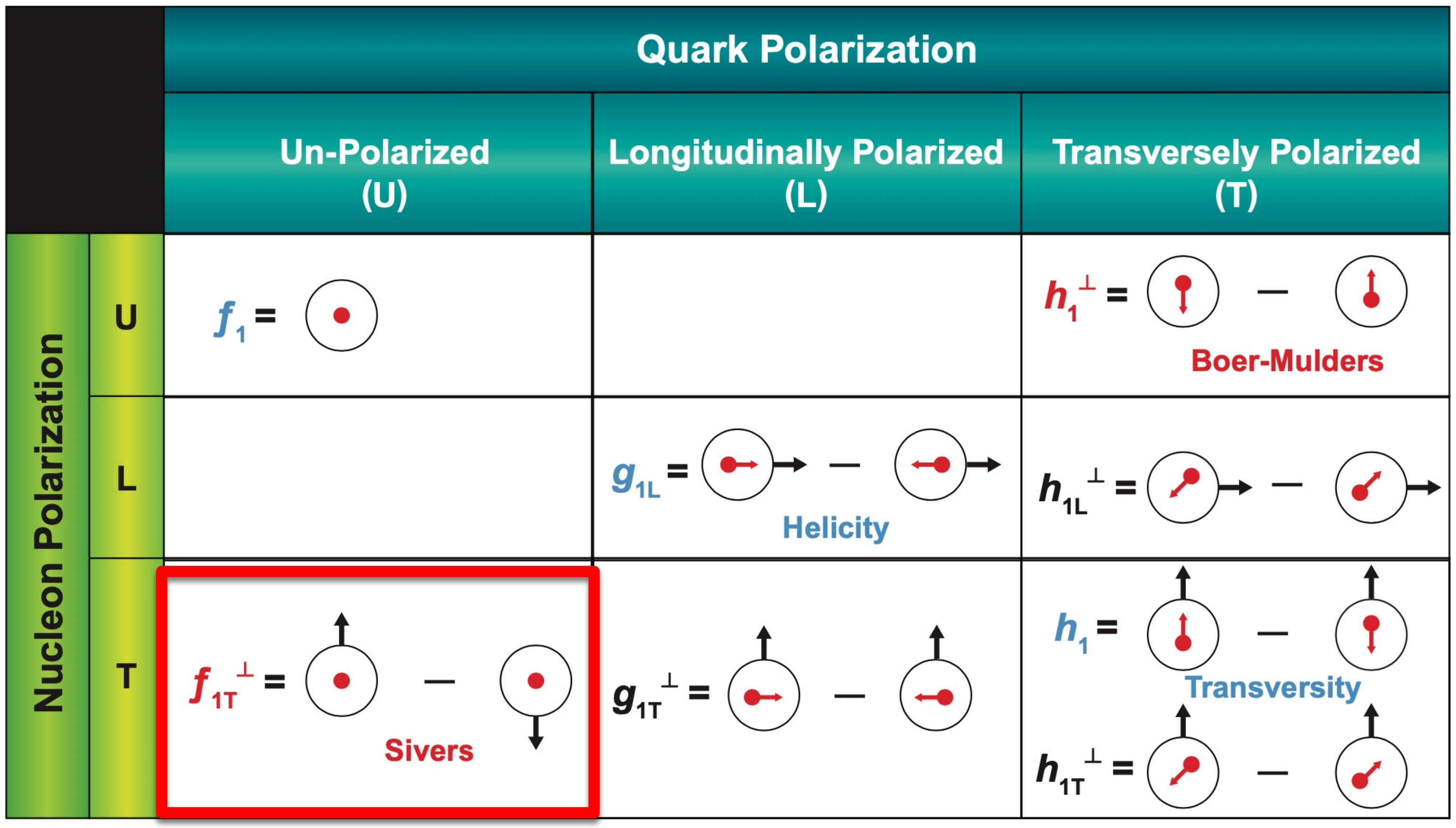
SpinQuest and Sivers Function

Leading Twist TMDs

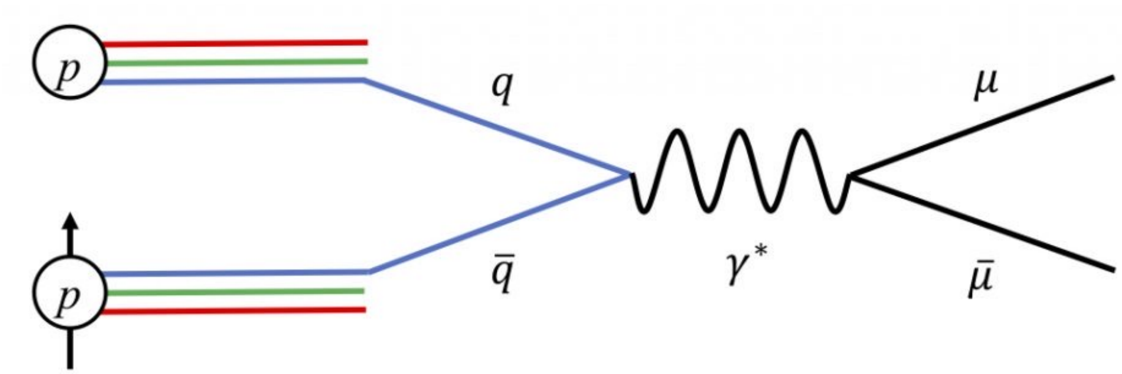
Nucleon Spin   Quark Spin



[taken from: SEAQUEST DocDB 1720-v3]

- Valence u- and d- quark Sivers functions are similar in size but opposite in sign [SIDIS experiments by HERMES, COMPASS, JLAB].
- Sea-quark Sivers function   => SpinQuest!

SpinQuest Experiment



Drell Yan Cross section [Boglione-HUGS2012-2] :

$$\sigma_{DY} = \sum_q f_q(x, k_\perp) \times f_{\bar{q}p^\uparrow}(x, k_\perp) \times \sigma^{q\bar{q}\to\mu\bar{\mu}}$$

, where the distribution of unpolarized quarks in the polarized proton: [PHYS REV D ***70,*** 117504 (2004)]

$$f_{\bar{q}p^\uparrow}(x, k_\perp) = f_1^{\bar{q}}(x, k_\perp) - f_{1T}^{\perp,\bar{q}}(x, k_\perp) \frac{(\hat{\boldsymbol{P}} \times \boldsymbol{k}_\perp) \cdot \boldsymbol{S}}{M}$$

Unpolarized TMD

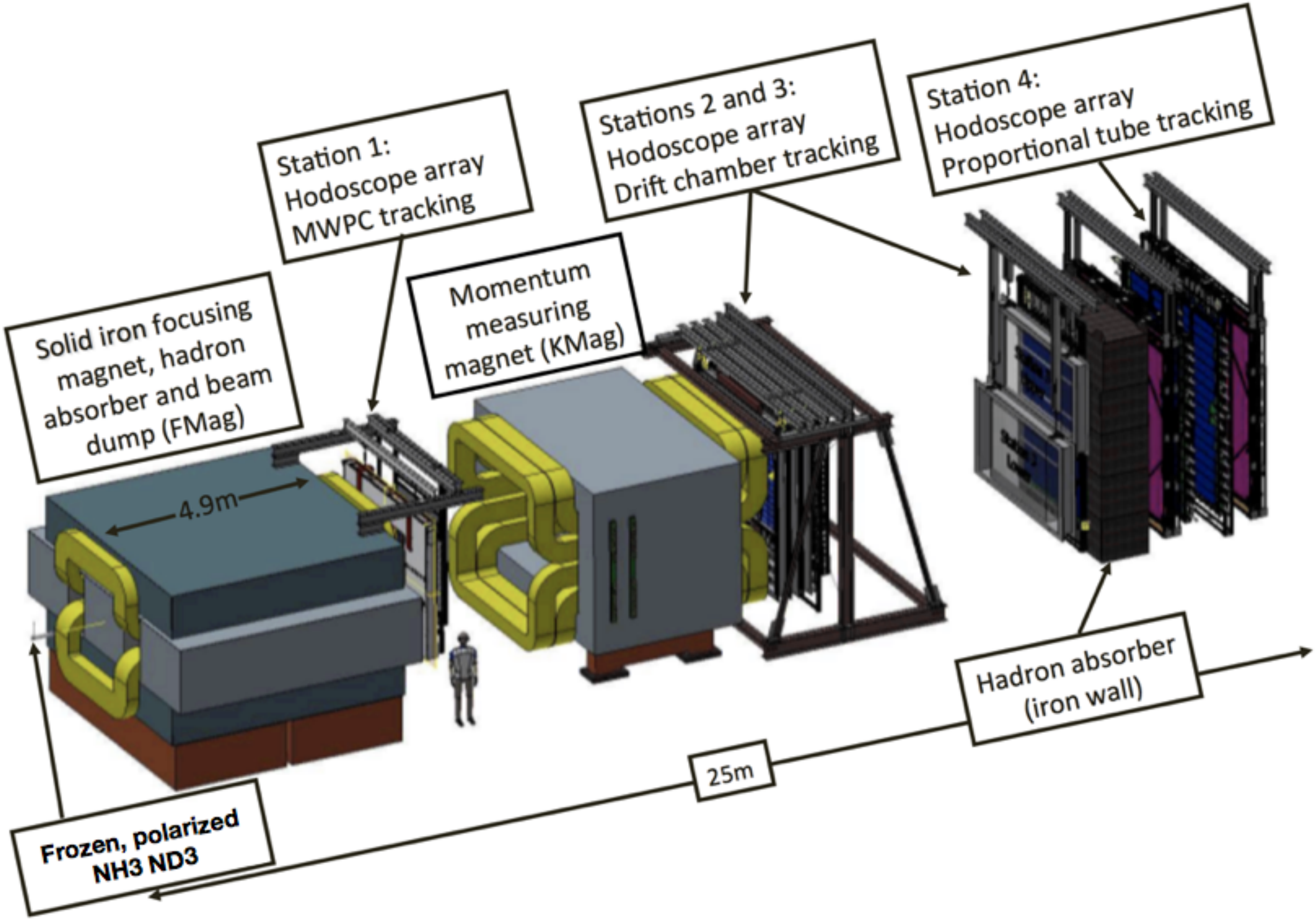
Sivers TMD

Spin of the proton

Accessing Sea Quark Sivers function from Asymmetry:

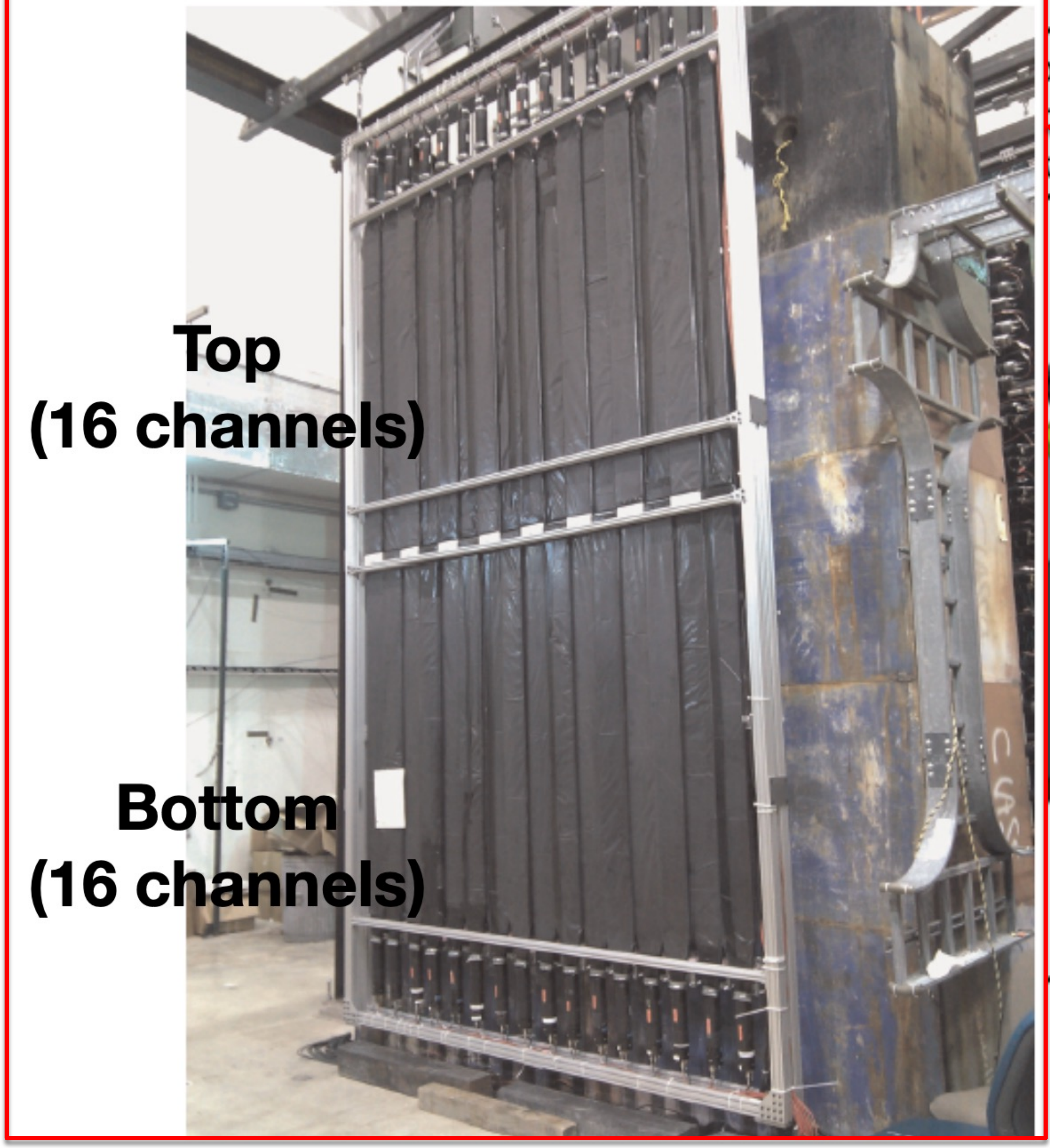
$$A_N = \frac{\sigma_\uparrow^{DY} - \sigma_\downarrow^{DY}}{\sigma_\uparrow^{DY} + \sigma_\downarrow^{DY}} \propto \frac{N_\uparrow^{DY} - N_\downarrow^{DY}}{N_\uparrow^{DY} + N_\downarrow^{DY}} \propto \frac{\boldsymbol{f_{1T}^{\perp,\bar{q}}(x)}}{f_1^{\bar{q}}(x)}$$

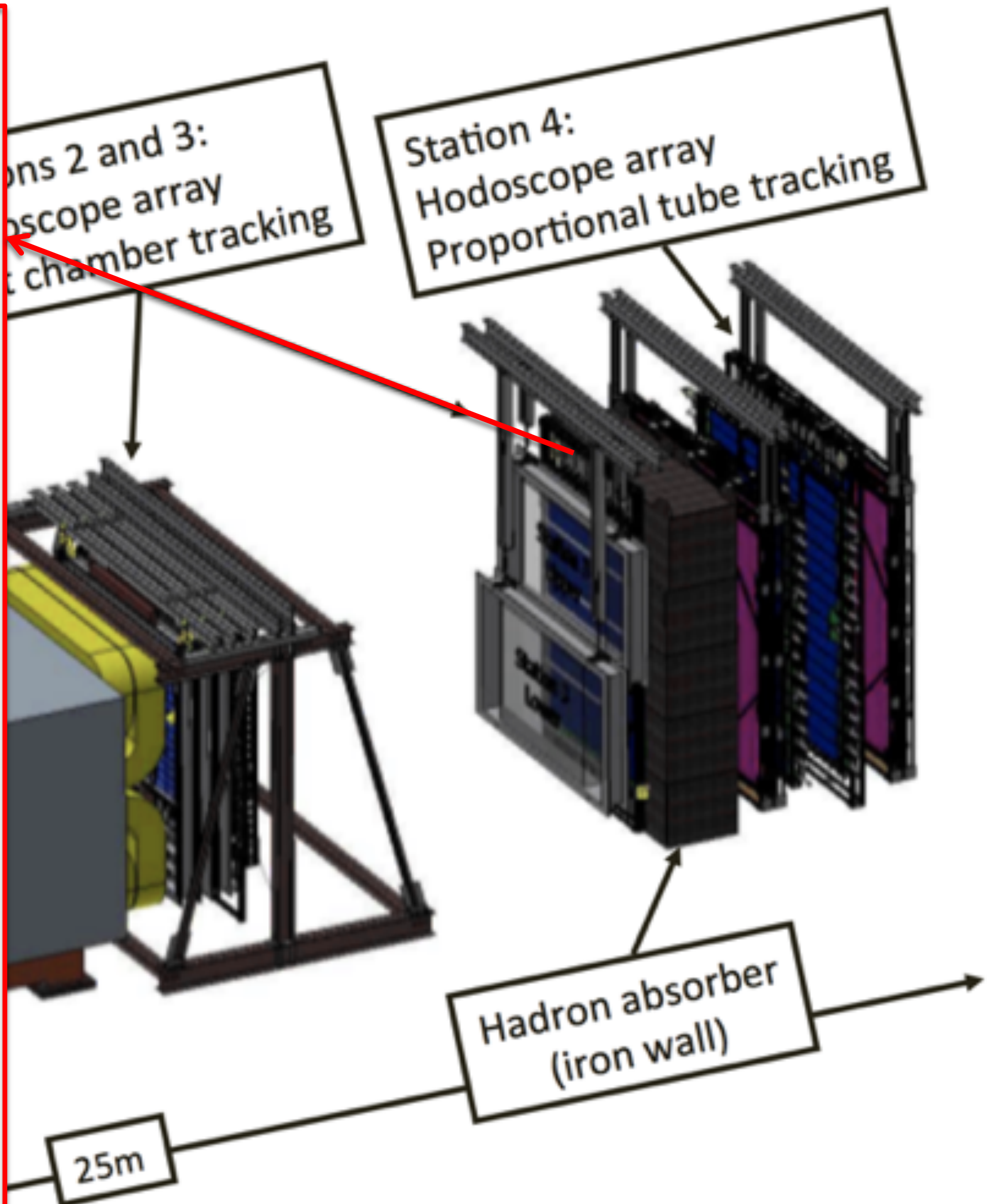
Spectrometer Overview



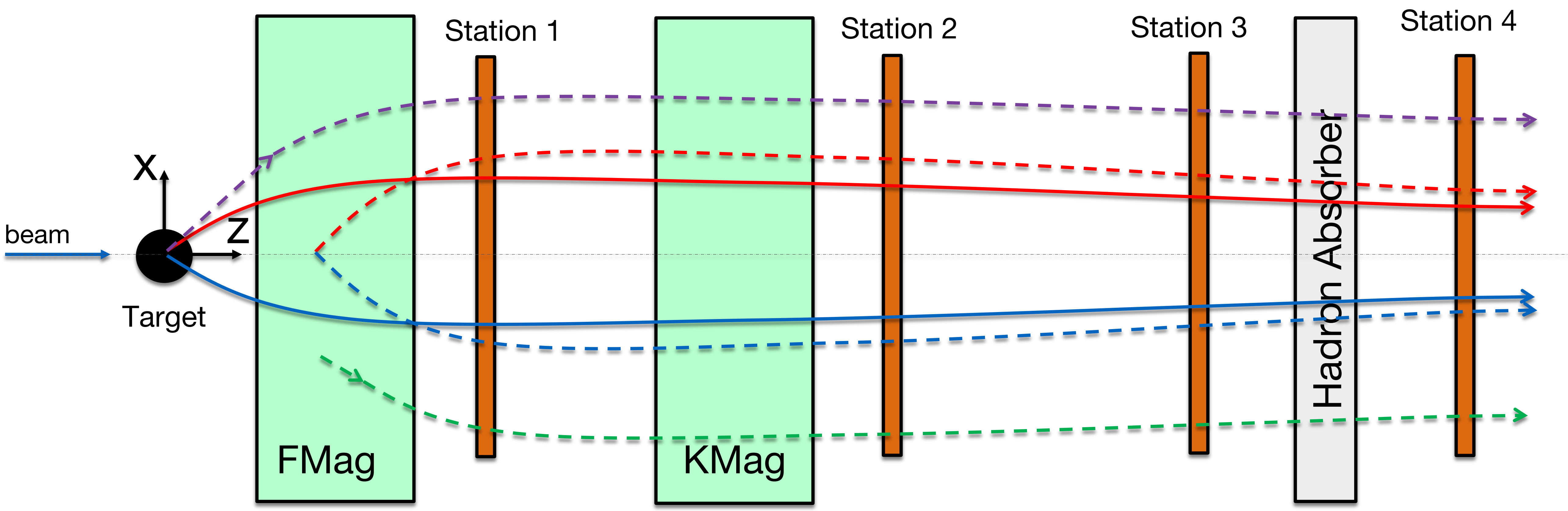
Spectrometer Overview

Station 3 Hodoscope:





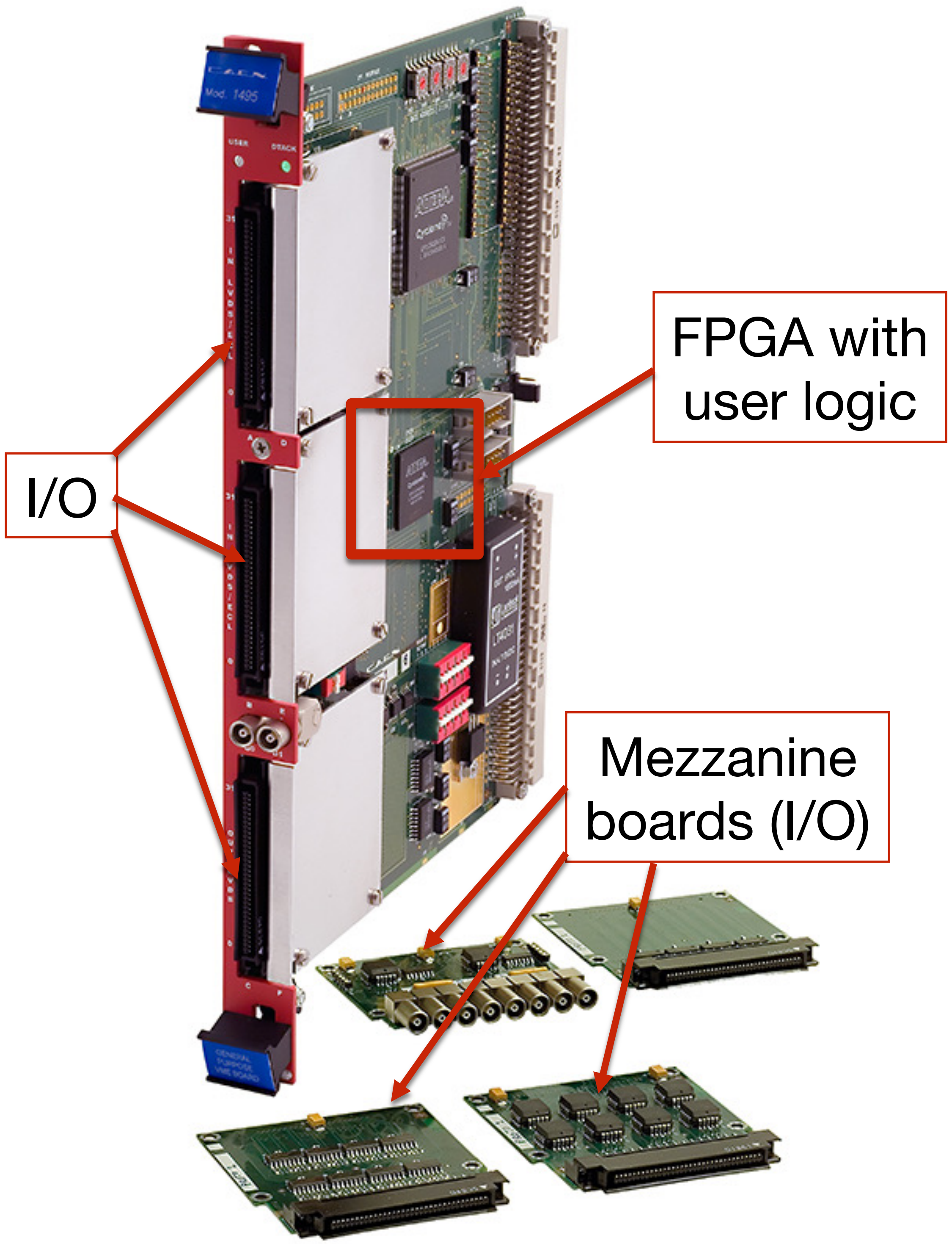
SpinQuest: Main Source of Background



1. Solid red and blue are dimuon tracks (positive and negative) from the target.
2. Dashed red and blue are dimuon tracks produced in the beam dump.
3. Dashed purple is a track of a single muon produced at target.
4. Dashed green is a track of a single muon produced at the bea dump.

The largest background and challenge for the FPGA trigger!

FGPA Trigger Overview: Logic



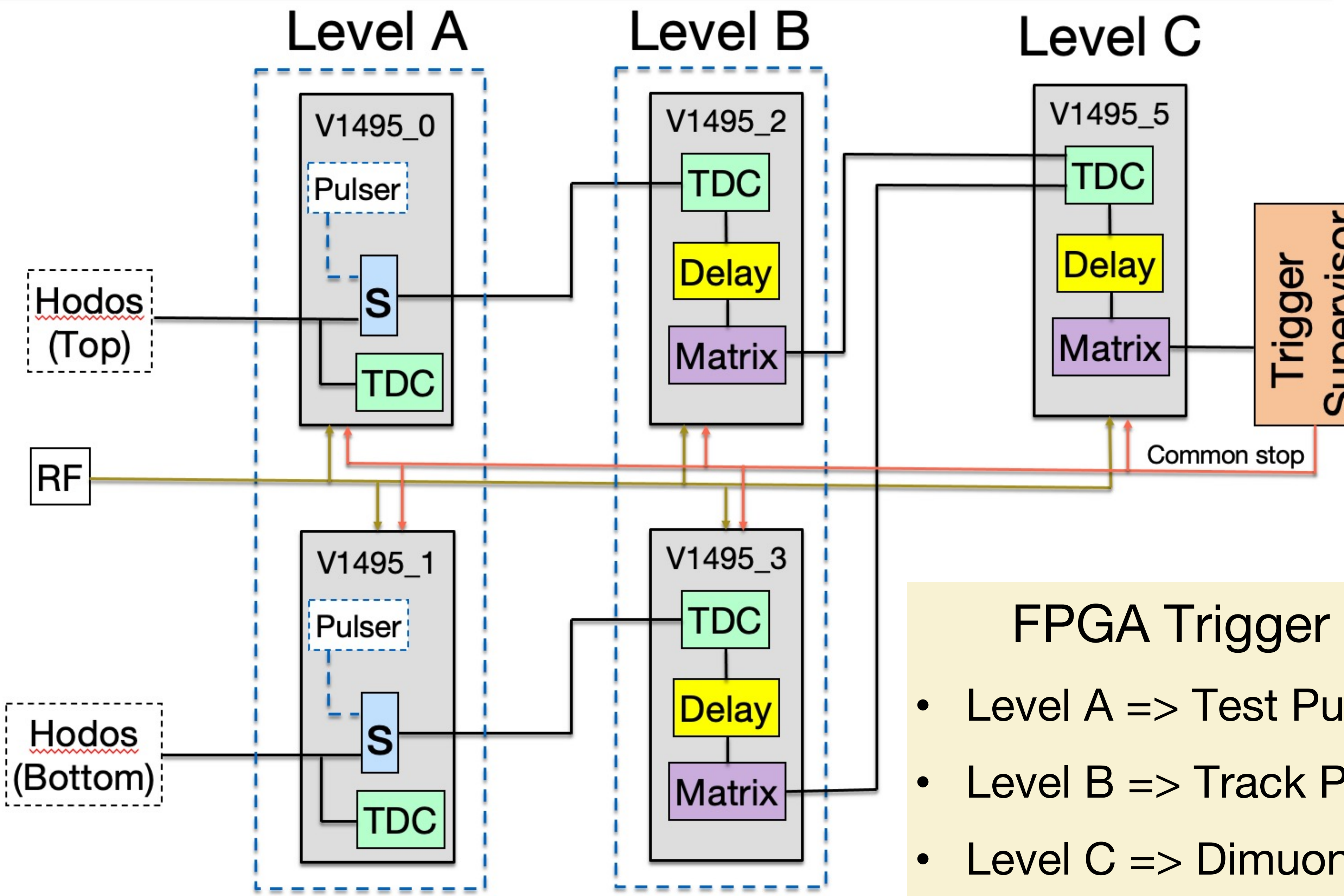
[https://www.caen.it/products/v1495/]

- CAEN v1495 User customizable FPGA Unit.
- LVDS/ECL/PECL inputs (differential).
- 64 inputs, expandable to 162 (with 32 outputs).
- 32 outputs, expandable to 130 (with 64 inputs).
- 405 MHz maximum frequency supported by clock tree for registered logic.

SpinQuest Requirements:

- RF clock of 53.1 MHz.
- 65 inputs (16 scintillators x 4 stations + RF) for each top/bottom boards.
- Total 5 boards are used by FPGA trigger system

FGPA Trigger Overview: Logic



TS distributes triggers to all DAQ components.

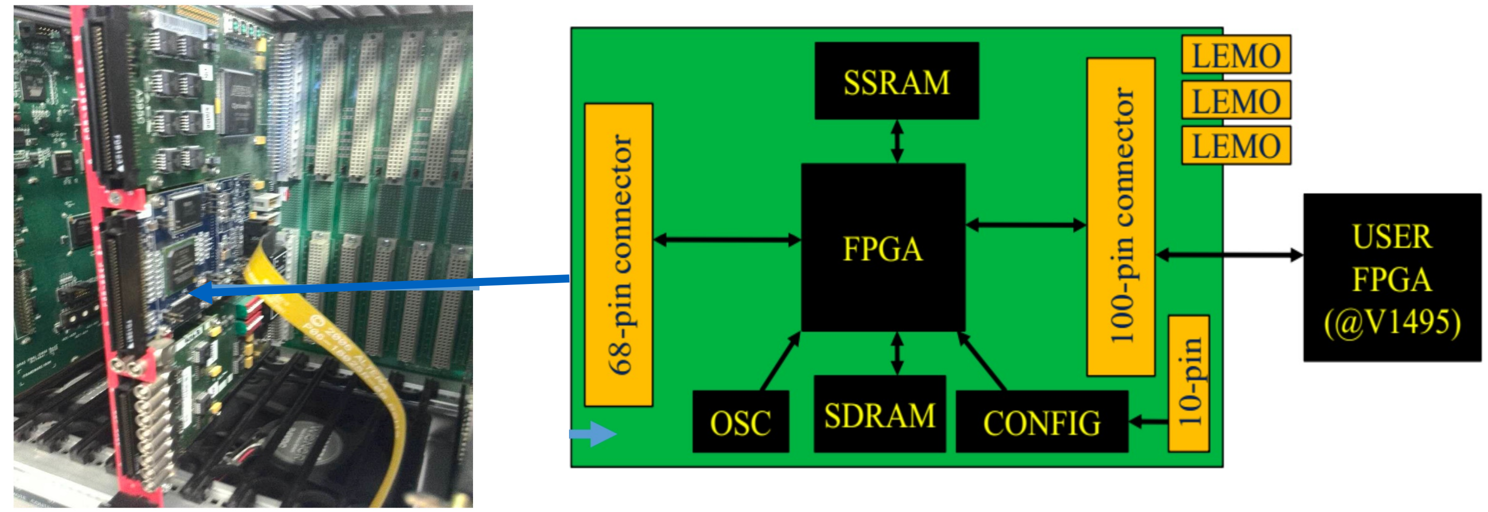
FPGA Trigger Firmware feature:

- Level A => Test Pulser Logic for Debugging.
- Level B => Track Pattern Recognition.
- Level C => Dimuon Event Reconstruction.
- All designs have TDC functionality for ch-by-ch delay adjustment.

FPGA Trigger: Progress ...

1. Buffered TDC data readout with a custom Daughter Card (DC):

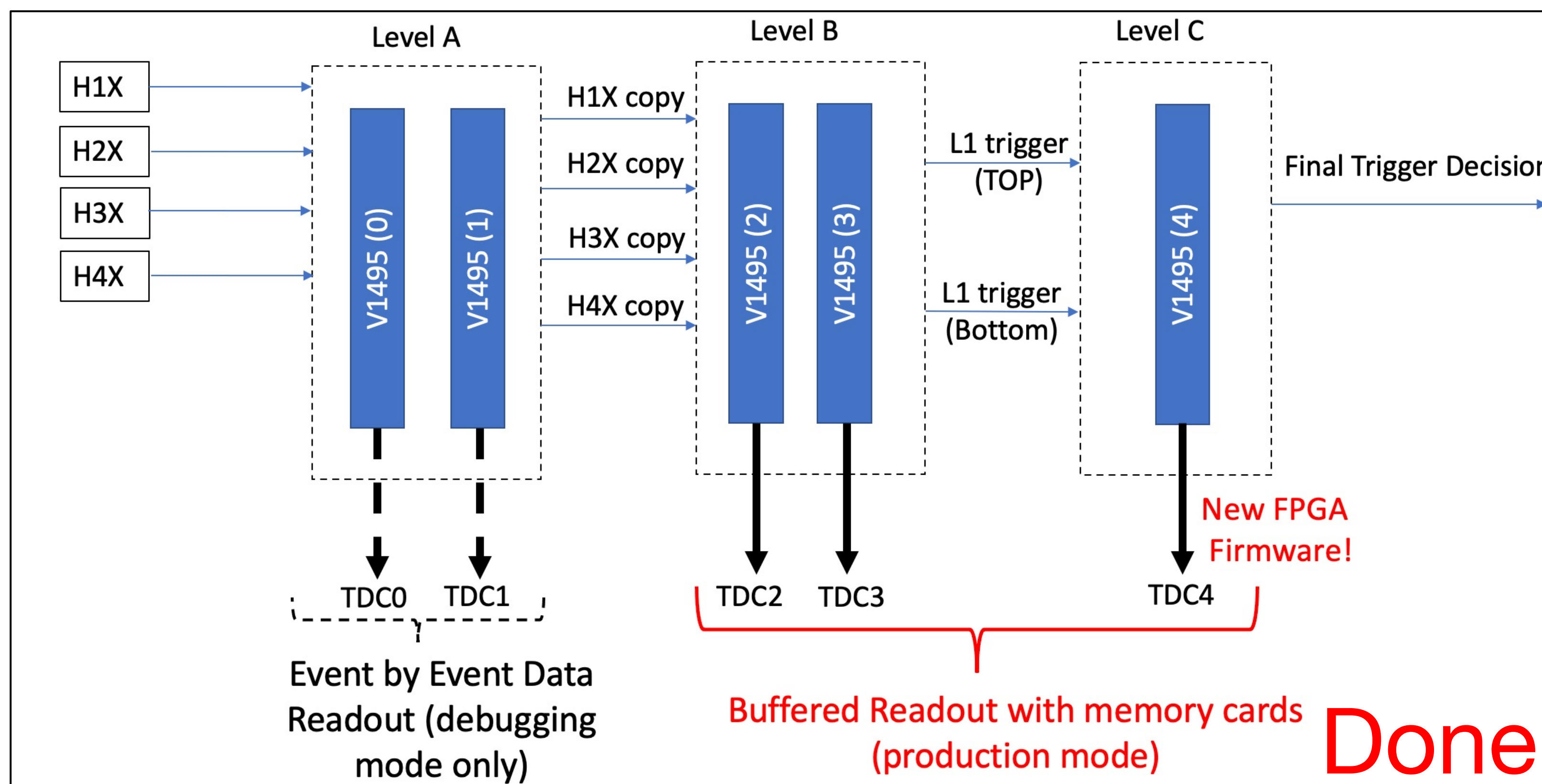
   [credit to Xinkun Chu]



Data generate @1495 FPGA -> 256 buffer -> DC SDRAM-> V1495 buffer ->VME

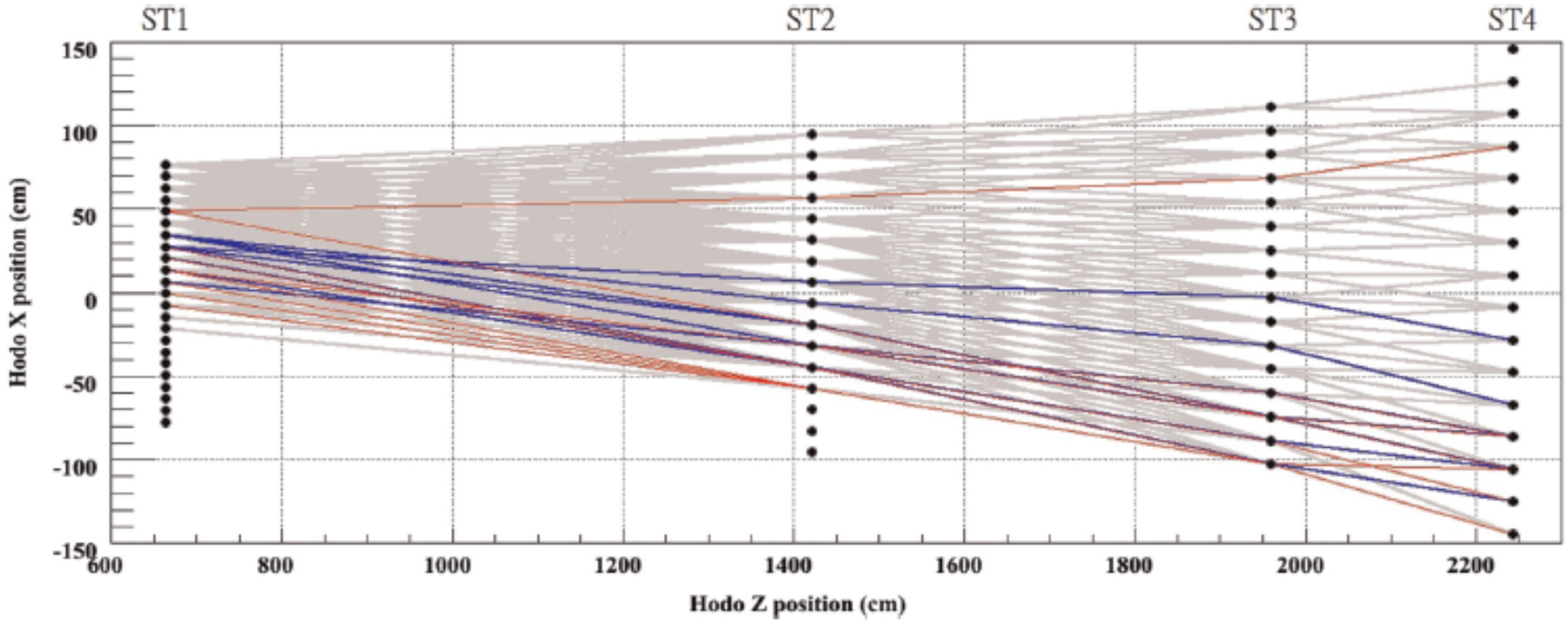
Main Features of DC:

- FPGA used as interface and memory controller.
- 32-MB SDRAM for buffering.
- Buffer size 2048 data words.
- Stores 6 physical events per spill.



FPGA Trigger: Progress …

2. Level B FPGA Design Upgrade with Road Set ID readout:



Example of the Visualized hit patterns (road sets) of positive muons from E906/SeaQuest MC simulation study. [taken from M. Kim]

- Current V1495 FPGA design reads out TDC data only (up to 95 TDC channels + headers).
- The plan is to add Road Set IDs (16 – bit data words) to VME data stream:

$0xH_4H_3H_2H_1$

  - Bits 0-3: bar fired at hodoscope station 1;
  - Bits 4-7: bar fired at hodoscope station 2;
  - Bits 8-11: bar fired at hodoscope station 3;
  - Bits 12-15: bar fired at hodoscope station 4;

Under Development!

FPGA Trigger Strategy

- Define patterns of hodoscope hist (road sets) for DY events with simulation [credit to M. Kim and K. Nakano].
- Test Trigger Efficiency for obtained road set with Level A trigger pulser.
- Use experimental data to remove noisy, “hot” roads.
- Implement lookup table of roads as a trigger matrix on v1495 FPGAs.
- Ready for data taking ☺

Thank you!