Final Design Review of the DUNE Cold Electronics ASICs

Scope of the review

- DUNE cold electronics PDR in Feb. 2020
  - Two options for the ASICs
    - A single chip CRYO
    - A 3-chip solution
      - LArAsic, ColdADC, COLDATA
      - One front-end mother board contains 8 LArAsic, 8 ColdADC and 2 COLDDATA
- This FDR is to review the ASICs of the 3-chip solution
  - To be used in protoDUNEII
- The rest of the electronic system (front-end boards and warm electronics) will be review during the Fall

Review Committee

- Tim Andeen,
- Alessandro Caratelli
- Philippe Farthouat (Chair)
- Marek Idzik
- ~~Jan Kaplon~~
- Pedro Leitao
- Mitch Newcomer
- Paul Rubinov

Charge

- Has the TPC Electronics consortium responded appropriately to recommendations from past reviews?
- Are the full specifications of the ASIC designs and complete documentations for ASIC users available in EDMS? Is the standalone testing of ASICs complete and are results available in EDMS?
- Do the standalone tests of the new generation of ASICs indicate that the design goals have been achieved? Do these design goals meet the detector requirements? Have all issues observed in previous versions of the ASICs been addressed? Do the performance measurements obtained from test stands meet the expected performance? Does the response of the ASICs match the expectations obtained from simulation? Specifically:
- What is the outcome of system tests? What are the plans and timeline for future tests?
- Are there any issues with the design of the cold electronics system that will complicate the procurement strategy and manufacturing plans for the ASICs and the FEMBs?
- Is the QA/QC plan complete and documented? Have sufficient resources been allocated to successfully execute the QA/QC plan?
- Is the probability that tests not yet performed or not yet fully understood may require a further design iteration negligible and should the TPC electronics consortium proceed with the engineering run for the ASICs? Is the TPC Electronics consortium ready for the engineering run submission at the beginning of August 2021?
- Are the Parts Breakdown structure, interfaces with other detector components, cost estimates and schedule fully documented?

- Main question to be answered: is the team ready to submit 2 engineering runs (one for LArAsic and one for ColdADC/COLDDATA) within a few weeks (days)

Documentation & Agenda

- Documentation available since a week
  - Details of the tests done and of the modifications made
- Two half-day sessions
  - Today with presentations
  - Tomorrow only for questions/answers
    - Depending on how it goes today, tomorrow session could start later

Report

- Report to be made available on Aug. 2nd
  - To give (or not) green light for the ERs
- I will write a draft based on my notes and on the comments you are asked to send me before Saturday night
- We'll see whether we need a special meeting to finalise the report in the course of next week

Thanks for your help