DUNE TPC Electronics ASICs (and FEMBs) Final Design Review - Overview

Marco Verzocchi

Fermilab

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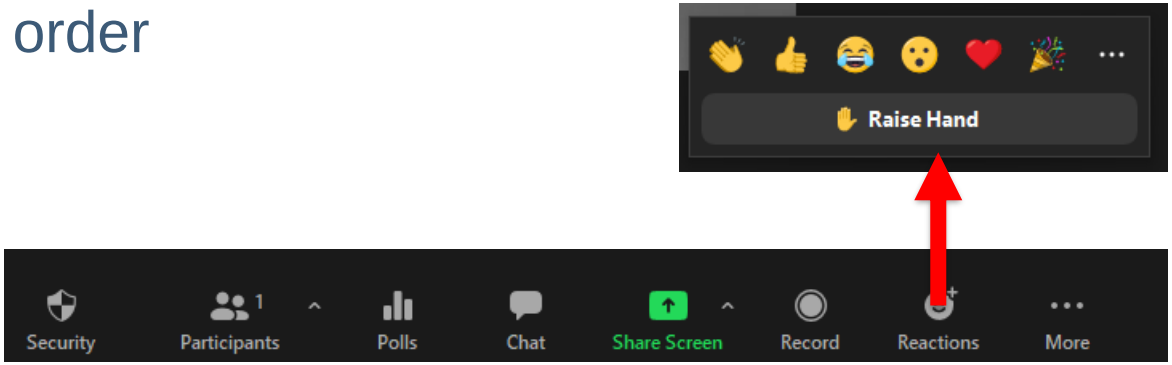
Thank you

- First of all, I would like to thank all the reviewers (old and new) for their time in reading the material we've provided you and attending this session (and tomorrow's)
- The review we had in February 2020 was extremely useful and gave us very good feedback on where we were with the design, informed some of the changes we've made to our ASICs
- This is an extremely important service to the overall HEP community, thanks again

Meeting ground rules

- Please mute when you are not speaking
- We have allocated a lot of discussion time at the end of each presentation, unless absolutely necessary please do not interrupt the speakers. We will take question at the ends of the talks
- If you need to intervene or ask questions, please use the “raise hand” feature of Zoom and the moderators will try to recognize people in order



Content

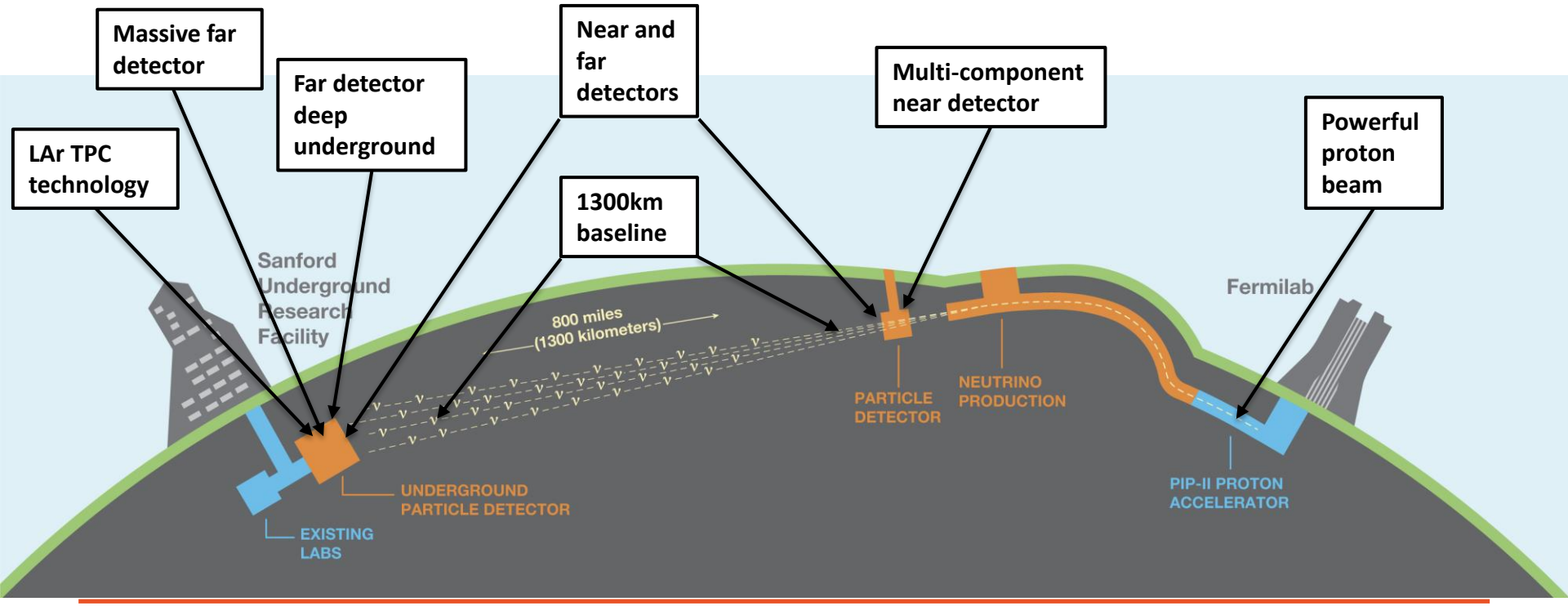
- DUNE overview
  - Role of TPC electronics and corresponding ASICs
- Scope and organization of the review
- Requirements
- Recommendations from previous review
- What is left to do ?
- Vertical drift detector
- Production and QC plans

Introduction to DUNE

- The DUNE experiment is being built with 3 main physics goals:
  - Precise measurements of neutrino oscillation parameters including study of CP violation in the neutrino system (i.e. differences in oscillation parameters between neutrinos and antineutrinos)
    - Possible source for matter – antimatter asymmetry in the universe
  - Search for proton decay
    - Physics beyond the standard model / grand unification
  - Observation of neutrinos from supernova explosion
    - Get a time-lapse movie of the stellar collapse
- Requirements for experiments of this kind
  - Large sensitive mass, long baseline and intense neutrino source, underground
  - Two technologies: water Cerenkov (HyperK, Japan), liquid argon TPC (DUNE)

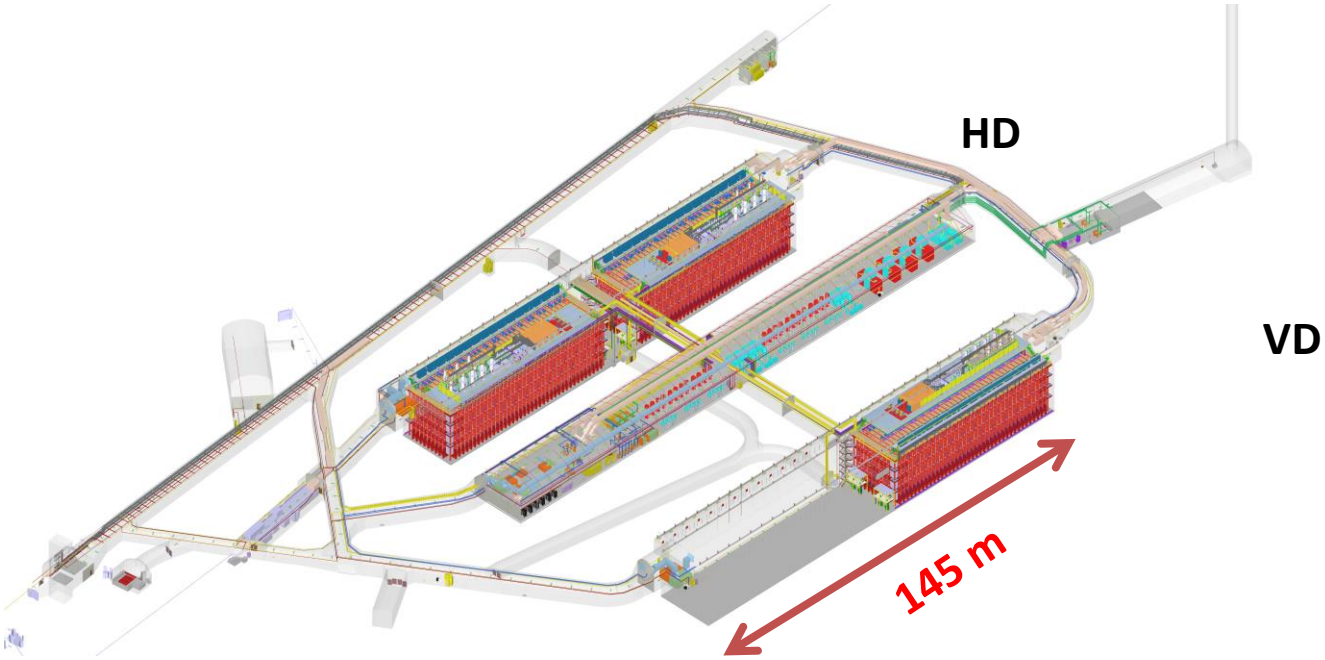
Introduction to DUNE

- LBNF is the facility (beam from Fermilab to South Dakota, near and far site caverns, infrastructure, cryostats)
- DUNE is the experiment (liquid argon time projection chamber)



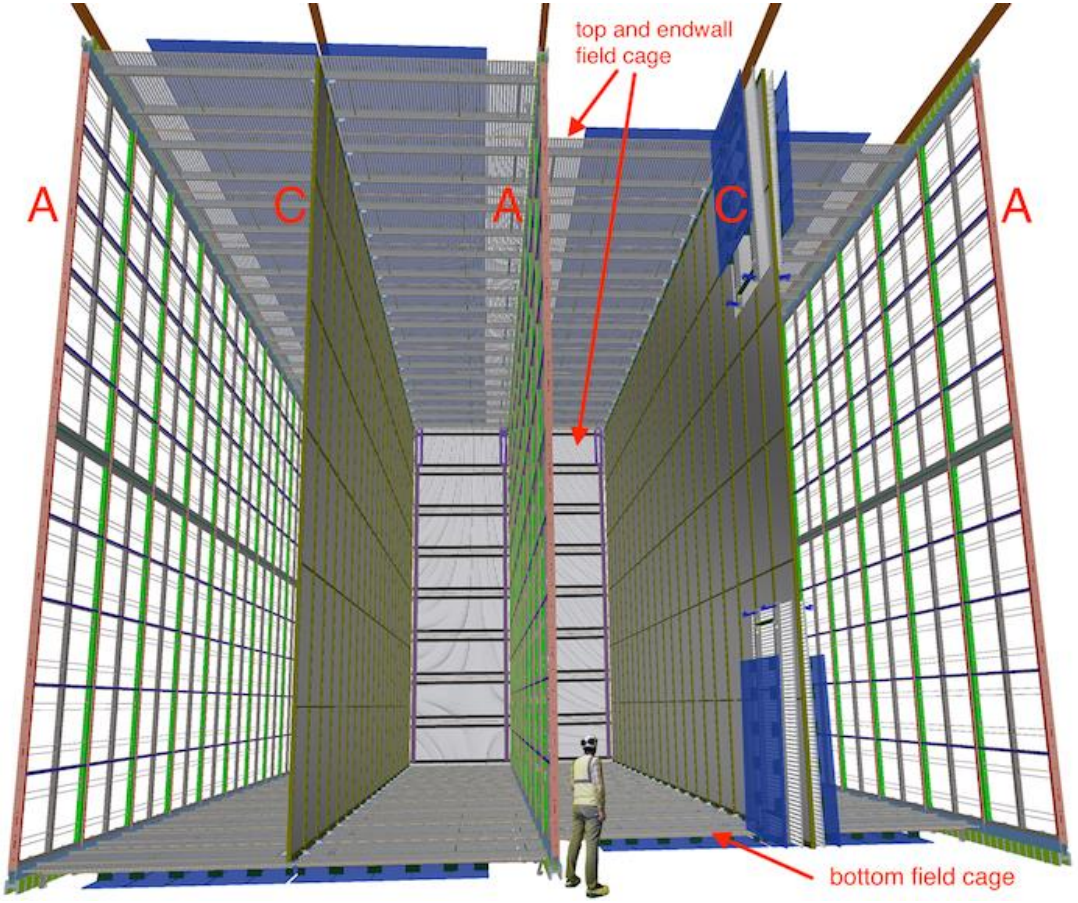
Introduction to DUNE

- Four separate 17 kt (> 10 kt fiducial) LAr TPCs
- 4 identically sized cryostats: current plan has horizontal drift (HD) detector (previously known as single phase – SP) in cryostat #1 and vertical drift (VD) detector (merging of SP and dual phase designs) in cryostat #2



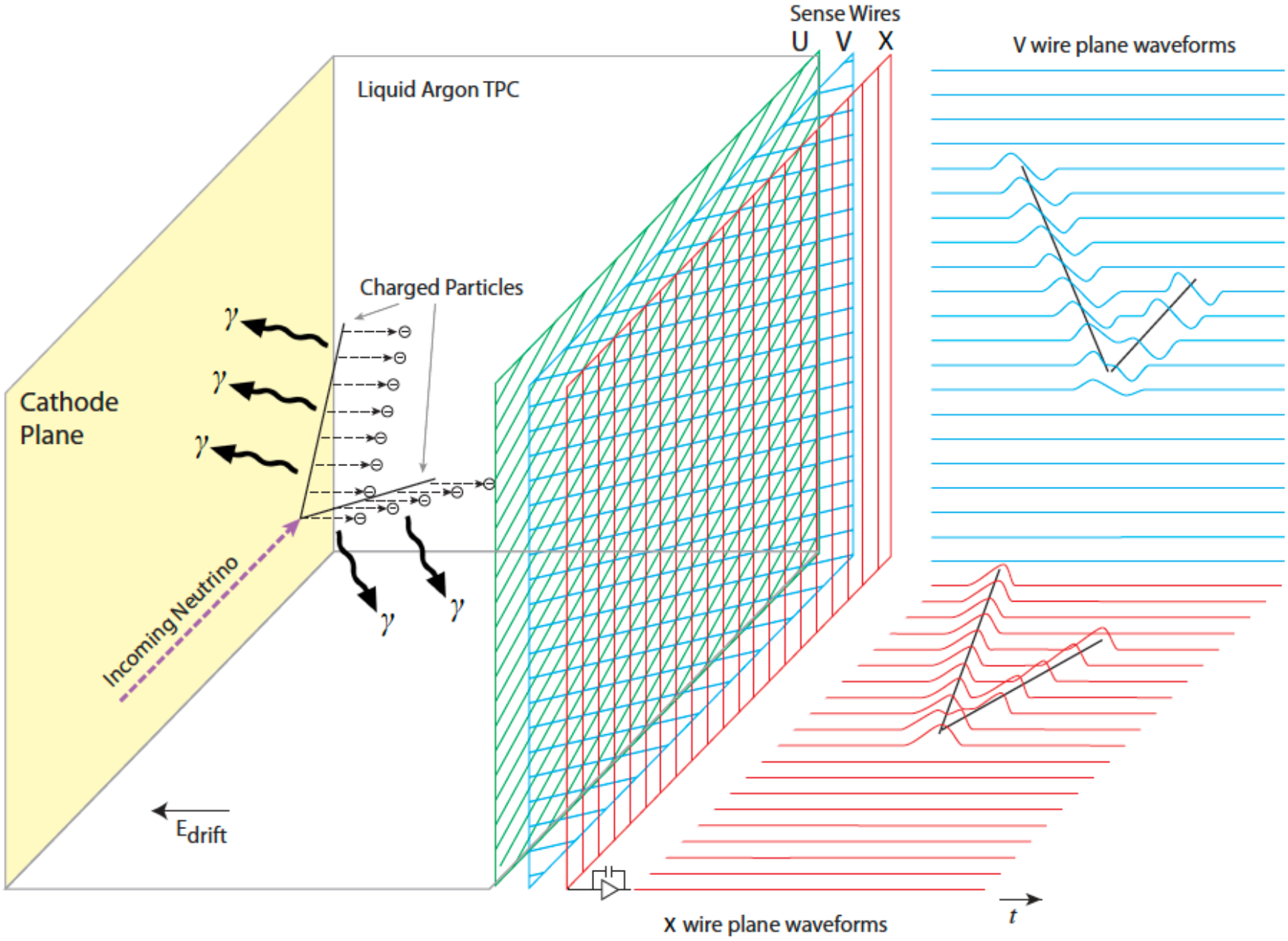
Horizontal Drift Detector

- Horizontal drift detector:
- 4 drift volumes of 3.5m
- Read out by a total of 150 anode plane assemblies (APAs), each with 2560 wires
- 128 channels per front-end motherboard (FEMB), 20 per APA
- Total of 384k readout channels, 3000 FEMB total



Signal formation

- Wires organized in multiple readout planes (U, V, X) to allow for 3d reconstruction of ionization from tracks, unipolar signal (negative) on collection wires (X), bipolar signal (first negative then positive) on induction wires (U,V) as electron cloud travels past the wires
- Signal duration o(μs), narrower for collection plane
- 20-30k e^- collected on the X wires for ionization from MIP near the cathode (3.5m distance, assume drift field 500 V/cm, 6 ms electron lifetime in Ar)
  - Limited by immediate recombination (30%), losses caused by recombination along the drift distance (depends on drift field and argon purity)
- No amplification in liquid


Sense Wires
U V X
Liquid Argon TPC
V wire plane waveforms
Charged Particles
Cathode Plane
γ
γ
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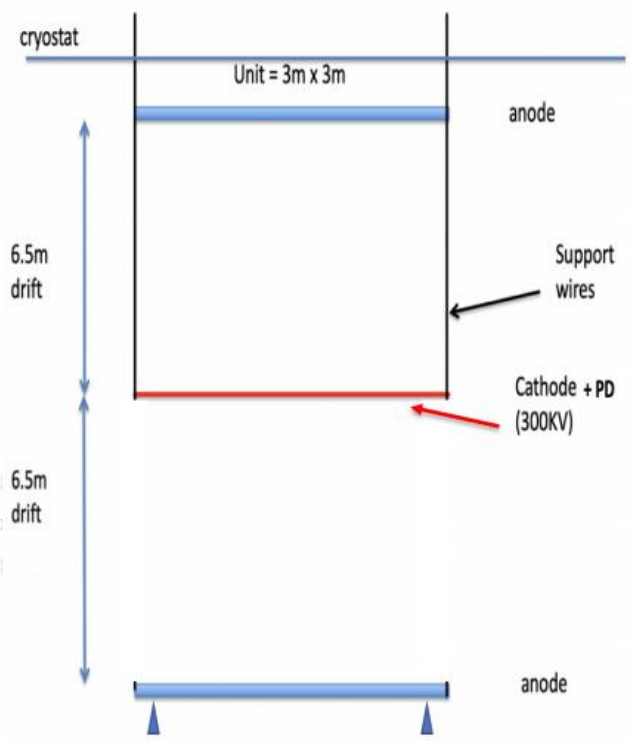
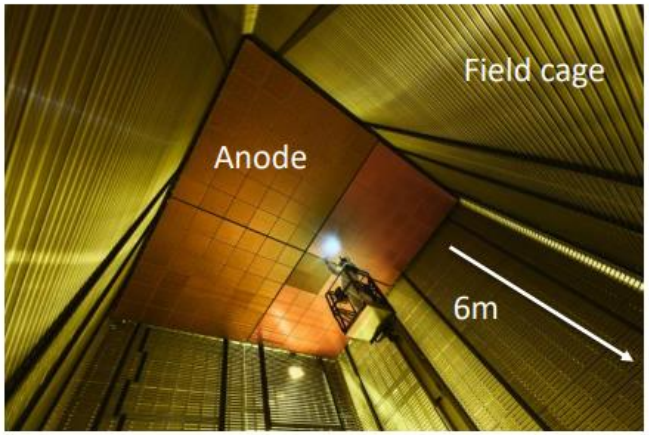
Incoming Neutrino
E drift
X wire plane waveforms
t

Vertical Drift Detector (i)



NP02 image



cathode

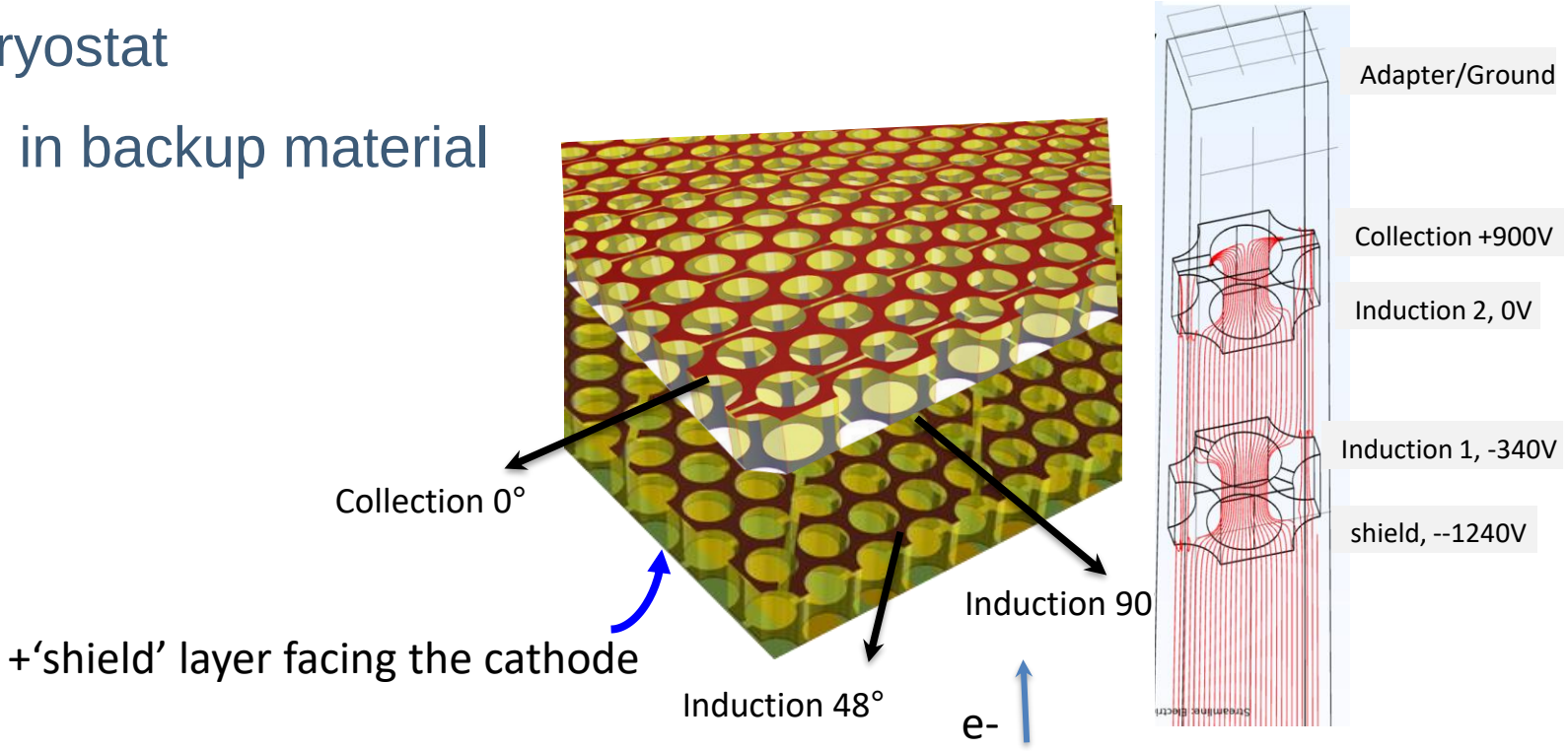
- Vertical drift detector:
  - Builds on experience gained with Dual Phase detector and long e^- lifetime achieved in ProtoDUNE

Vertical Drift Detector (ii)

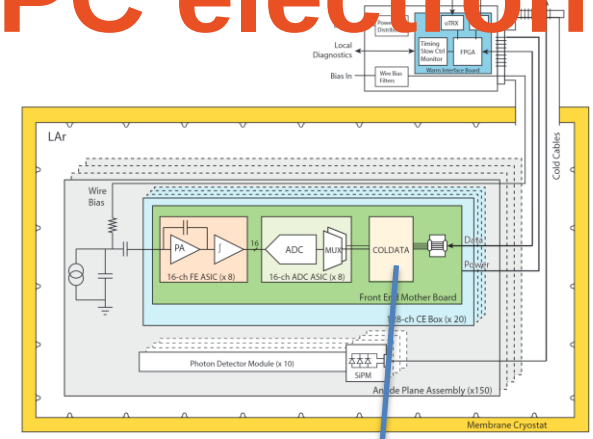
- Vertical drift detector:
  - Builds on experience gained with Dual Phase detector and long e^- lifetime achieved in ProtoDUNE
  - Drift over distances of 6 m (3.5 m in horizontal drift detector)
  - Use strips on perforated printed circuit boards (inspired by LEM of dual phase detector) for charge collection, can have multiple views like on the APAs
  - With current design (2 perforated PCBs plus ground plane that also serves as adapter card for the electronics) and the current dimensions of the charge readout planes (CRPs) we have a capacitive load on the front-end amplifiers similar to that for the APA wires (range 130-250 pF, depends on strip orientation and length)
  - Not only the capacitive loads are similar, signals' shapes are also very similar, can use the same electronics developed for the APA readout

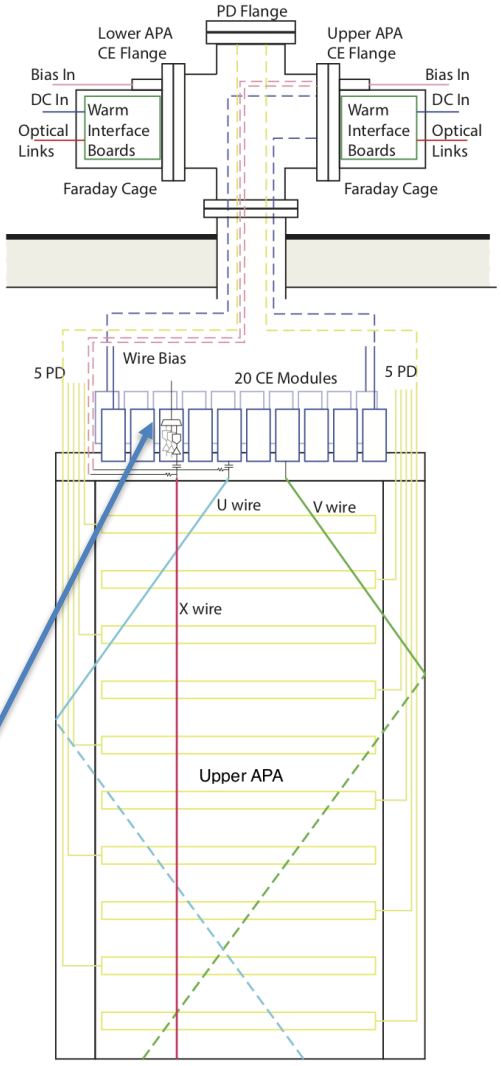
CRP Design

- The design of the CRPs has evolved, current baseline foresees shielding plane, two induction views and one collection view: (0^o,90^o, 48^o) and (90^o, 30^o) orientations being considered
- Use same electronics as for APAs for the CRPs at the bottom of the cryostat
- More in backup material



The TPC electronics





128 readout channels per FEMB (front-end amplifier, ADC, data serializer) implemented as
8 LArASIC + 8 ColdADC +2 COLDATA chips

20 FEMBs per APA

Scope of the Review (i)

- The main issue today is whether the TPC electronics consortium is ready for the engineering run submission at the beginning of August 2021 (question 7 of the charge)

- How did we get here ? What drives this question ?
- Past review was in February 2020 at CERN
- At that time we had
  - First complete DUNE version of the ASICs (LArASIC p3, ColdADC p1, COLDATA p2, CRYO) gone through standalone tests
  - We were preparing for system tests, we were working on design changes for the next round of prototypes

Progress since February 2020

- Since then
  - LArASIC: 2.x prototype submissions (p4, p5 and p5a)
    - We believe that the p5 chip meets all the DUNE requirements. We also have a version with stronger ESD protection. We propose to have both version of the chip on the reticle for the engineering run
  - ColdADC: 1 prototype submission (p2)
    - We believe that the p2 chip meets all the DUNE requirements and we want to put this version on the reticle for the engineering run
  - COLDATA: 1 prototype submission (p3)
    - The p3 chip can be used for building FEMBs that meet all the DUNE requirements, but we prefer to fix two minor features to make the operation of LArASIC more reliable and to provide additional functionality on the FEMB. We propose to put the new version of the chip (p4) on the same reticle as ColdADC and proceed with the engineering run
  - While the development of CRYO continues, we are no longer considering it for the first two DUNE far detector modules

Future Timeline

- We are planning on a second run of ProtoDUNE-HD at CERN in the 2nd half of 2022
  - Need 80 fully populated FEMBs (plus spares/yield) early in 2022
  - Very tight timeline
    - ASIC production: August-October (we have a timeline for LArASIC, not yet for ColdADC/COLDATA)
    - ASIC packaging: November-December
    - ASIC testing starting in January
    - 2-3 weeks later start populating FEMBs, then perform quality control
    - 2-3 weeks later install on APAs at CERN (beginning of March)
  - Large uncertainties in the schedule due to issues with ASIC industry (not just the foundries, there are issues also with packaging)
- This is the reason for wanting to start the engineering run as soon as possible (beginning of August)

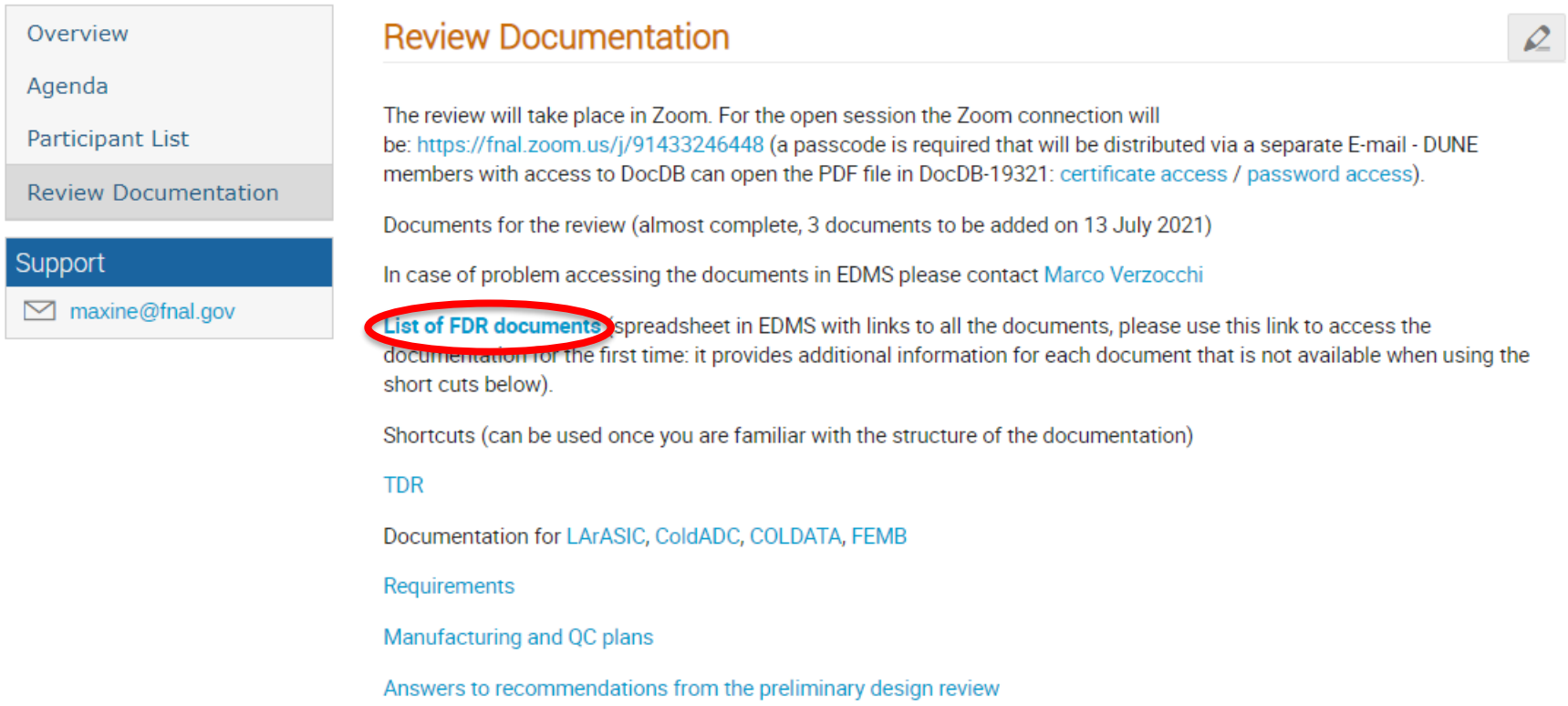
Scope of the Review (ii)

- Detailed charge available in EDMS

1. Recommendations from previous reviews
2. Specifications / test results ?
3. Meet performance requirements ? Fixed issues in previous round of prototypes ?
4. System tests ? Future tests ?
5. Issues with procurements for ASICs/FEMBs ?
6. QA/QC plan ?
7. Is there any problem we didn't consider ? Are we ready for the submission of the engineering run
8. Part breakdown structure / schedule / costs

Guide to the Documentation (i)

- From the Indico agenda page



Guide to the Documentation (ii)

- In EDMS:

Category	Document	EDMS	File Name	Description
Design Documents	TDR Chapter	CERN-0000219276	DUNE-FD-TDR-vol-IV-SP-for-arxiv.pdf	DUNE Technical Design Report, Volume 4: DUNE FD SP Technology (copy or arXiv:2002:03010, also published in JINST 15 (2020) 08, T08010
			DUNE_TDR_SinglePhase_TPCElectronics_from_arXiv-2002.03010_Chapter4_only.pdf	Chapter 4: TPC Electronics only (subset of the previous document)
	Design Updates		This document will not be available for the ASIC FDR of 21-22 July 2021, please see the datasheets for LArASIC, ColdADC, and COLDATA instead	An updated Chapter 4 with all new design, construction, and installation information included. This file can be viewed as a drop in replacement for the original Ch. 3 in the TDR. Document will be prepared for the overall FDR of the TPC Electronics (September/October 2021)
	LArASIC Documentation	2314428	LArASIC_P5_Datasheet_V1.pdf	Datasheet for version P5 of LArASIC. Includes expected performance from simulation.
			LArASIC_P5A_Datasheet_V1.pdf	Datasheet for version P5A of LArASIC. Version P5A is identical to version P5 except that it includes different combinations of ESD protections and RQI subtraction (channel dependent), as discussed on pages 4 and 5 (otherwise the two documents are identical)
			Not yet available	Datasheet for version P5B of LArASIC. In preparation, will not be available for the ASIC FDR of 21-22 July 2021.
			LArASICDevelopment.docx (document updated 7/14, added appendix on ESD protection and Reset Quiescent Current)	This document starts with the measurements performed on the P4 version of LArASIC, followed by the design changes that were implemented as a consequence in the P5 version, as well as the tests done in a parallel development (P5A) to improve the ESD protection and try to understand the issues related to RQI subtraction. The document ends with the measurements of the P5/P5A performance, and with a proposal for the reticle for the engineering run of LArASIC.
			P5LArASICDesignSimulation.pdf (document added 7/14)	Design and simulation of the single ended to differentail buffer.
	ColdADC Documentation	2314429	ColdADC_-_Summary_of_Design_Modifications_-_v2.docx	Summary of the design changes introduced between version P1 and version P2 of ColdADC
			ColdADC_-_Expected_Performance_from_Simulation_v2.docx	Expected performance of version P2 of ColdADC based on simulation
			COLDADC_P2_Datasheet.pdf	Datasheet for version P2 of ColdADC.
			COLADC_P2_Testing_v3.docx (document uodated 7/15, replaced figures 13-15)	Measurements of ColdADC P2 performance
	COLDATA Documentation	2314430	COLDATA_P3_Datasheet.pdf (updated to verson 1.7 on 7/14, see change log for details)	Datasheet for versions P3 of COLDATA
			COLDATA_Design_Changes_v3.docx (posted 7/14)	Design changes from the P2 version of COLDATA to the P3 version (and proposed design chanes for the P4 version).
			COLDATA_P3_Testing.docx (posted 7/14)	Measurements of the COLDATA P3 performance
	ColdADC/COLDATA Reticle	2588343	IMEC_reticle.pdf	Description of the ColdADC and COLDATA reticle provided by IMEC
			ColdADC_COLDATA_Reticle.layout	LayoutEditor macro used to generate a simplified view of the ColdADC/COLDATA reticle
			ColdADC_COLDATA_Reticle.gds	GDS file of the ColdADC/COLDATA reticle created with LayoutEditor
			ColdADC_COLDATA_1x1.pdf	PDF file of the ColdADC/COLDATA reticle (1 reticle) including all test structures
			ColdADC_COLDATA_3x3.pdf	PDF file of a 3x3 matrix of the ColdADC/COLDATA reticle without the test structures
	FEMBs	2588344	FEMBDevelopmentPower.20210712.docx	Document describing the current status of the FEMBs for DUNE and future development. Also included are results from system tests of the FEMBs.
			DUNE_Monolithic_FEMB_Schematics.pdf	Schematics of the current monolithic FEMB prototype
			DUNE_Monolithic_FEMB_Layout.pdf	Layout of the current monolithic FEMB prototype
			DUNE_Monolithic_FEMB_Bill_of_Materials.xlsx	Bill of materials for the current monolithic FEMB prototype

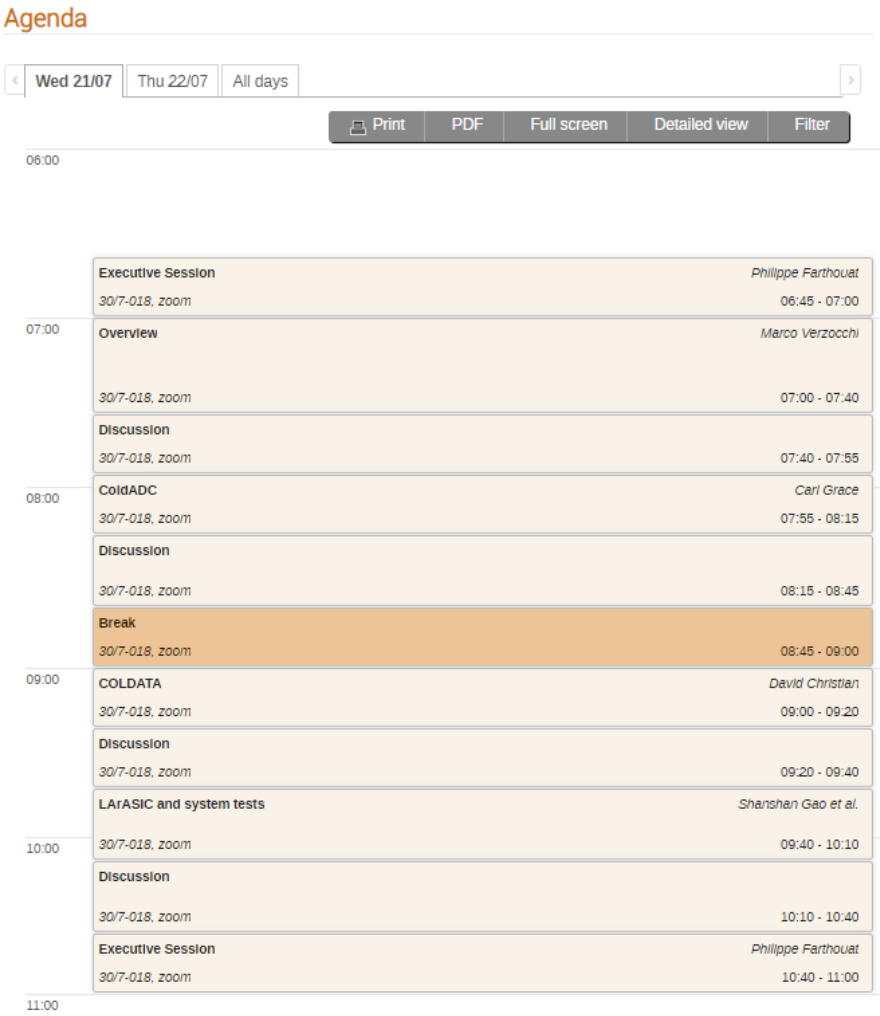
Guide to the Documentation (iii)

- In EDMS:

Category	Document	EDMS	File Name	Description
Requirements Documents	Summary of requirements on ASICs	2397298	ASIC_Requirements_v3.docx	Summary list of the requirements affecting the DUNE ASICs
	EB-Held Requirements	2346091	Far_Detector_EB_held_specifications_5June2020-2.xlsx	Complete list of all the top level specifications for the first DUNE far detector module (approved by the DUNE executive board)
	TB-Held Requirements	2384645	Far_Detector-TB-held-specifications-12JUN2020-update28sep2020.xlsx	Complete list of all the specifications for the first DUNE far detector module that required for integration and installation purposes (require approval by the DUNE technical board)
	Consortium-held Requirements	2397298	DRAFT_Far_Detector_SP_consortium_specifications_12Jul2021.xlsx (document updated 7/16, fixed typo in ENOB requirement)	Spreadsheet with all the requirements / specifications, including those determined by the individual consortia
Production and QC plans	Preliminary Manufacturing and Procurement Plan and Preliminary QC Plan	2604783	2604783_ASIC_Production_QC (need to update the document to add sections on cost estimates and more details on the schedules)	Document describing the production plans and the preliminary quality control procedures for the ASICs. This includes a detailed description of the measurements to be performed as well as a conceptual design of the test equipment.
Previous Reviews	Answers to the recommendations from the February 2020 review	2401928	DUNE-SP_CE_FEMB_2002_recommendations_v2b.xlsx	Response to the recommendations from the FEMB review of February 2020. The TPC Electronics consortium proposes to consider six of the eight recommendation closed (in one case in a non-entirely satisfactory way). One recommendation (accelerated aging measurements is still in progress), while the last one is related to the CRYO ASIC and is no longer considered relevant).

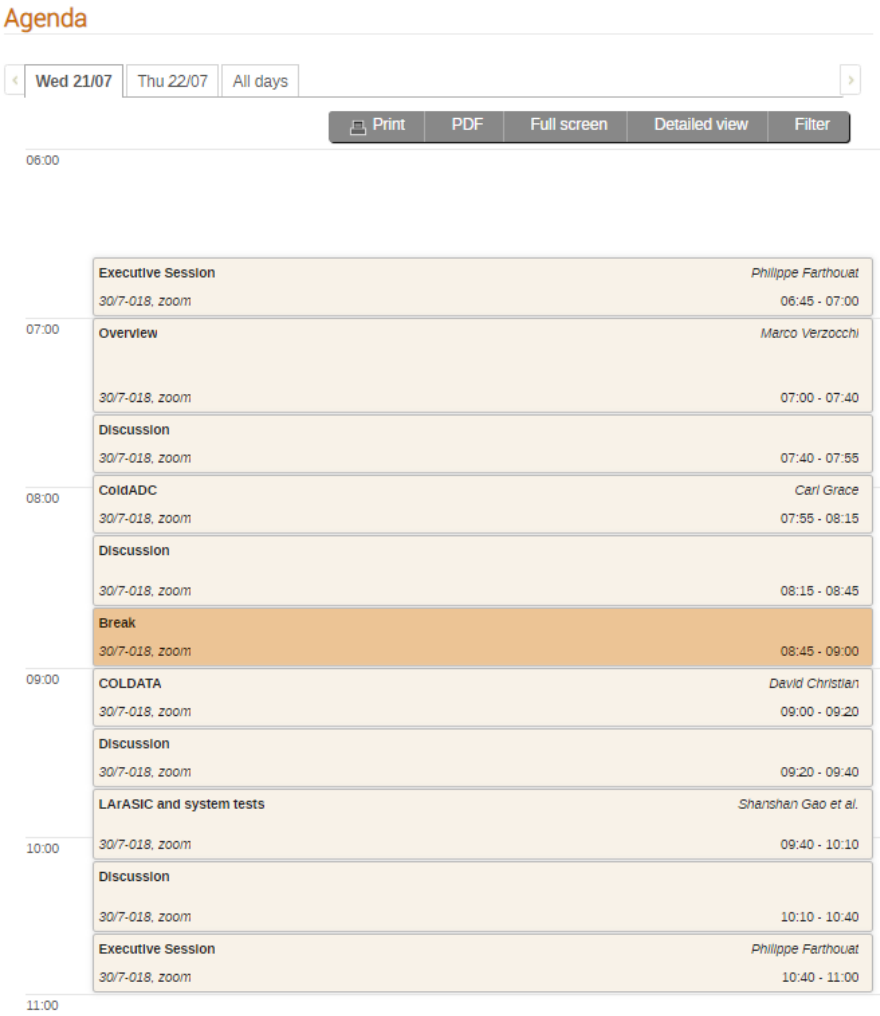
Today's Agenda (i)

- The idea of presentations is to focus on measurements done on the more recent generation of prototypes and demonstrate that the ASICs meet all the requirements for DUNE
- We want to leave a lot of time for discussions and Q&A
- Tomorrow reserved for Q&A or other presentations if needed
- We have backup material ready, largely based on the documentation posted in EDMS



Today's Agenda (ii)

- We are not ready for a final design review of the FEMBs
- FEMBs discussions should be limited to system test results and questions on whether there is anything related to the FEMB requirements / interface to WIB that would necessitate design changes on the ASICs



Requirements on FE electronics (i)

- Revisited and improved the list of specifications for the ASICs:
  - System noise < 1,000e^-
  - FE shaping time adjustable in the 1-3 μs range
  - Signal saturation level 500,000 e^-
  - ADC sampling frequency ~2 MHz
  - 12 bits ADC
  - Power consumption < 50 mW/channel
  - Non-FE noise contribution << 1,000 e^-
  - Fraction of dead channels < 1% over lifetime

Requirements on FE electronics (ii)

- Revisited and improved the list of specifications for the ASICs:
  - Two baselines in the FE amplifier
  - Gain: ~10 mV/fC
  - Capability of synchronizing the system at the < 50 ns level
  - 128 channels per FEMB
  - Data transmission at ~1.28 Gbps (now it's 1.25 Gbps)
  - Detector capacitive load 120-210 pF (test with 150 pF)
  - Channel to channel cross talk < 1%
  - Monotonic saturation recovery
  - Double pulse resolution ~5 mm

Requirements on FE electronics (iii)

- Revisited and improved the list of specifications for the ASICs:
  - ADC Dynamic Nonlinearity (DNL) < 1 LSB at 88 K
  - ADC Integral Nonlinearity (INL) < 1 LSB at 88 K
  - ENOB > 10.3 bits at 88 K for signals with frequencies up to 410 KHz (use 150 KHz for performance measurements)
  - ADC overflow/underflow protection

- The presentations on LArASIC, ColdADC, COLDATA discuss how these requirements are met by the various ASICs and with system tests

From previous review (i)

DUNE-SP_CE_FEMB_PDR_2002_recommendations								
TITLE	DATE	REVIEW #	#	System	Subsystem	RECOMMENDATION	OWNER	RESPONSE	Status
DUNE-SP TPC electronics FEMB/ASIC PDR	2020-02-05	2020-01	1	TPC Electronics	ASIC and FEMB	A complete and coherent list of specifications from both developments should be agreed and established. This includes: * Input capacitance to be updated (150pF instead of 220pF) Maximum allowed clock jitter on the received clock * Maximum noise on power supplies (ripple vs frequency) and expected range of allowed PS * Minimum acceptable ENOB. Is 10 bits enough? * Double pulse resolution and settling time * Overload recovery (maximum recovery time vs overload) * Maximum acceptable crosstalk * Specifications for the FEMB (there are currently none) * For the 3-chip solution, all the interfaces (clocks, communication, data path) between COLDATA, COLDADC and LArASIC are to be fully specified and documented. It is recommended to review these specifications with all development teams prior to submission of these chips.	Christian, Verzocchi	We have updated our requirements document, which needs to be finalized (not in the area of ASICs) and approved by the technical board. This addresses all the point about specifications. The interfaces between the 3 ASICs are completely defined. We have not included yet the maximum noise for the power supplies, as this depends on the exact configuration of the power distribution chain that involves DC-DC voltage regulators, LDOs, and filters on the PTC/WIB, and additional LDOs and filters on the FEMB. This specification should be reviewed during the final design review of the overall TPC Electronics in September/October 2021	Closed
TPC electronics FEMB/ASIC PDR	2020-02-05	2020-01	2	TPC Electronics	ASIC and FEMB	The ASIC specifications, for parameters such as "ENOB", "SNR", noise and others, must explicitly list the testing conditions, such as the loading capacitance and shaping time for the noise tests, the sampling frequency for the ENOB tests, and so on.	Christian, Verzocchi	We have agreed on using 150 pF for the loading capacitance, 150 kHz for the ENOB tests (we plan to test also other frequencies).	Closed
DUNE-SP TPC electronics FEMB/ASIC PDR	2020-02-05	2020-01	3	TPC Electronics	ASIC and FEMB	The design methodologies and verification methodologies need to be clarified and improved for all the ASICs.	Christian, Verzocchi	The verification methodologies for ColdADC and COLDATA have been improved, and for both chips this can be claimed to be a success: version p2 of ColdADC has no problems. Version p3 of COLDATA (the second complete version) has two small features that did not prevent us from using this version to build FEMBs. In both cases the problem can be traced back to an incomplete definition of the interface between COLDATA and other systems (the FEMB in the case of I/O bits and LArASIC in the case of the asymmetric clock). These problems have been corrected in the p4 prototype. In the case of LArASIC while there have been improvements in the verification, we have been forced to make a new prototype (p5) that was not in our development plan. There are two reasons for this: in the case of the RQI subtraction circuit, we are suffering from the limitation of the cold models (the spread of parameters is not available). In the case of the single-ended to differential output buffer the issue is the limited phase margin and this could / should have been seen in simulation prior to the submission.	Closed
DUNE-SP TPC electronics FEMB/ASIC PDR	2020-02-05	2020-01	4	TPC Electronics	ASIC and FEMB	Concerning the cold temperature models, a drop-in test structure with standard transistors could be designed and used to follow lot to lot process variations in the cold. This methodology is used for checking the radiation hardness of some technologies: test structures are added to each submission and measured. Transistor matching data as a function of temperature should be derived from measurements and used in simulations.	Christian, Verzocchi	A ring oscillator has been added to the ColdADC design and already tested in the chips received back from the foundry. This will cover the process variations for ColdADC and COLDATA. We are considering adding a separate chip in the LArASIC reticle, since we do not want to add a structure inside the chip itself. We have finally received new cold models for the 180 nm technology, which will be used prior to the final submission of LArASIC (there were held back for over a year due to legal issues with a non-disclosure agreement). These models have arrived too late to be useful for the design of LArASIC, ColdADC, or COLDATA, but they will be used in the design of the ASIC for the near detector liquid Argon TPC. Like in the case of the 65 nm models, these models do not describe the spread of the parameters in cold, and for that we have to assume that the spread is the	Closed

From previous review (ii)

DUNE-SP_CE_FEMB_PDR_2002_recommendations									
DUNE-SP TPC electronics FEMB/ASIC PDR	2020-02-05	2020-01	5	TPC Electronics	ASIC and FEMB	A program and protocol for accelerated aging tests should be agreed and established for both solutions.	Christian, Verzocchi	We have started the program of accelerated tests on ColdADC and we have plans in place for the accelerated tests of LArASIC. For COLDATA we are in the process of designing a test board that can ve used for the accelerated test and we are discussing how to monitor the performance of the chip as a function of time. We expect to complete the accelerated aging tests before the production readiness review that will give the go ahead for the fabrication of the ASICs to be used in the first and the second DUNE far detector modules.	In progress
TPC electronics FEMB/ASIC PDR	2020-02-05	2020-01	6	TPC Electronics	ASIC and FEMB	Using a single clock source as master clock for all functions should be considered for the 3-chip solution (already done for the CRYO solution). In particular, as part of the design changes to be done for the COLDATA PLL, it should be considered to use the master 62.5MHz clock as input.	Christian, Verzocchi	This change has been implemented in the second prototype of COLDATA that was submitted for fabrication in September. This recommendation was closed in March 2021 after demonstrating that the new COLDATA works as designed with a single external clock at 62.5 MHz.	Closed
DUNE-SP TPC electronics FEMB/ASIC PDR	2020-02-05	2020-01	7	TPC Electronics	ASIC and FEMB	For the 3-chip solution, the design of a single FEMB housing all the chips (i.e. no mezzanine) is to be pursued.	Christian, Verzocchi	Initial tests of the FEMBs with the three ASIC solution (LArASIC, ColdADC, and COLDATA) have been performed using a stacked FEMB (i.e. analog motherboard with LArASIC and ColdADC and digital mezzanine with COLDATA). The design of the monolithic FEMB has been developed and the first prototype of this board is currently under test. Results will be reported during the review of 21-22 July 2021.	Closed
DUNE-SP TPC electronics FEMB/ASIC PDR	2020-02-05	2020-01	8	TPC Electronics	ASIC and FEMB	The DUNE CRYO ASIC should be submitted only when all missing tests with nEXO version are finished. In particular, the test with the APA is to be done prior the submission. The schedule of this test is to be revisited if the DUNE CRYO is to be submitted in July.	Christian, Verzocchi	The progress with the development of the CRYO ASIC has been quite slow and system tests have not been performed yet (we hope to make a first test in ICEBERG in August 2021). The development of CRYO at this point is continuing outside of the scope of the DUNE-US project.	No longer relevant

- Out of 8 recommendations from the previous review we think we have satisfied 6 of them
- One (related to CRYO) is no longer relevant (system tests of CRYO are in progress, the SLAC group proceeded with the 2nd submission without waiting for the results)
- One (lifetime measurements) is in progress

Recommendations - Closed

1. Specifications – see previous slides
2. Specify testing conditions for the measurement of the ASIC parameters (done, see presentations on LArASIC/ColdADC)
3. Clarify design and verification methodologies
   - We were not perfect: improvements on all ASICs, but there was one problem in LArASIC p4 and two small problems in COLDATA p3 that should have been caught in verification
5. Add test structures to follow lot-to-lot process variations
   - Added ring oscillator on ColdADC (checks also COLDATA, same reticle)
6. Use a single clock for COLDATA
   - Done
7. Develop a single PCB housing all the ASICs on the FEMB
   - Done

Recommendations - Ongoing

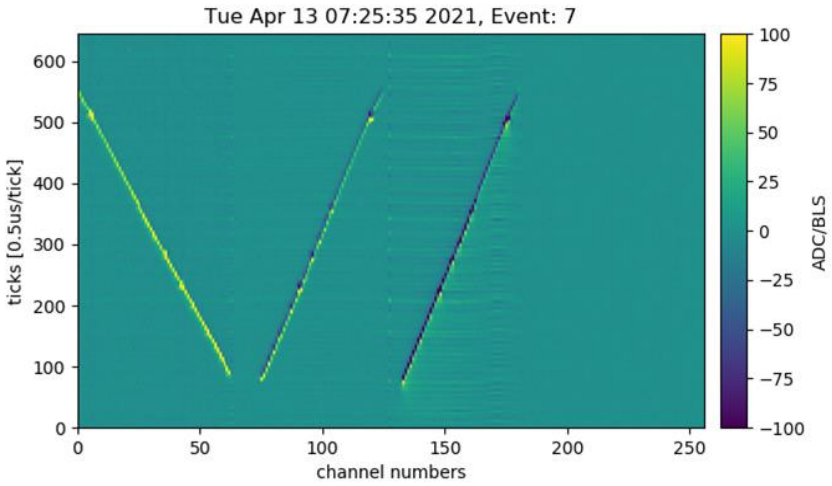
4. Protocol for accelerated aging tests
   - We are not where I would like to be on this issue
   - Started measurements with ColdADC (to be discussed in Carl Grace talk, it turns out it's hard to kill a chip…..)
   - Plan in place for LArASIC (in Shanshan Gao's talk)
   - Developing test board for COLDATA
   - We will have results prior to the production readiness review

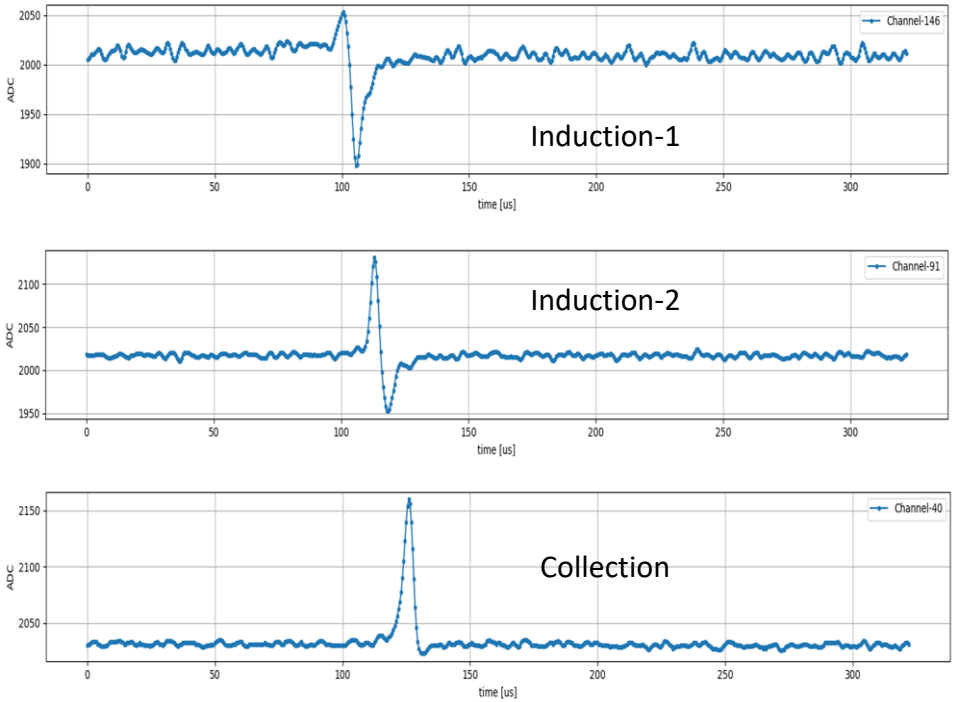
Future Tests

- Shanshan will cover initial tests with first prototype monolithic (all the ASICs on a single PCB) FEMB using LArASIC p5, ColdADC p2, COLDATA p3
  - We plan on making a few more of these FEMBs and possibly test them on a small APA
- We will need a 2nd iteration of the monolithic FEMB with the following modifications
  - Reduce number of connections between WIB and FEMB (both power and signal cables)
  - Decide which calibration signals from the WIB and which analog monitor signals from the FEMB we want to route
  - Plan on having few FEMBs available in the Fall (require new WIB, new cables, ongoing)
- Production of large number of FEMB's PCBs to be done in the Fall, in such a way that we can populate them with the ASICs from the engineering run
- Use those FEMBs for ProtoDUNE-HD-II

Vertical Drift Detector (i)

- Are any changes needed for the Vertical Drift Detector ?
  - Tests done so far on small prototypes (max 32 cm * 32 cm) have used the SBND FEMBs and show excellent results / signal over noise ratio





Vertical Drift Detector (ii)

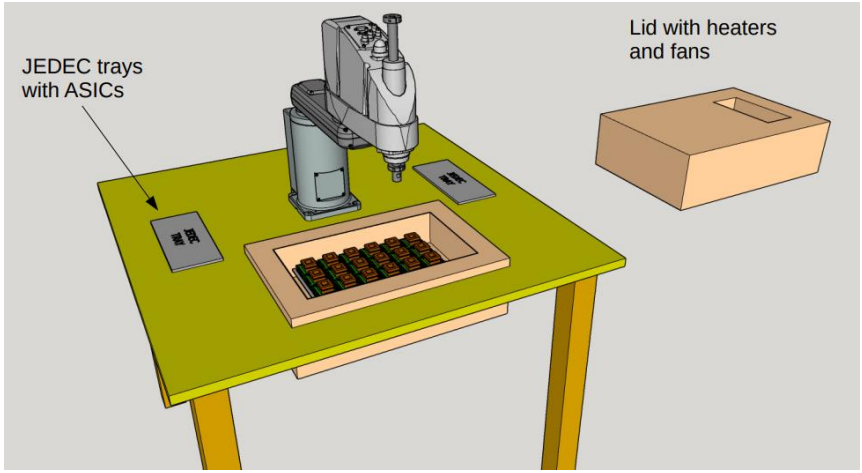
- Are any changes needed for the Vertical Drift Detector ?
  - We are planning for full scale CRP tests
    - Later this year: use ProtoDUNE FEMBs (LArASIC p2)
    - Next year: use ProtoDUNE-II FEMBs (LArASIC p5, ColdADC p2, COLDATA p4)
- Any design changes at the ASIC level ? At the FEMB level ? No and maybe:
  - Need to check whether COLDATA can drive signals through 2 cable segments in order to add patch panel on CRP
    - short (3.5 m max) MiniSAS or SAMTEC cable from the FEMB to the patch panel, followed by long (23-24 m) SAMTEC cable to the CE flange
  - We can do this with a single SAMTEC cable of equivalent length, but having the patch panel would simplify installation of CRPs in the vertical drift detector

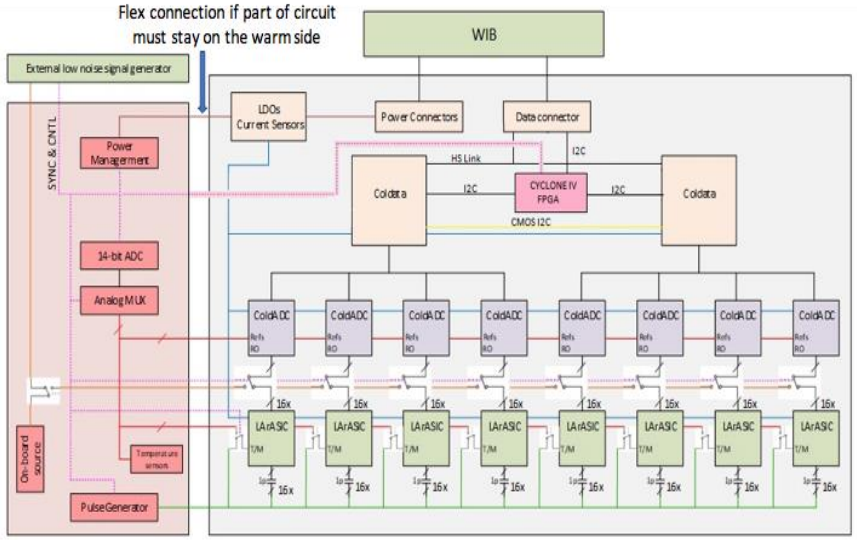
Quality Assurance / Quality Control

- All what we have been doing and we will continue doing with standalone ASIC tests, ProtoDUNE-II, system tests and lifetime tests is quality assurance
- We are also laying the foundations for a solid quality control program during production based on the experience gained with the QC testing during the construction of the detector components for ProtoDUNE
- We have formed a task force to discuss the requirements for test boards / cryogenic test system for the QC program for DUNE
- A preliminary version of the QC program with details on the measurements to be performed was provided in EDMS

Quality Control

- Cornerstones of the QC program
  - Each ASIC will have a unique identifier on the packaging that follows the rules of the DUNE parts breakdown structure. This PBS id will be used to record all the properties of each ASIC in the calibration DB.
  - All ASICs need to be tested both at room temperature and in LN_2 to ensure that the fraction of FEMBs that are reworked due to failures seen only in cryogenic liquids is minimal
    - It will take us a while to demonstrate that maybe we can do without the tests in LN_2
  - Given the number of ASICs to be tested we need a robotic pick and place system
  - We have tried several ideas on how to merge the two aspects and we have a conceptual design that we are trying to develop into a real system over the next few months
  - We also have a conceptual design for a test card capable of testing multiple ASICs at once, based on the experience gained with previous test cards and FEMBs





- Final ASIC selection criterias to be determined in time for the production readiness review

Production (i)

- Assuming the engineering run and further tests with ProtoDUNE-II (and with vertical drift detector prototypes) are successful, we expect to be ready to launch production of the ASICs for the 1st and 2nd DUNE far detector modules at the beginning of 2023
- This also depends on the overall approval status of the project in the US which we expect to get on the same timescale
- The timescale for making all the ASICs and FEMBs for 2 FD modules is ~2.5 years
- Early start will be important to avoid issues in the ASIC industry that are not likely to be solved before the 2024-2025 timescale

Production (ii)

Number of ASICs (assume 10% of spare FEMBs)		
ASIC	FD-1 (3,000 FEMBs)	FD-2 (1,920 FEMBs)
LArASIC	26,400	16,900
ColdADC	26,400	16,900
COLDATA	6,600	4,225
Number of wafers (325 LArASIC, 750 ColdADC, 255 COLDATA per wafer)		
LArASIC	4*25	(2-4)*25
ColdADC / COLDATA	2*25	(1-2)*25

- The number of wafers for FD2 depends on the yield of the ASICs from FD1. The minimum yield that can be accommodated for FD1 is 81.2% (LArASIC), 70.4% (ColdADC), 51.7% (COLDATA)
- After the selection of LArASIC p5 vs p5b it may be more economical to make a second engineering run if we are approved to build two far detector modules

Next Presentations

- Going through the presentations in the following order

1. ColdADC (Carl Grace, LBL)
2. COLDATA (David Christian, Fermilab)
3. LArASIC and System Tests (Shanshan Gao, BNL)

- I hope that these presentations will convince you that the ASICs meet all the requirements for the DUNE experiment and that we are ready for a submission of the engineering runs for LArASIC (180 nm TSMC) and ColdADC/COLDATA (65 nm TSMC) with minimal risks

Next Presentations

- We have reserved as much time as possible for discussion after the presentations
- We have supporting material that can be shown if necessary
- We would like to reserve as much time as possible tomorrow for further Q&A and we would like to leave some time to the committee for a brief executive session today, in such a way that there is time to send us questions in advance of tomorrow session

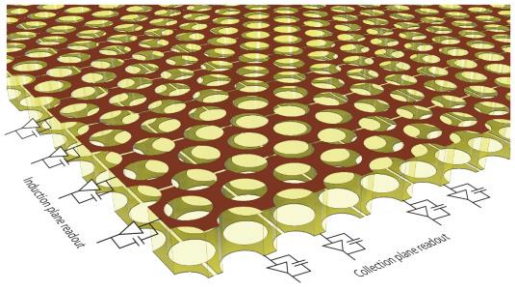
Questions ?

Backup Material

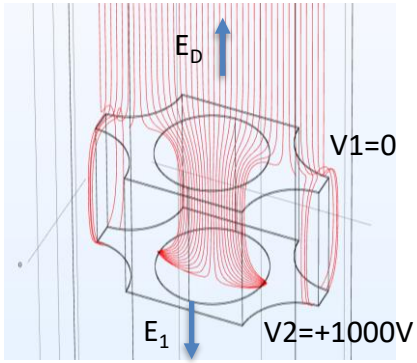
- Signals on the CRPs from the vertical drift detector

Electron Transport Through the Perforated PCBs

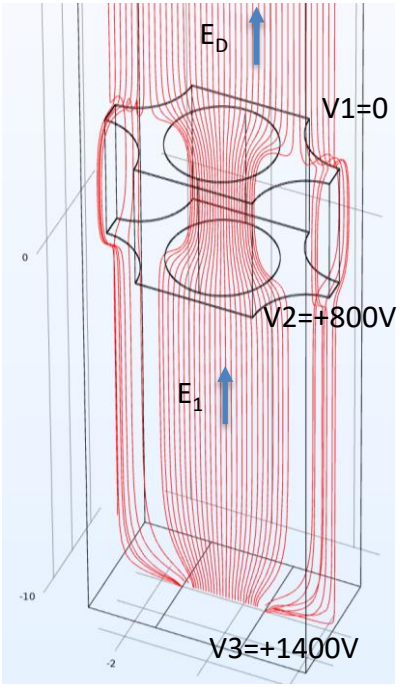
- Electron transport and amplification through perforated electrodes in gas was introduced by F. Sauli at CERN in the form of Gas Electron Multiplier (GEM). Multi-layer GEM was used to multiply electrons to sufficient level to be detected on the collecting anodes with various strip patterns.
- The same principle can be used to transport electrons through multiple layers of electrodes, and detect the current signals induced on the electrodes as the charges move toward or away from it.
- The perforated PCBs used in the SPVD TPCs are thicker with larger holes than the GEM, or LEM used in NP02.
- The E field inside the holes needs to be >5x that of the drift field on the entrance side, and to extract the electrons out of the exit side, the transfer field needs to be no less than the drift field. If the electrons are to be collected on the exit side of the holes, a strong reverse field is preferred to minimize the overshoot of electrons.



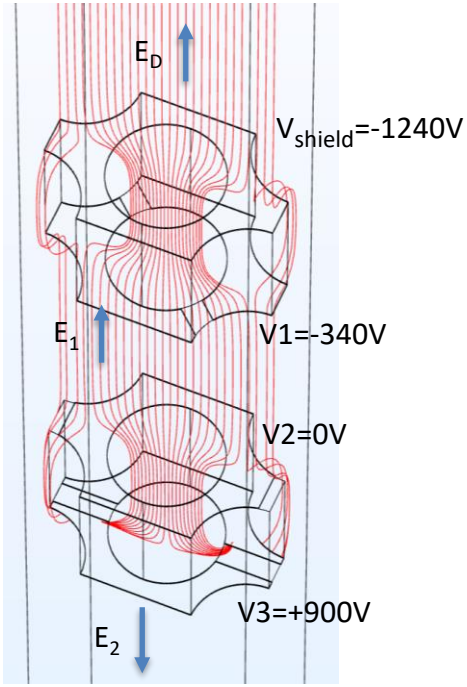
A detailed view of a corner of the 2-view perforated anode PCB.



Electron paths from a line charge in a 2-view configuration



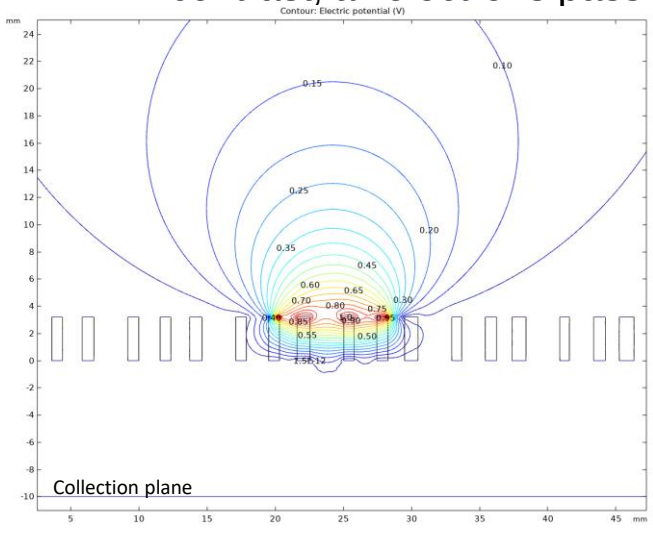
Electron paths from a line charge in a 3-view configuration



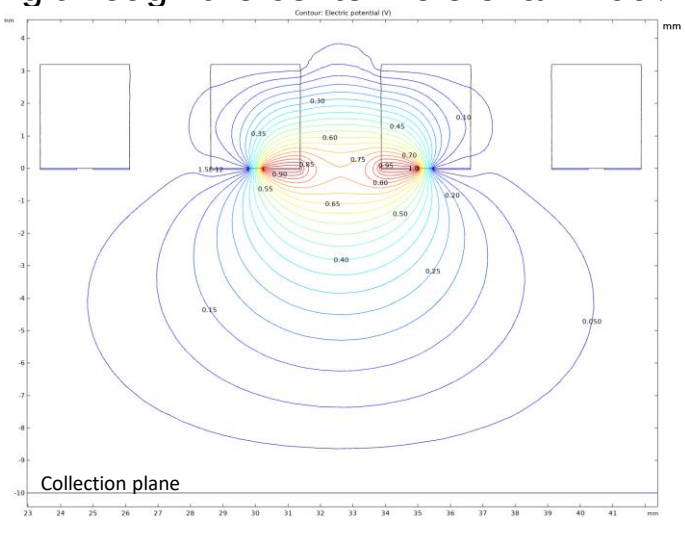
Electron paths in a 3-view configuration with a shield plane facing the cathode.

Weighting Potential Distribution

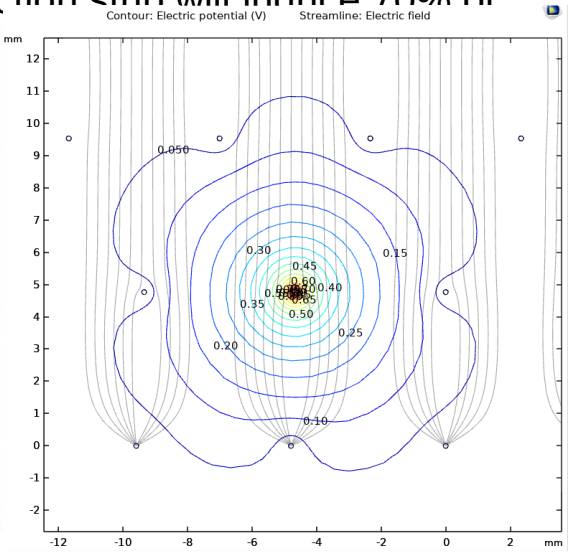
- One major benefit of using the perforated double-sided PCB anode is the strong induction signals. This is largely due to the more expansive induction electrodes, and their proximity to the electron drift paths.
- With the APA wire grid, the weighting potential distribution of a given induction plane wire falls off very quickly w.r.t. the distance from the wire surface. For example, if a point charge is more than 0.7mm from the center of the sense wire, the induced charge has dropped below 50%. Most of the electrons from a track segment are further away from the sense wire and therefore induce far less signal.
- In contrast, all electrons passing through the center hole of an induction strip will induce 70% or



Weighting potential contours of a 1st induction plane strip of the 3-view configuration

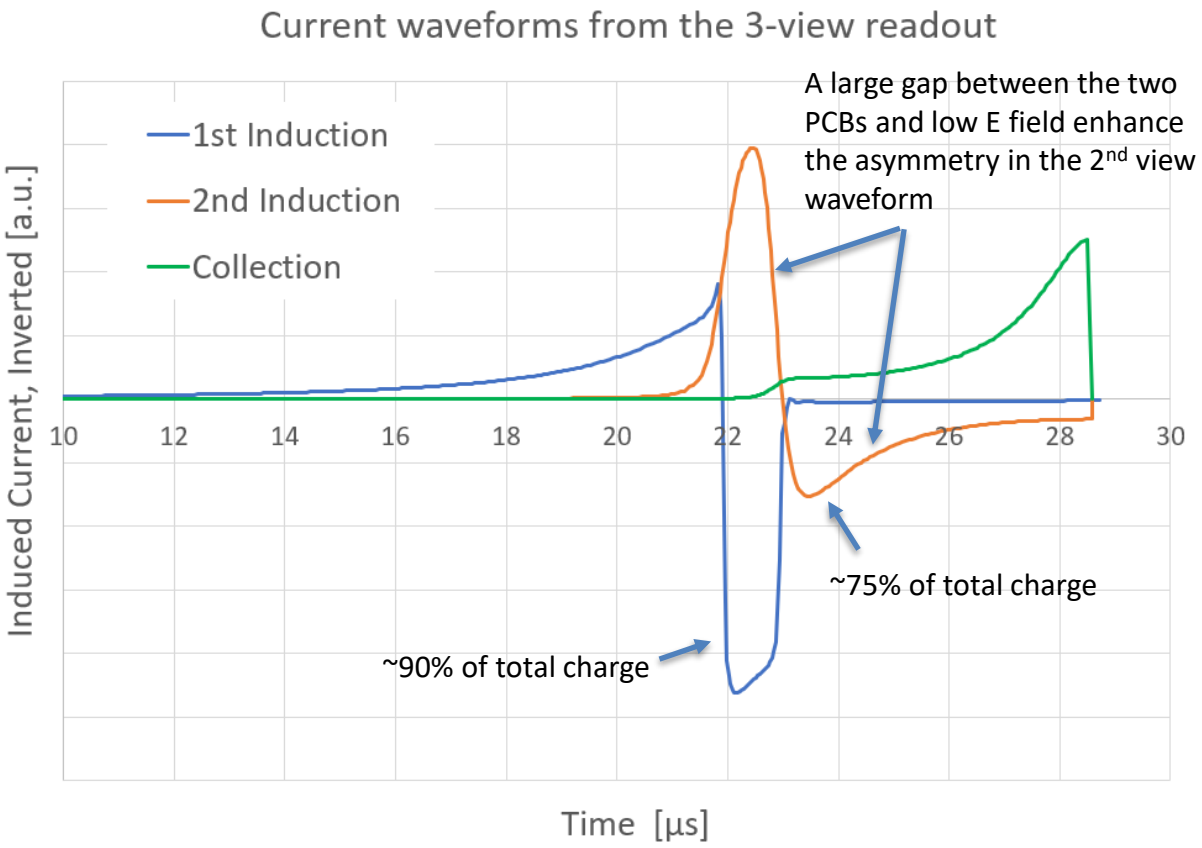


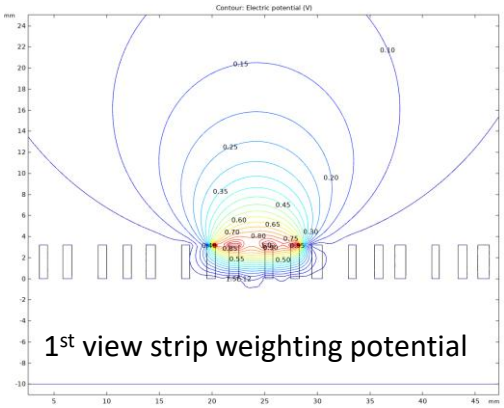
Weighting potential contours of a 2nd induction plane strip of the 3-view configuration

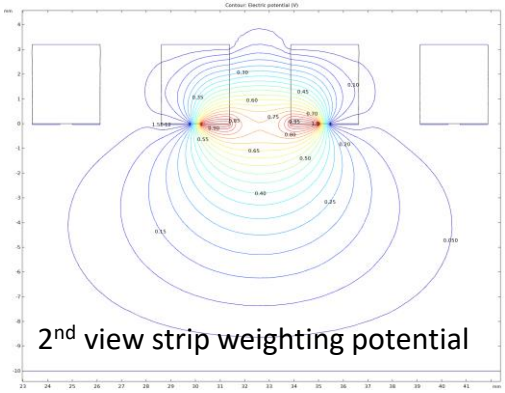


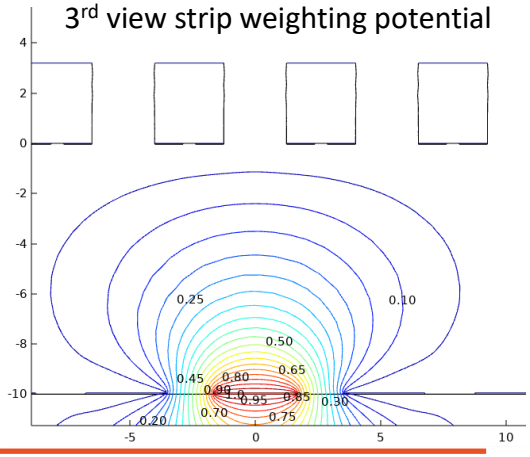
Weighting potential contours and the electron drift lines (gray) in a small section of the APA wire grid.

Simulated Current Waveforms, 3-View









Point charge drifts through the middle of a strip on each view