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U.S. DEPARTMENT OF ENERGY
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DUNE ColdADC FDR

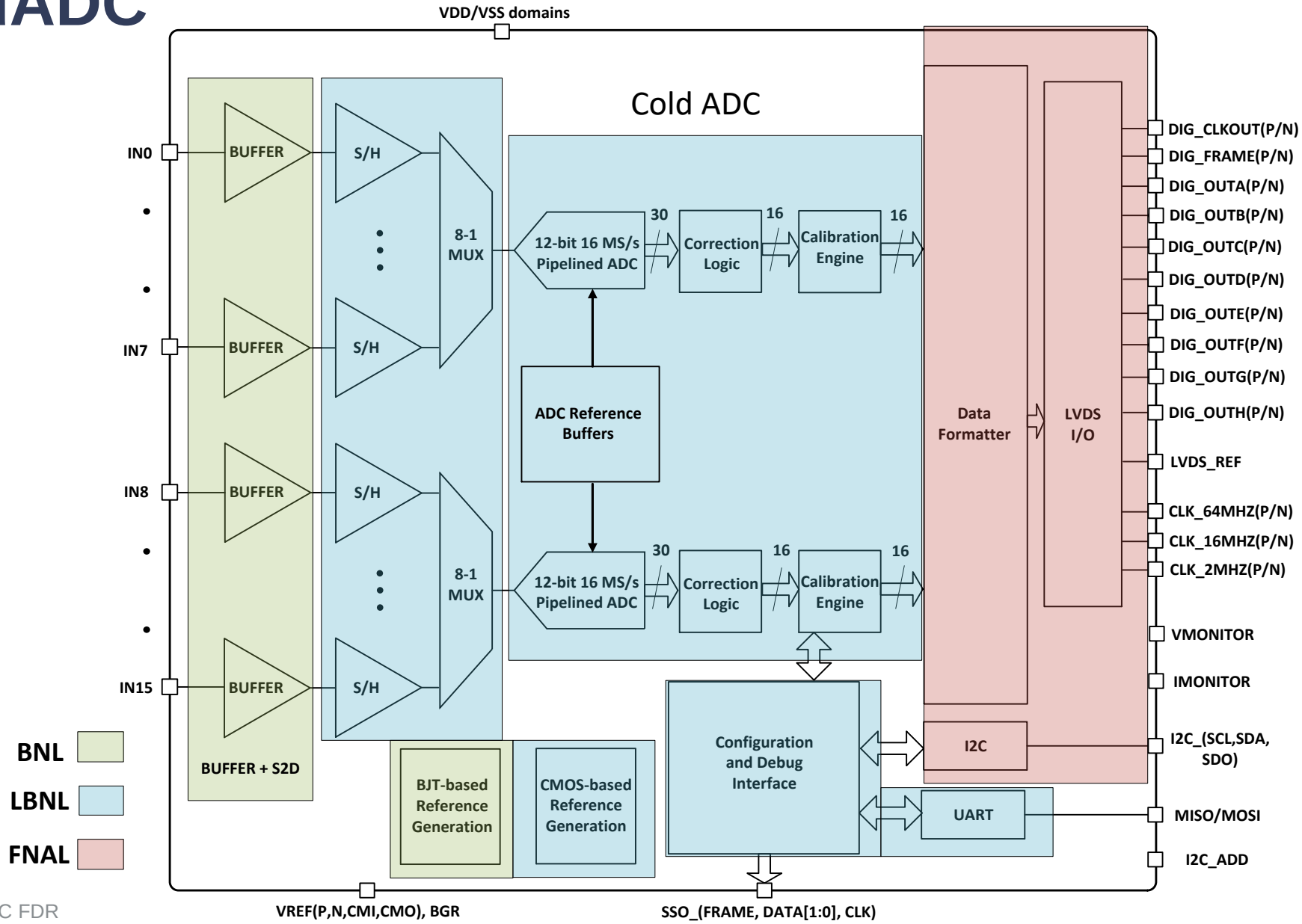
Carl Grace, on behalf of ColdADC Design Team – July 21, 2021

Lawrence Berkeley National Laboratory

Executive Summary

- The ColdADC was reviewed in January 2020 at the CERN Front-End Motherboard and ASIC Review
- A number of planned design modifications and bug fixes were presented
- **The current version of ColdADC, ColdADC_P2 (received September 2020) meets requirements and all bug fixes and modifications work as expected.**

ColdADC


VDD/VSS domains
Cold ADC
IN0
IN7
IN8
IN15
BUFFER
S/H
8-1 MUX
12-bit 16 MS/s Pipelined ADC
30
Correction Logic
16
Calibration Engine
16
ADC Reference Buffers
Data Formatter
LVDS I/O
DIG_CLKOUT(P/N)
DIG_FRAME(P/N)
DIG_OUTA(P/N)
DIG_OUTB(P/N)
DIG_OUTC(P/N)
DIG_OUTD(P/N)
DIG_OUTE(P/N)
DIG_OUTF(P/N)
DIG_OUTG(P/N)
DIG_OUTH(P/N)
LVDS_REF
CLK_64MHZ(P/N)
CLK_16MHZ(P/N)
CLK_2MHZ(P/N)
VMONITOR
IMONITOR
I2C_(SCL,SDA, SDO)
MISO/MOSI
I2C_ADD
BUFFER + S2D
BJT-based Reference Generation
CMOS-based Reference Generation
Configuration and Debug Interface
I2C
UART
BNL
LBNL
FNAL
VREF(P,N,CMI,CMO), BGR
SSO_(FRAME, DATA[1:0], CLK)

Summary of Key Design Changes

Change	Bug Fix, Performance enhancement, or New Functionality?	Comment
Input Buffer Level Shifters added	Bug Fix	Critical fix
Bandgap reference opamp flavor	Bug Fix	
IR drop at room temperature	Performance Enhancement	
ADC Auto-Calibration	Bug Fix	Critical fix
ADC Core Linearity	Performance Enhancement	
ADC Mux Linearity	Performance Enhancement	
ADC Crosstalk	Performance Enhancement	
ADC Data Overflow	Bug Fix	
Reset Sync	Performance Enhancement	
Power-On Reset	New Functionality	
Process Monitor (Ring Oscillator)	New Functionality	

Discussion of Key Changes

- Both of the critical fixes (input buffer level shifter omission and auto-calibration timing failure) were due to communication failures between labs

- To fix these, and ensure other issues were not created we took several steps to improve our communication and verification during the P2 design process:

1. Developed full-chip simulation using industry standard UVM (universal verification methodology) and two labs (FNAL and LBNL) ran overlapping simulations
2. Created spreadsheet for every signal and block, checked twice by engineers at different Labs
3. Implemented single digital block for chip (to empower automated timing checks)

Input Buffer Level Shifters

- Issue: Digital level shifters that convert from core voltage to voltages used in ADC were omitted in the final design
- Effect: VDDD needed to run at elevated supply
- Root cause: Communication error between labs
- Fix: Correctly insert level shifters, more importantly have engineers at different labs check schematics for omissions
- Result: P2 buffers worked as expected

Bandgap Opamp Flavor

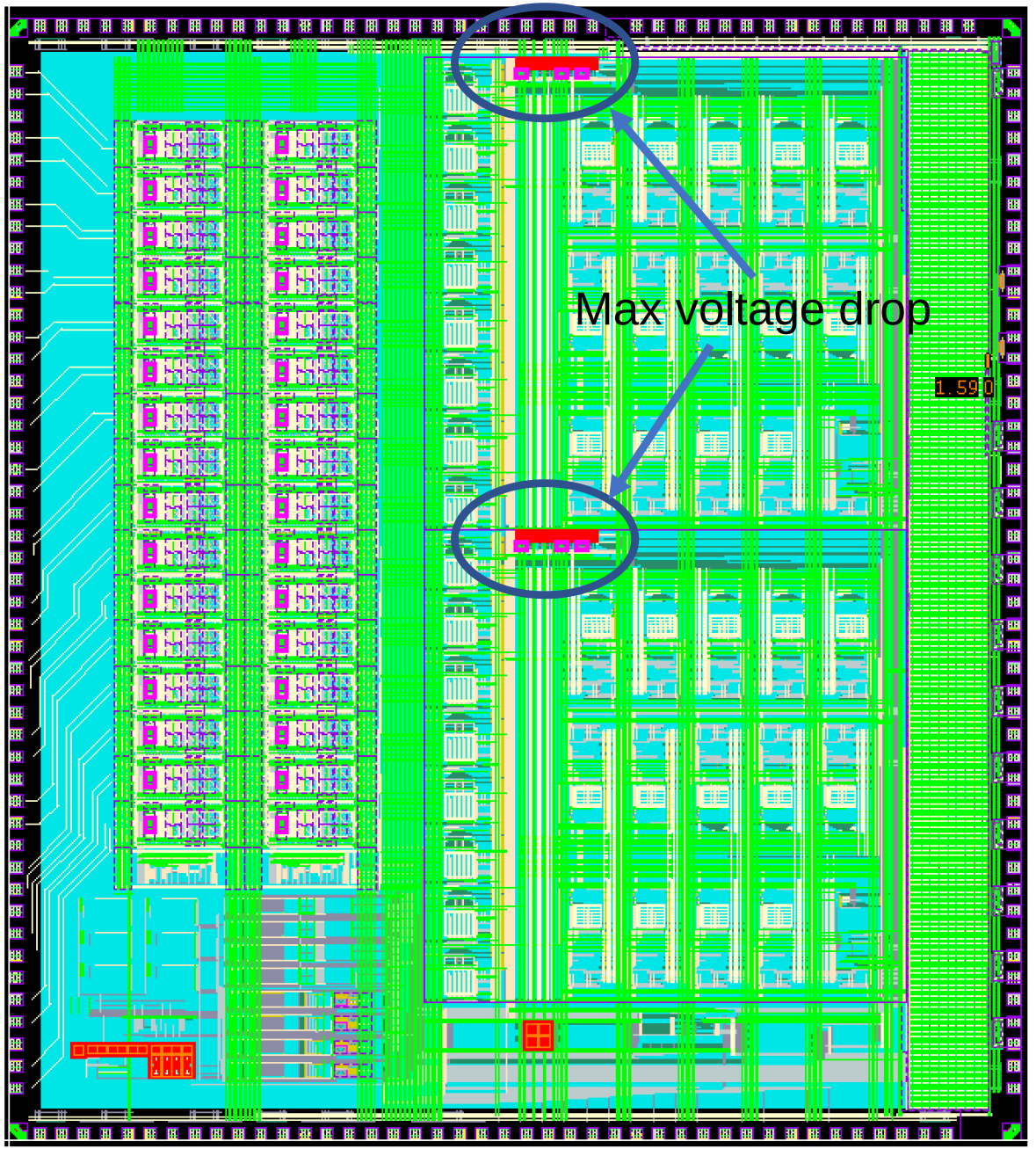
- Issue: Opamp of wrong polarity included in P1 bandgap reference generation circuit
- Effect: VDDA needed to run at elevated supply for circuit to function correctly
- Root cause: Design error
- Fix: Correct opamp inserted into bandgap design
- Result: Bandgap reference in P2 worked as expected

IR Drop

- Issue: Significant current draw caused IR drop at room temperature that caused significant voltage drop at ADCs
- Effect: ADC nonlinearity at room temperature unless ADC operated at elevated supply (no problem at cold).
- Root cause: Insufficient routing metal in power/ground (PG) network
- Fix: A specialized CAD tool called Volta was used to analyze the PG network in P1 and this allowed up to add sufficient routing metal to avoid IR drop issues in P2
- Result: No IR drop issues observed in P2 (max warm IR drop of 80 mV)

IR Drop

Additional metal limited IR to 80 mV worst case at room temperature

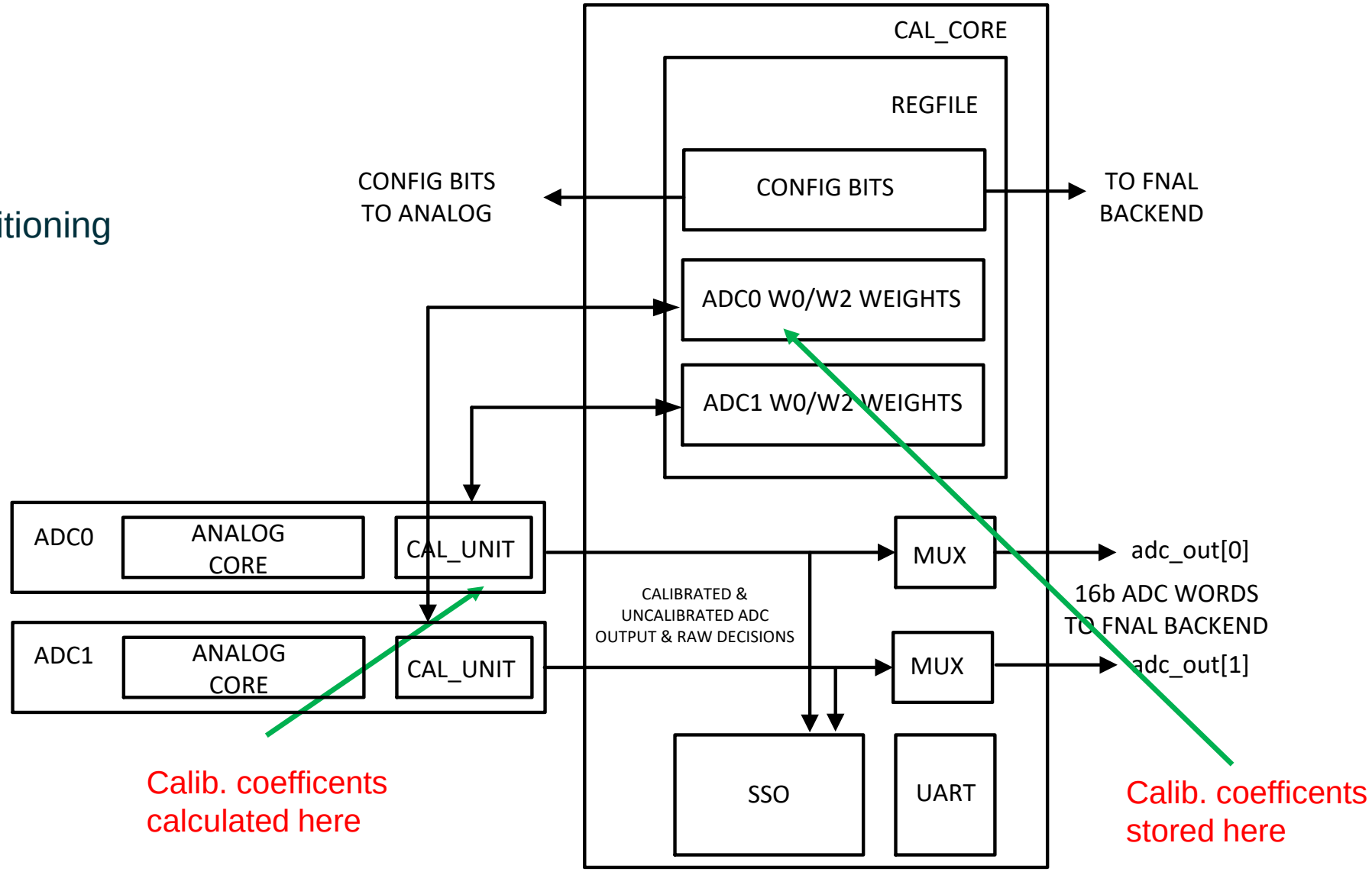


Autocalibration

- Issue: The automatic calibration function in P1 failed to operate correctly
- Effect: While evaluation of the calibration algorithm was still possible, required calculating calibration correction data off-chip and then reloading the calibration weights on chip (not suitable for fielding in practical detector)
- Root cause: Miscommunication between design teams, and separation of different functional unit in separate synthesized blocks
- Fix: Repartitioned design to use a single, monolithic digital block. Implementing more extensive verification, improved communication through use of shared documents and meetings
- Result: Autocalibration fully functional in P2 without problems

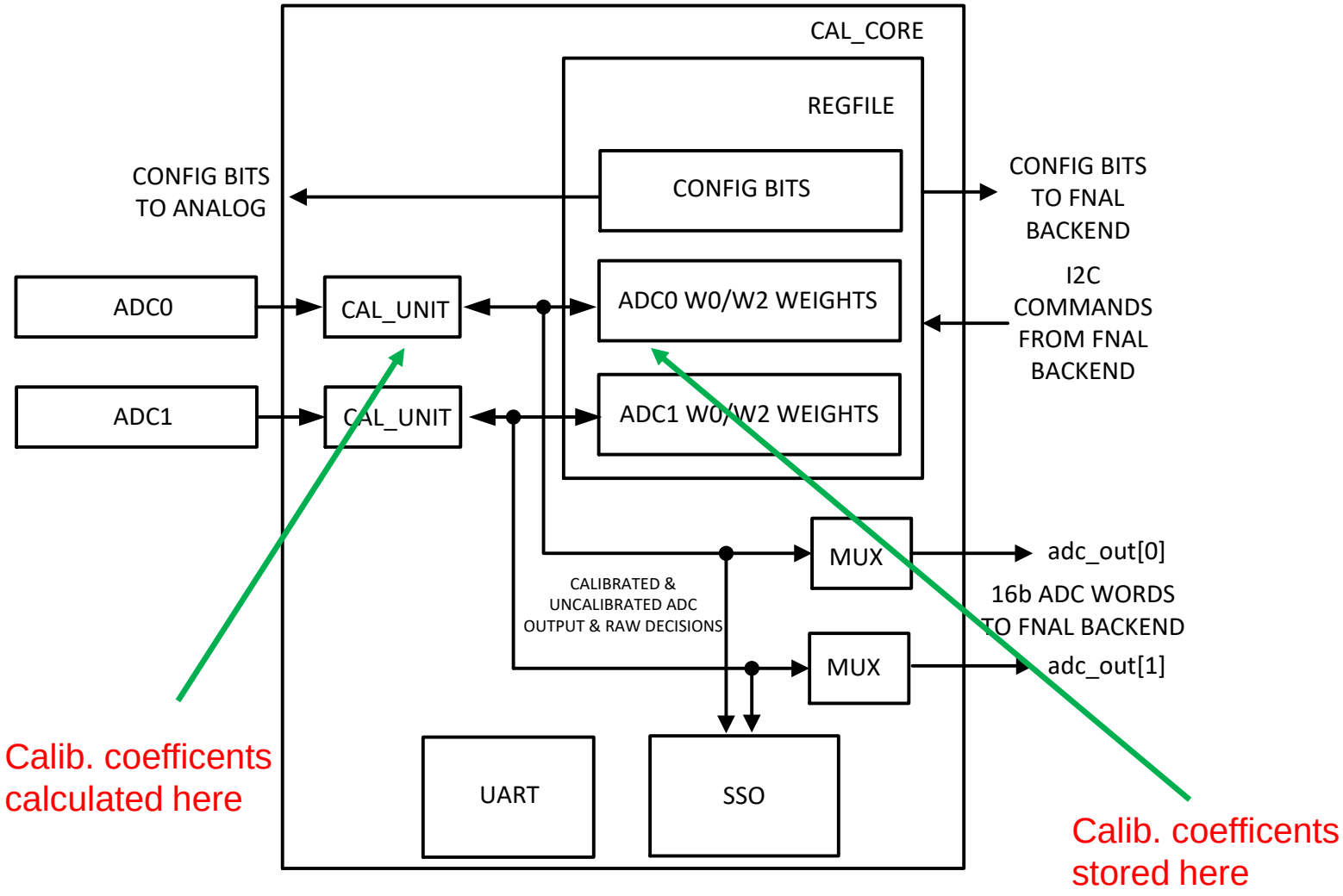
Autocalibration

P1 Partitioning



Autocalibration

P2 Partitioning

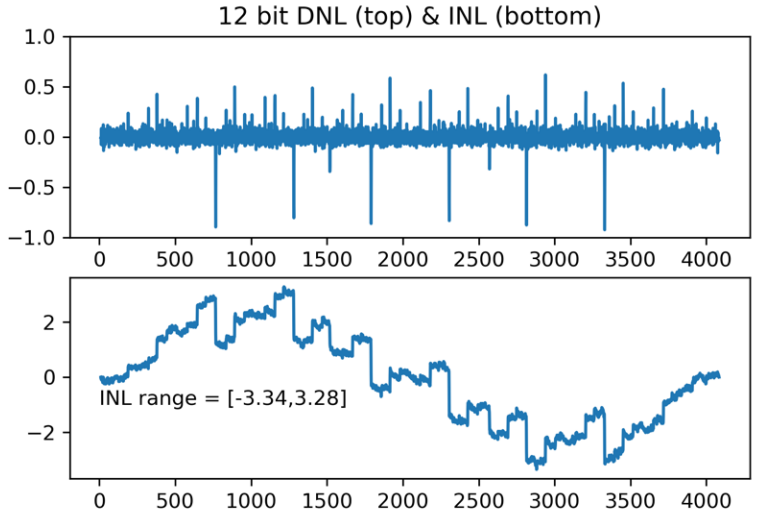


ADC Linearity

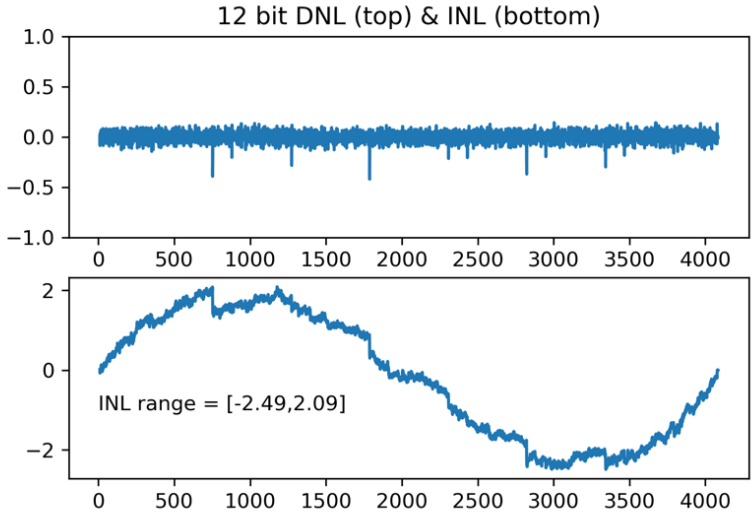
- Issue: The ADC linearity was not as good as expected (based on simulation)
- Effect: Additional nonlinearity in P1 above expectations
- Root cause: Several issues, including insufficient opamp gain and insufficient swing across corners
- Fix: Op amps were redesigned to improve swing and increase gain
- Result: Linearity was improved relative to P1. Residual nonlinearity consistent with dielectric absorption in the capacitors used to implement the ADC stages (stable correction possible)

ADC Linearity

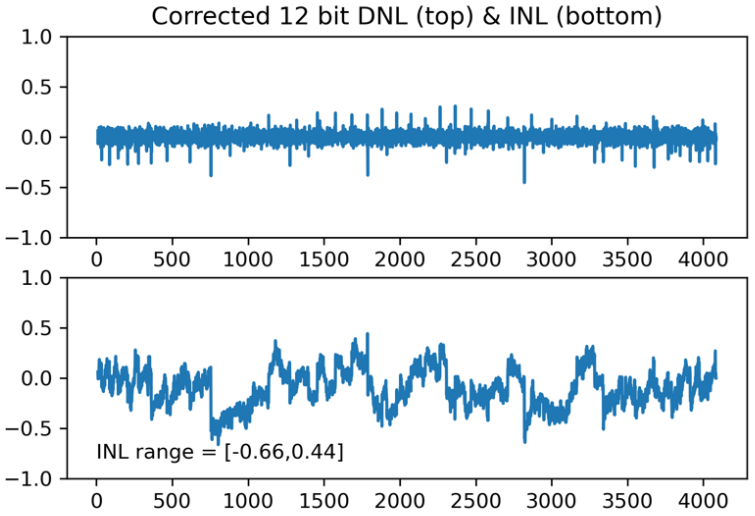
Uncalibrated



Autocalibrated



Correction Applied

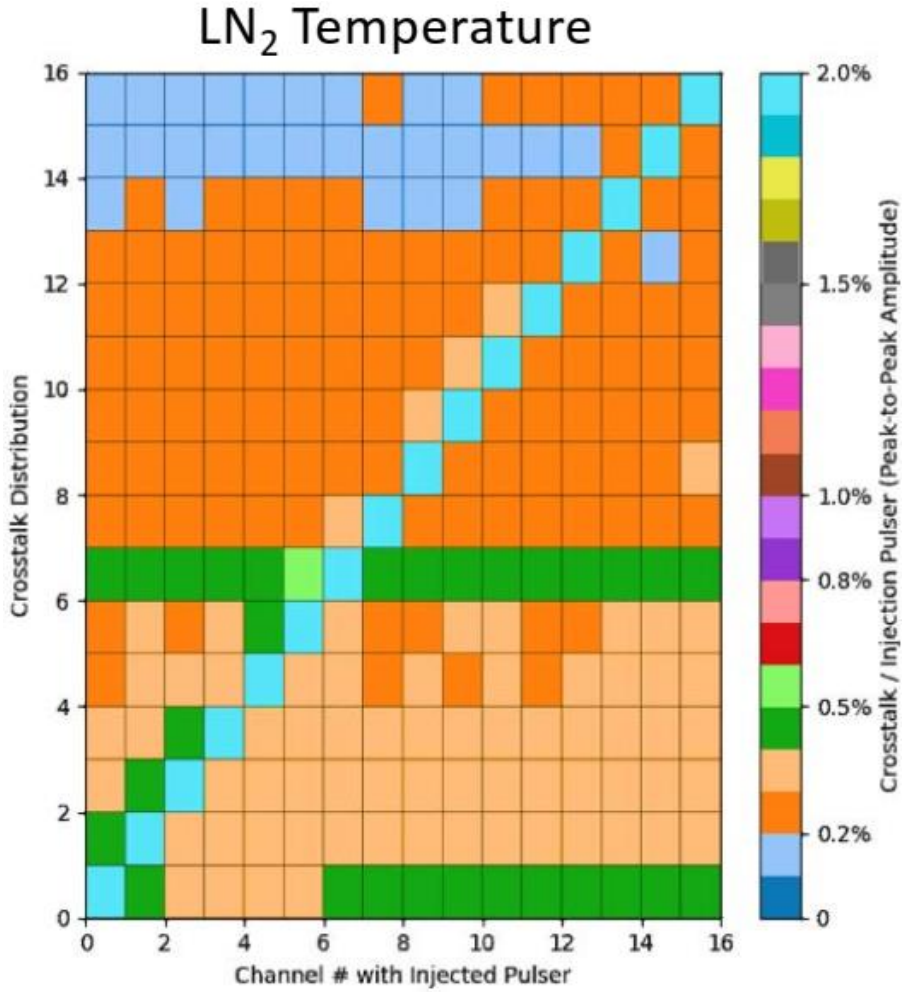


X-axis: ADC code
Y-axis: nonlinearity in LSBs (12 bit)

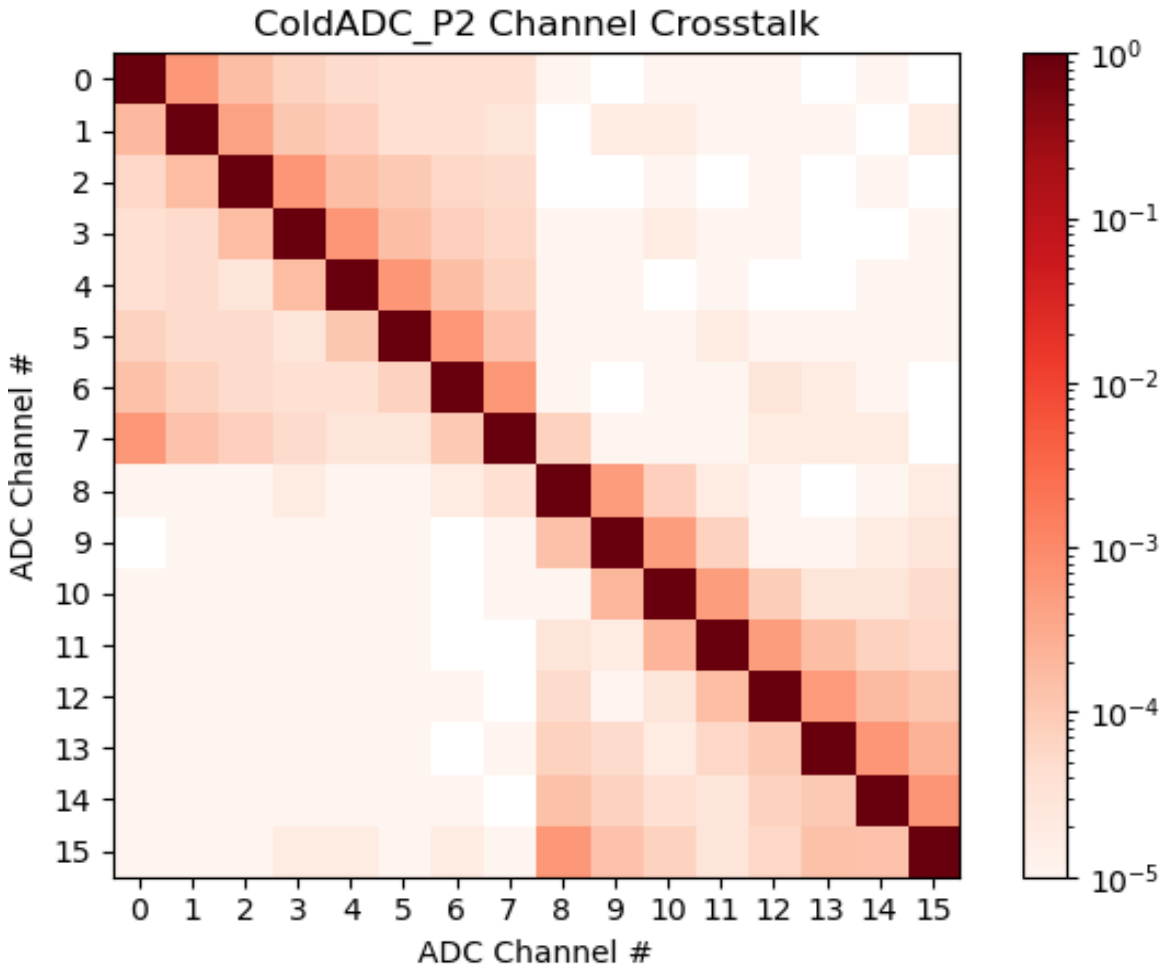
ADC Crosstalk

- Issue: While not critical, there was evidence of a low level of crosstalk (~0.5%) between channels.
- Effect: Limited performance of some channels
- Root cause: Insufficient bandwidth in the mux (too high on-resistance in switches) leading to kickback and mutual capacitive coupling between channels
- Fix: Improve BW to mitigate memory effect (kickback) and reduce channel-to-channel coupling via layout optimization
- Result: Crosstalk improved to 0.06% (almost order-of-magnitude improvement)

ADC Crosstalk



P1 Crosstalk (0.5% worst case)



P2 Crosstalk (0.06% worst case)

Digital Overflow

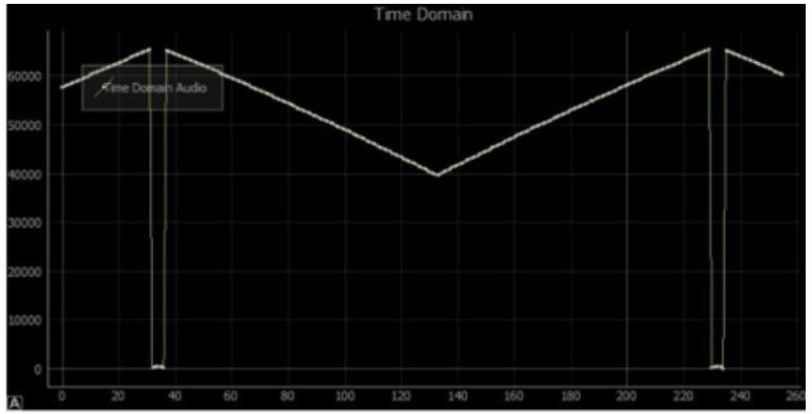
- Issue: If the sum of all ADC stages gains > 2^{15}, overflow (or underflow) possible
- Effect: Overflow observed in testing of P1
- Root cause: Capacitor mismatch can cause some ADC stages to have gain > 2.
- Fix: Implement digital overflow monitor to detect overflow condition and pin the ADC output to appropriate value
- Result: Overflow monitor demonstrated to work as expected

Digital Overflow

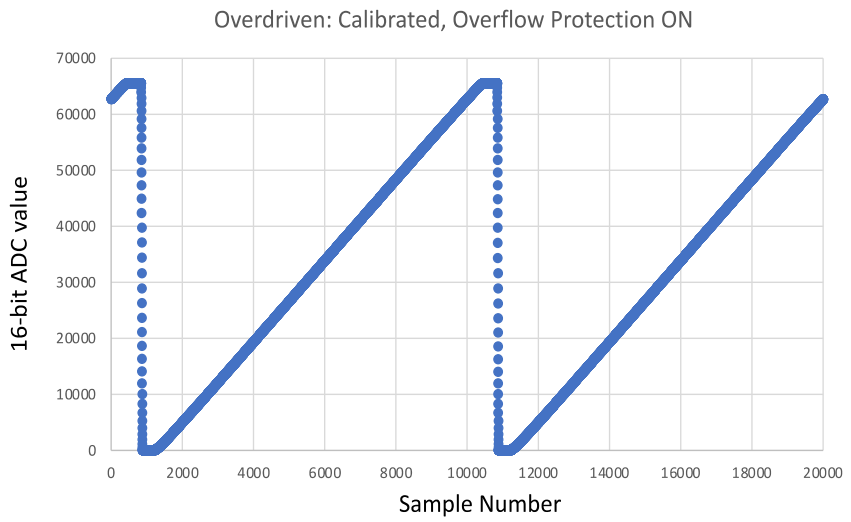
P1

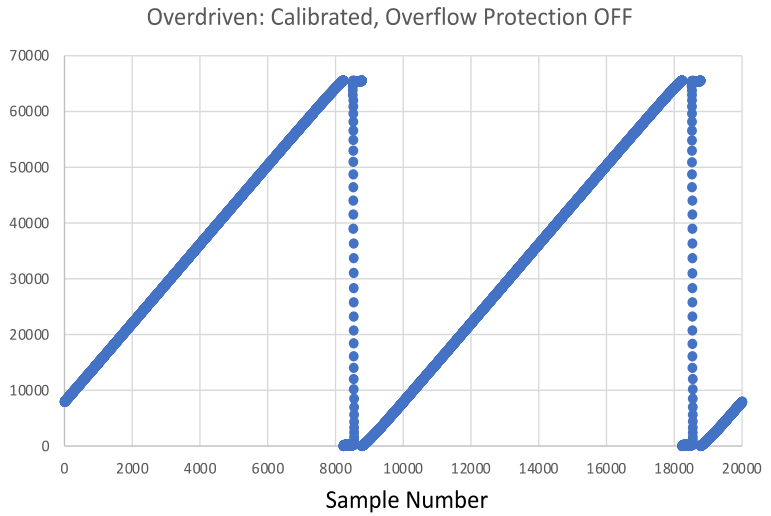
ADC Without Overflow

ADC With Overflow



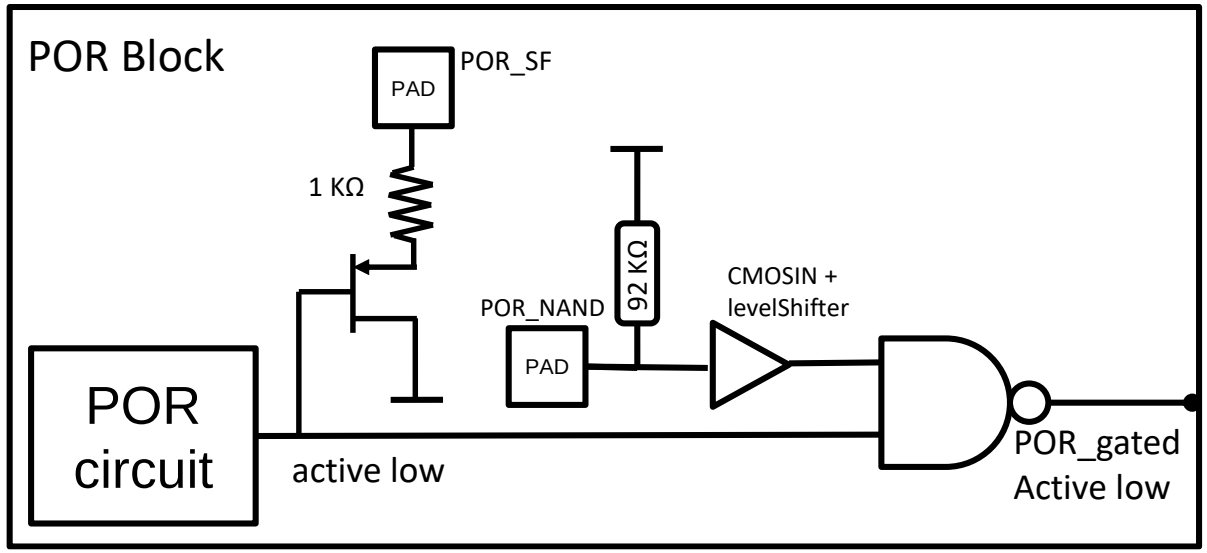
P2



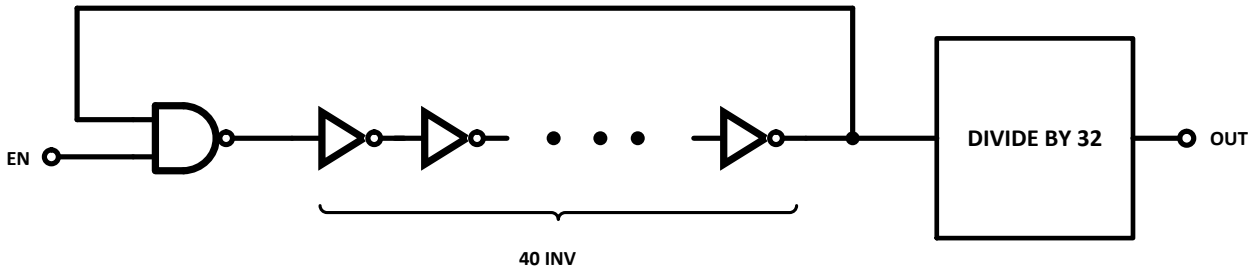


New Functionality added to P2

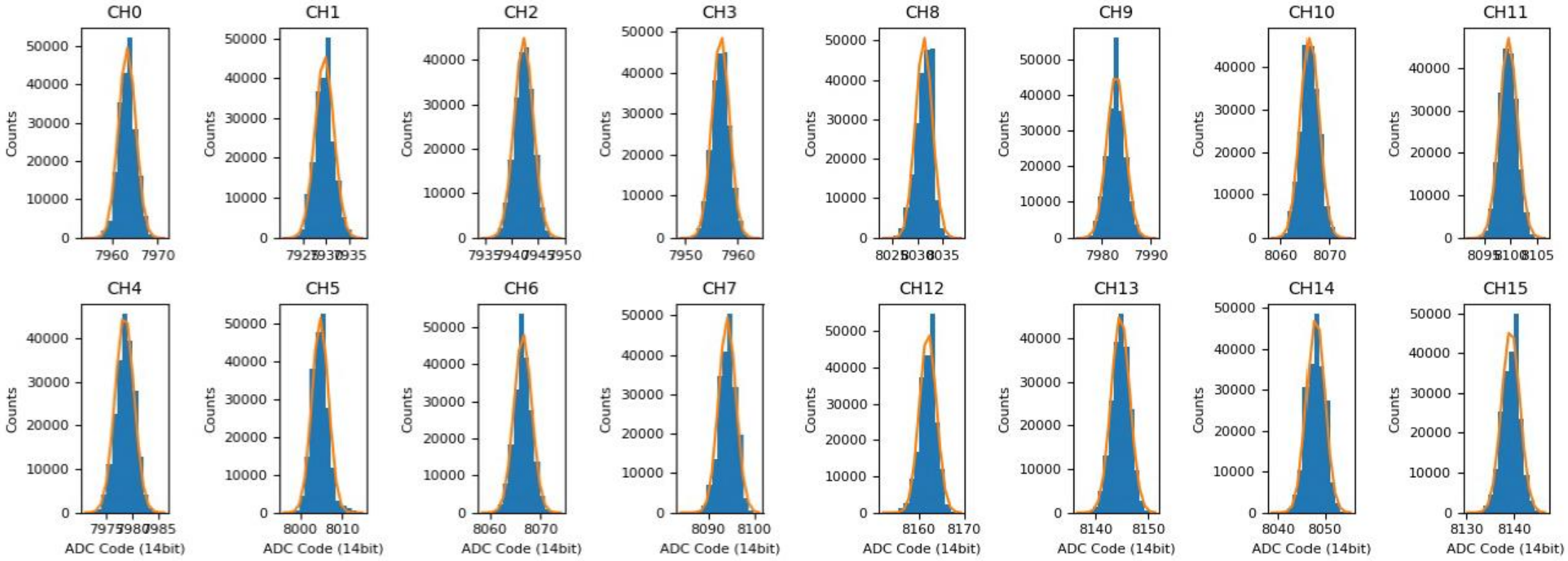
Power On Reset Circuit



Process Monitor Circuit

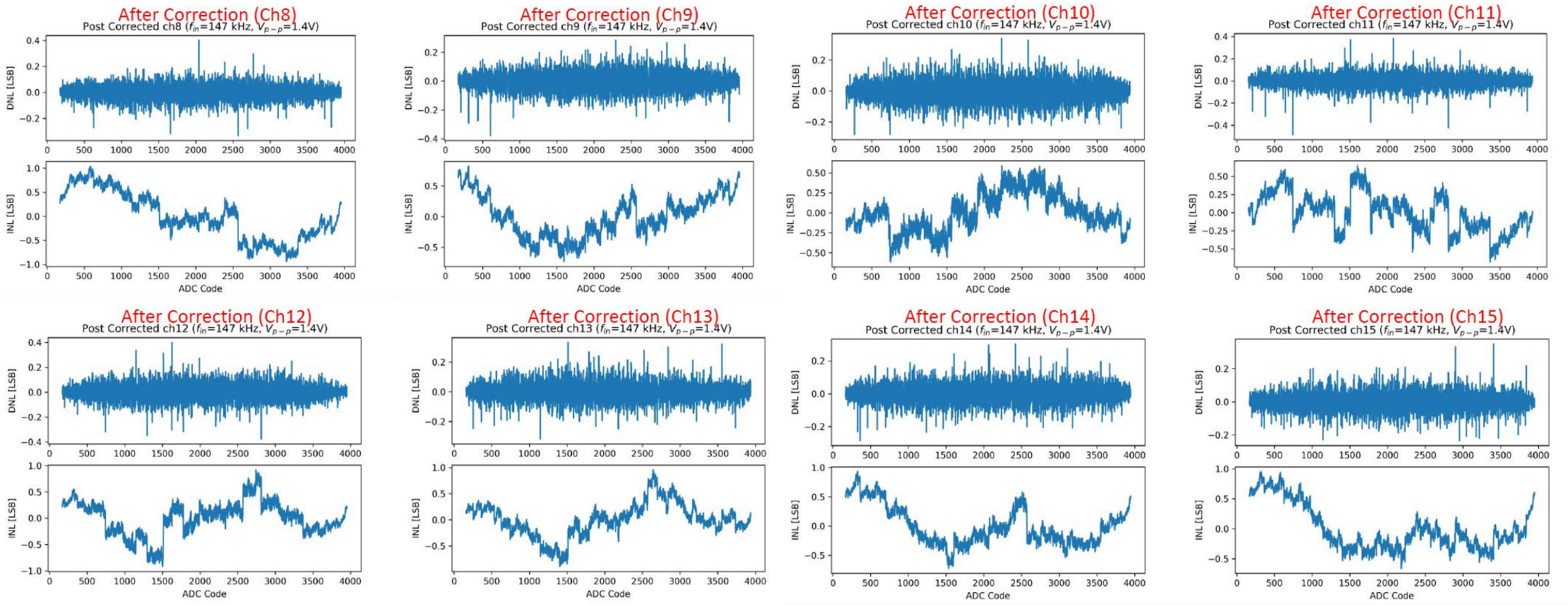


Noise Across Channels

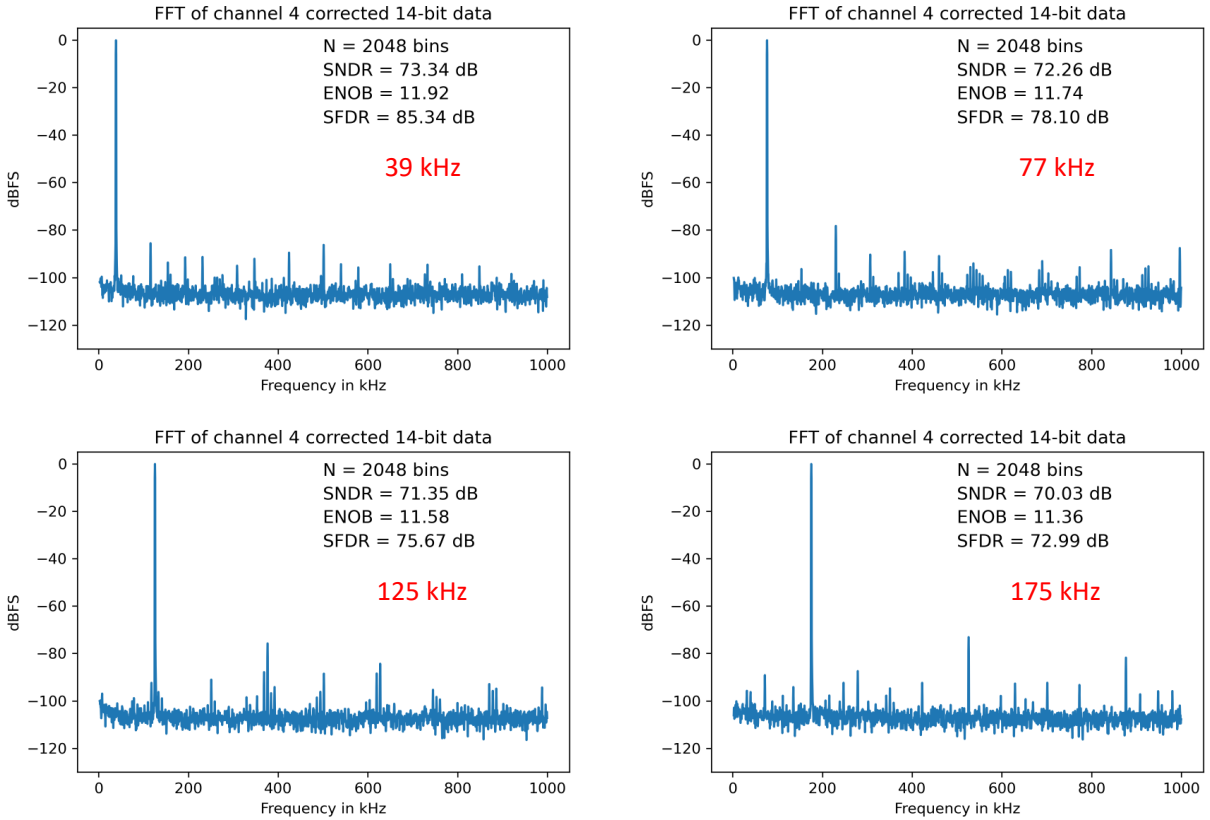


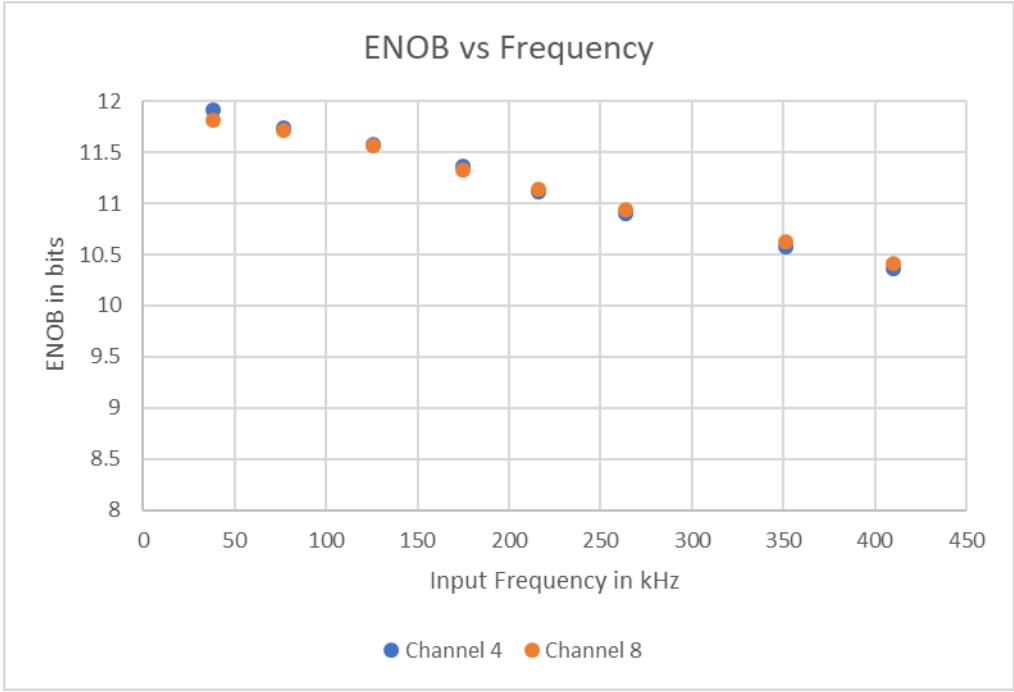
Highly stable noise characteristic → about 140 μV-rms at LN_2

Linearity Across Channels



Dynamic Linearity Across Channels





410 kHz is LArASIC BW when configured in 0.5 µs shaping mode

ColdADC QC & Lifetime (early data)

QC:

- P1 – ~100 chips at LN_2. 1 failure. (short between pins).
- P2 – 12 chips tested at LN_2. 0 failures.

Measurements are consistent with an approximately 95% or better yield

Lifetime (just starting):

Currently have P2 chip under stress: 10 days at 4.4 V (room temp) and 10 hours at 4.4 V immersed in LN_2. No visible degradation of the chip performance.

Performance Summary

Specification	Value	Result	Note
Operating Temperature	Room Temperature and 88K	Success	
Sampling Rate	~2 MHz (62.5 MHz/32)	Success	
Noise	200 µV rms	168/140 µV rms 236/205 µV rms	Single Ended/Differential input At LN_2 temp at Room Temp
Differential Nonlinearity (DNL)	± 0.5 LSB (12-bit)	Success	At LN_2, typical values
Integral Nonlinearity (INL)	± 1 LSB (12-bit)	Success	At LN_2, typical values after correction
Effective Number of Bits (ENOB)	≥10.3 for frequency ≤410 kHz (at LN_2)	Success	At LN_2.
No Missing Codes	N/A	Success	At LN_2 and RT
Crosstalk	< 1% (goal = 0.1%)	0.1%/0.06%	Single Ended/Differential input At LN_2 temp

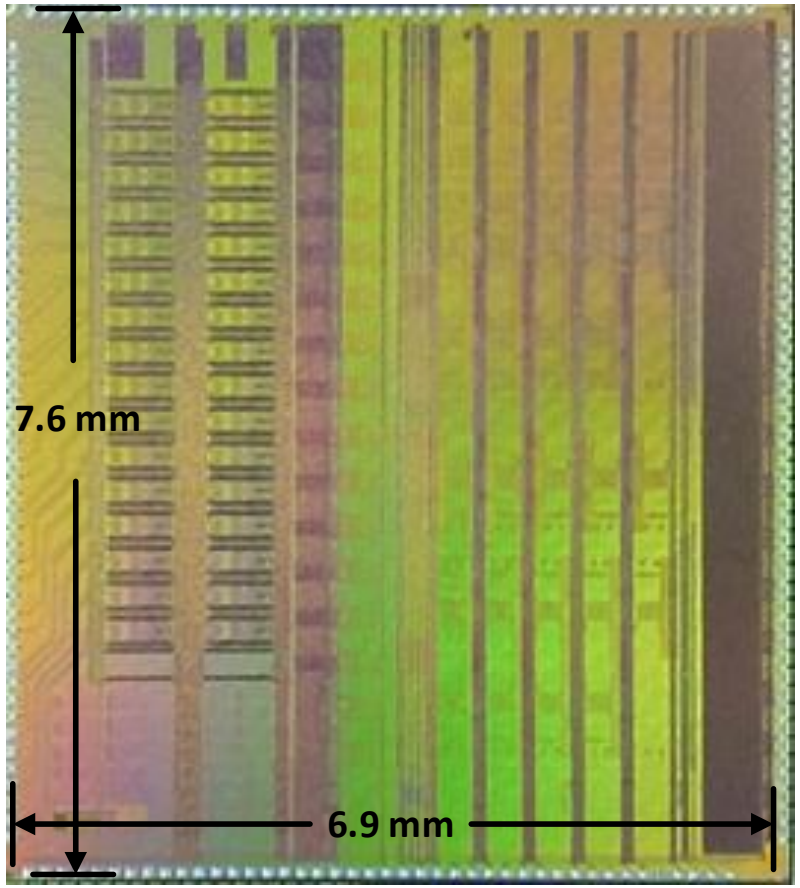
Response to Charge Questions for ColdADC (3b)

- Are the issues with the autocalibration and with the kickback from the pipeline to the sample and hold amplifier understood and fixed? **YES**
- Are all the other problems with the first prototype understood and fixed? **YES**
- What yield has been observed in testing all the prototype ASICs? **The yield is very high, likely greater than 95%. (1 failure in ~110 devices tested)**
- Is there any understanding of the different types of failures? **Only one failure observed and it was understood (electrical short between two pins)**

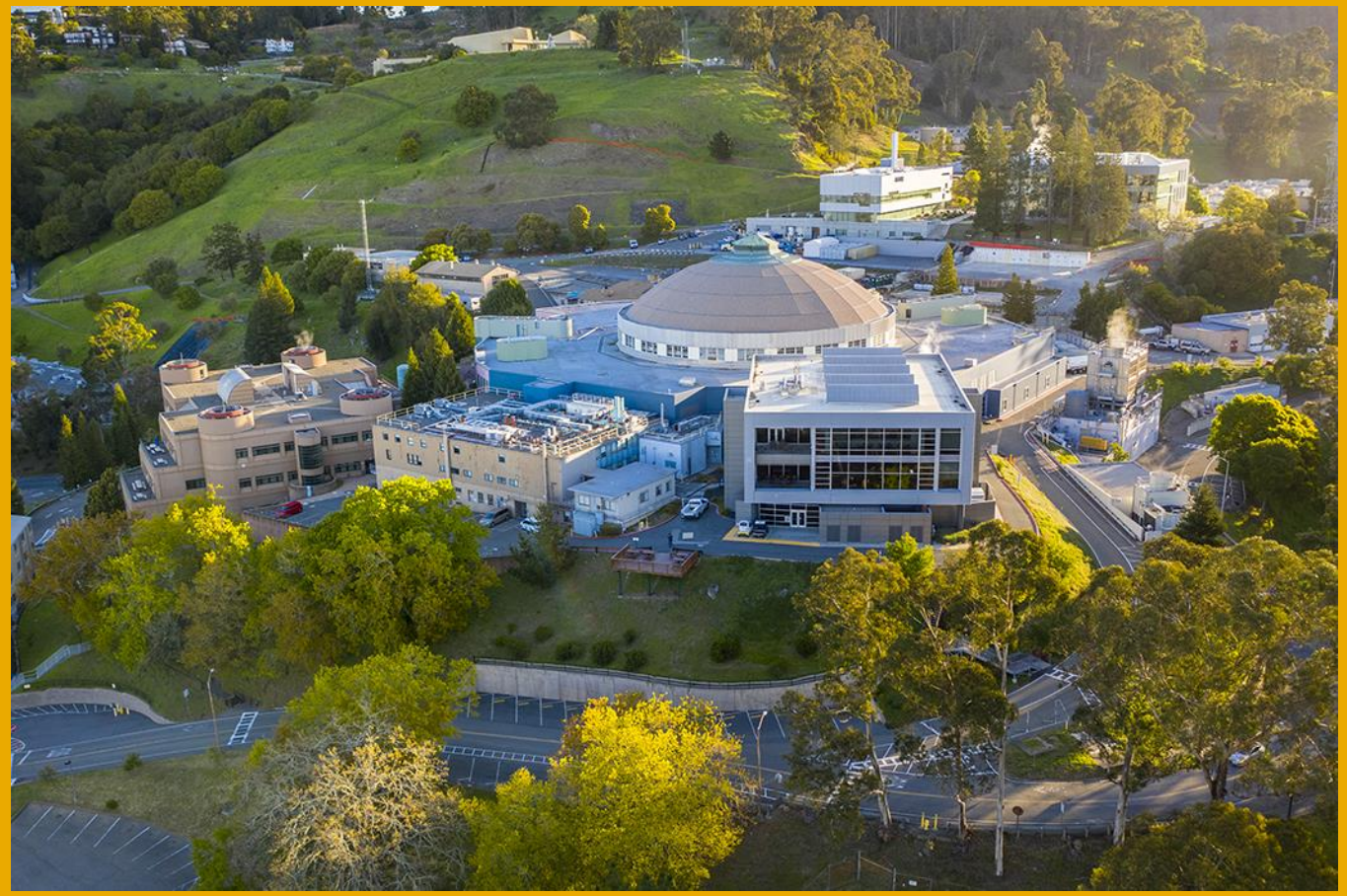
Conclusion

- A number of issues were identified with ColdADC_P1 during testing
- The most serious issues were a missing logic level shifter and the autocalibration failure
- Neither problem precluded full evaluation of the P1 chip, but needed to be addressed for a fieldable ASIC
- All fixes worked as expected and ColdADC_P2 meets requirements

ColdADC_P2



Thank You



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