COLDATA_P3 Testing

David Christian

Xiaoran Wang

Scott Holm

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Summary

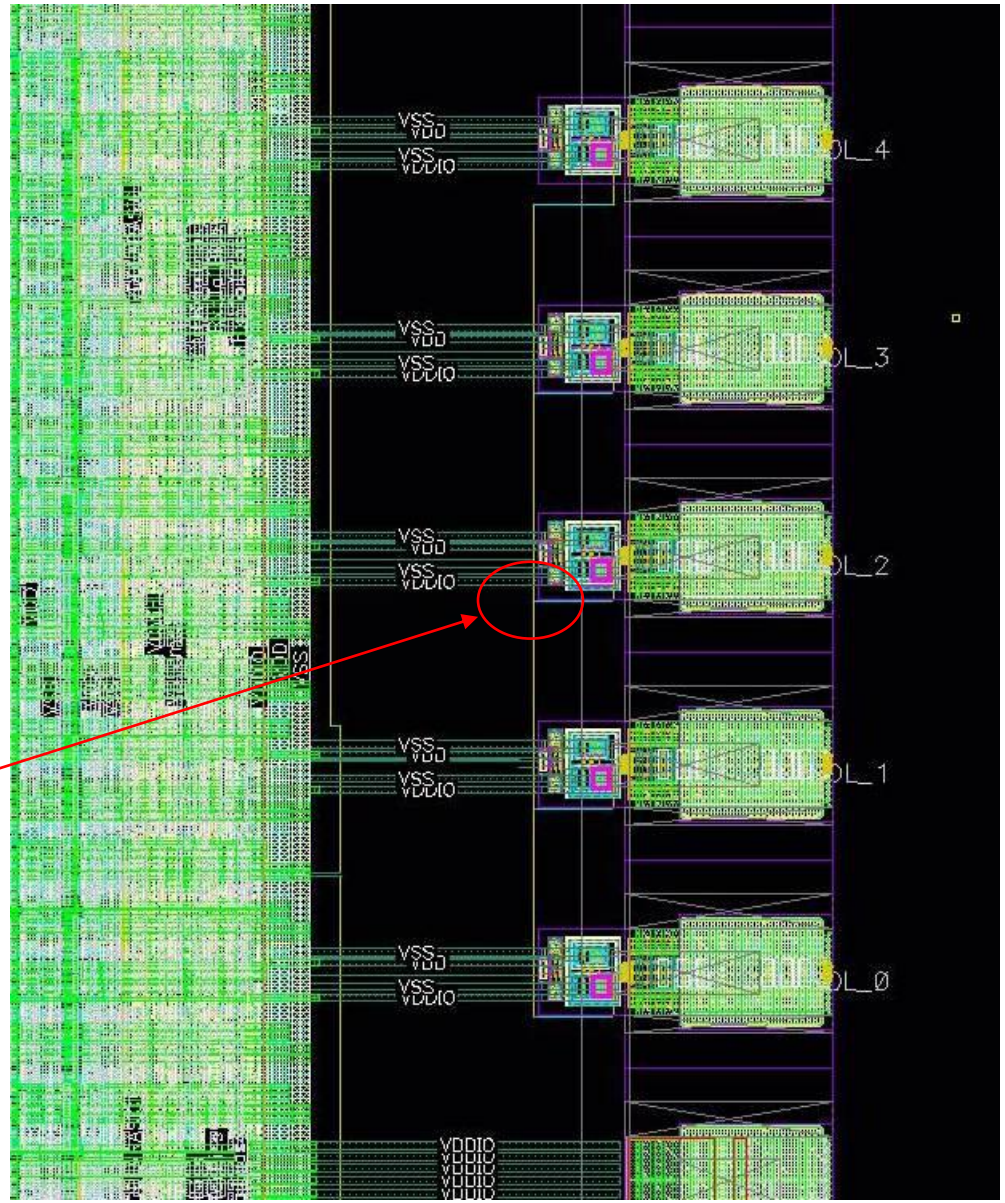
- The PLL is now referenced to the 62.5 MHz clock from the WIB and now locks at room temperature as well as at cryogenic temperature at the nominal bias voltage of 1.1V.
- The I2C relay bug has been eliminated.
- All control registers are initialized as intended and can be read/written.
- The timestamp now counts 16 ns ticks and has been extended to 15 bits.
- The registers used to control the time between LArASIC charge inject pulse edges are now 16-bit registers.
- The WIB echo-back feature designed to enable cable-length measurement works as designed.
- eFuse register readback has been simplified.
- All LArASIC and COLDADC control functions operate as intended.
- All FAST commands operate as intended.
- Two minor bugs have been discovered.

Modifications to Output Frame Formats

- The “Frame-15” format included in COLDATA_P2 has been eliminated.
  - This format was included as a COLDADC debugging option and was never used.
- The control symbols used for the data formats have modified slightly.
  - All frame types now begin with a 16-bit header starting with K.28.1 and are padded to 64 bytes long with K.28.5 comma characters.
  - This requires a minor WIB microcode change.
  - COLDATA_P3 is being read out successfully at BNL in tests of 3-ASIC FEMBs.

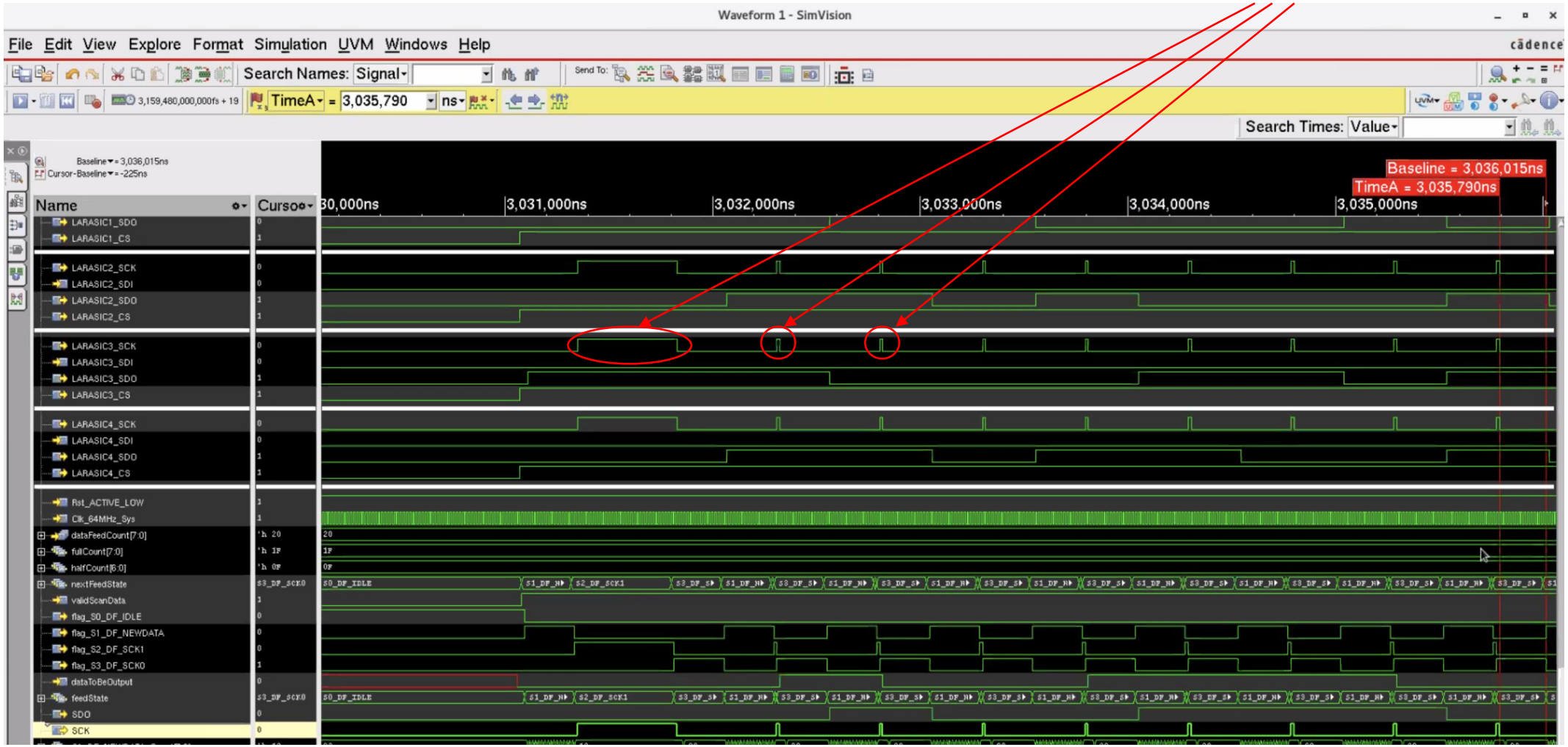
Bug#1: FEMB control bits

- The output drivers & pads for the control bits include the possibility of pulling the pad up to Vdd or down to ground.
- We did not intend to implement either a pull up or a pull down.
- An error in the RTL resulted in all 5 pads being shorted together through the PULL_UP_DOWN nodes.
- Trivial fix for COLDATA_P4.



Bug #2: SPI clock error

Clocks after the first are high for only 16 ns



Simulation

LArASIC SPI Clock Error

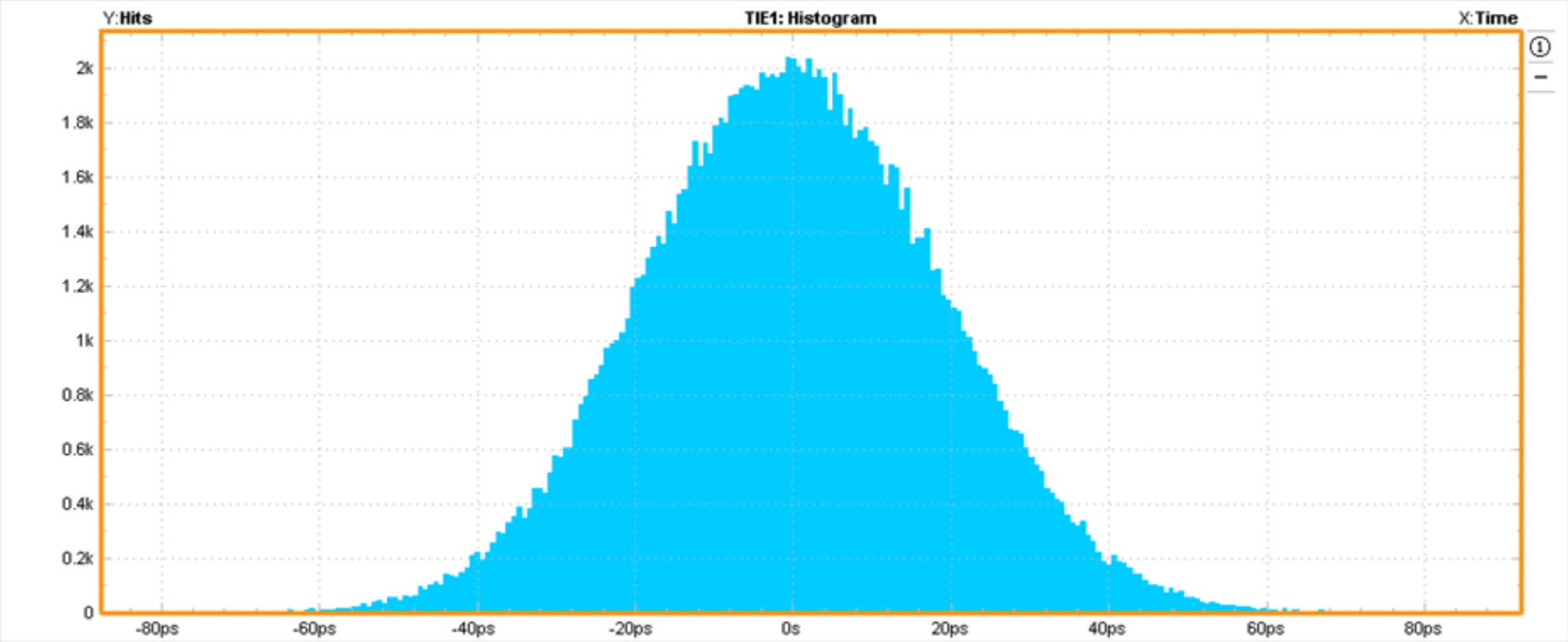
- Tests at BNL demonstrate that LArASIC can be programmed even if the SPI clock is high for only 10 ns.
- Nonetheless, the RTL has been modified and COLDATA_P4 will provide 50% duty factor SPI clocks.

PLL locking tests

- The PLL in chips tested locks at room temperature with a bias voltage of at least 1.0V (1.1V is nominal)
- At 77K, the PLL locks even with a bias voltage of 0.95V.

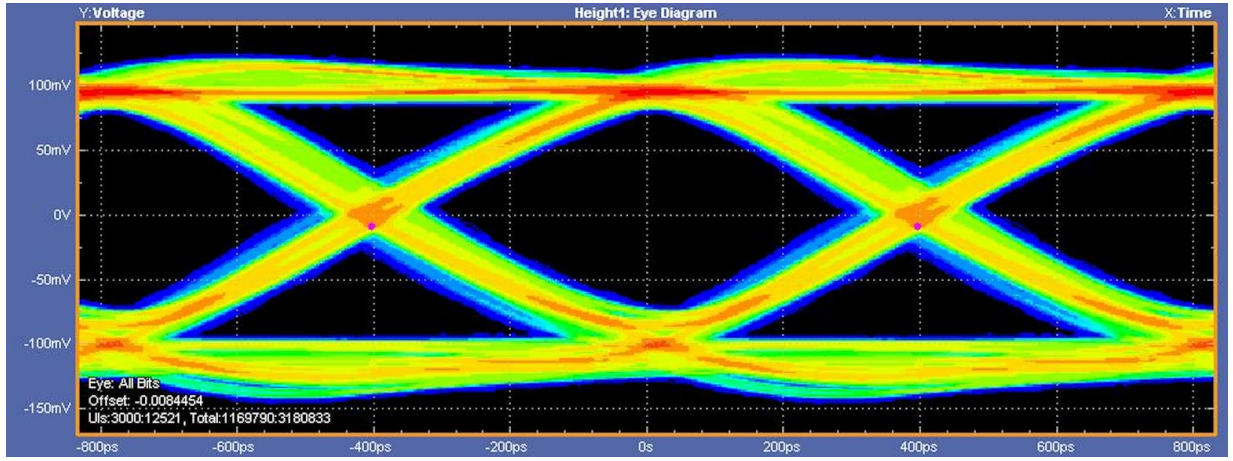
Performance Tests: ADC sample clock jitter

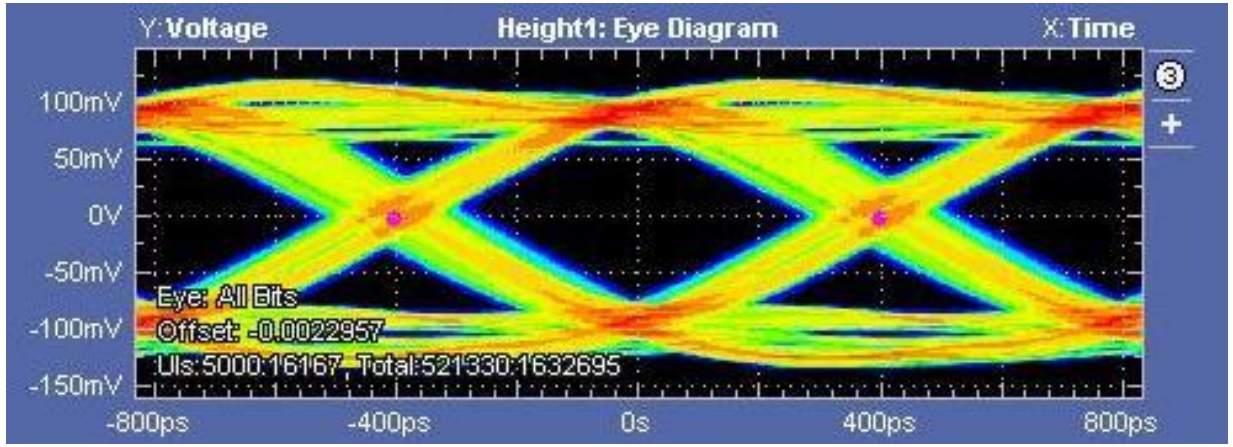
- Specification is less than 180 ps rms.
- “2 MHz” clock edge jitter measured at room temp is 18.7 ps.
- Similar or better performance is expected at cryogenic temperature



Performance Tests: 1.25 Gbps links

- Specification: Need to drive 23m cables for FD1; slightly longer for FD2.
- PRBS7 eye measured at room temperature with a 25 m long Samtec twinax cable has an open height of ~150 mV.
- PRBS7 eye measured at room temperature with a 35 m long twinax has an open height of >100 mV.





Performance Tests: 1.25 Gbps links

- Brute force bit error rate measurement:
- PRBS7 output from COLDATA_P3 to 25 m long Samtec twinax to Xilinx KC705 evaluation board.
  - Ran for ~ 8.5 days (9.4E14 bits received) with no error.

COLDATA_P4

- COLDATA_P4 is currently in the final stages of layout and verification and will be ready for tape-out by August 6.
- We are confident that our verification procedure is robust enough to allow us to implement the two minor RTL modifications in an engineering run.

Charge Question 3C

- Are there any issues?
  - *Two minor bugs will be resolved in COLDATA_P4.*
- Does the chip still require two clocks?
  - *No; all clocks are now derived from the 62.5 MHz master clock.*
- Are bit error rate measurements available?
  - *A BER measurement was presented for a 25m long warm cable and PRBS7 eye diagrams were presented for 25m and 35m long warm cables.*
- Is an equalizer chip required on the WIB?
  - *No.*
- Are all synchronization issues understood?
  - *Yes (Integration with timing system was demonstrated in ICEBERG).*
- What level of synchronization can be achieved?
  - *Much better than 16ns; this will depend on how precisely the cable delay is measured by the WIB.*