DUNE FDR: TPC Electronics ASIC

Measurements of LArASIC Performance

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Content

- **LArASIC Requirements and Specifications**
- Measurements to Confirm Design Changes
- Full Chain Measurements
- System Tests
- Summary

LArASIC Requirements and Specifications

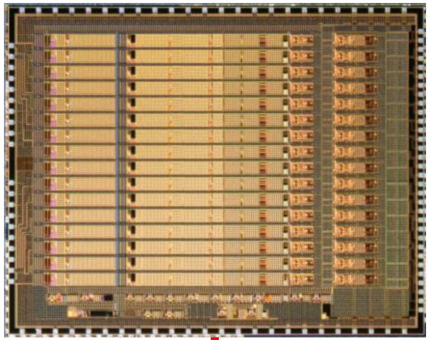
- https://edms.cern.ch/document/2397298/1
- System noise < 1000 e^- [SP-FD-2]
- FE peaking time adjustable from 1 to 3 μs [SP-FD-13]
- Signal saturation level ~500,000 e^- (80 fC) [SP-FD-14]
  - **Gain of the front-end amplifier ~ 10 mV/fC [SP-ELEC-2, 2284]**
- Dead channels < 1% [SP-FD-28]
- Cold electronics power consumption < 50 mW/channel [SP-FD-21]
- Two baselines in the front-end amplifier [SP-ELEC-1, 2283]
- Input capacitance to front-end ASIC should be optimized for 120 to 210 pF [SP-ELEC-12]
- Channel-to-channel crosstalk < 1% (goal of < 0.1%) [SP-ELEC-11]
- Monotonic saturation recovery [SP-ELEC-10]

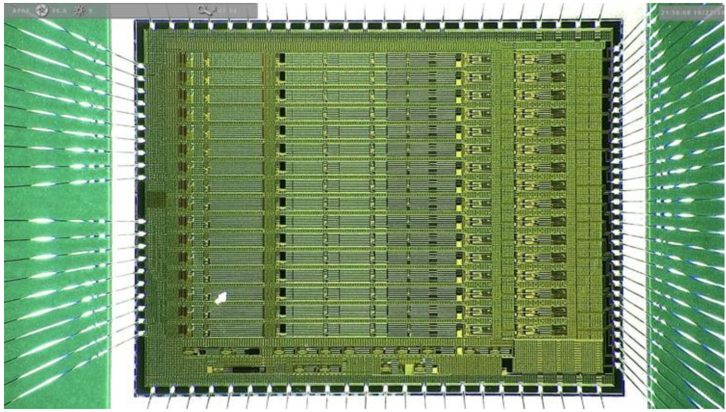
LArASIC Developments

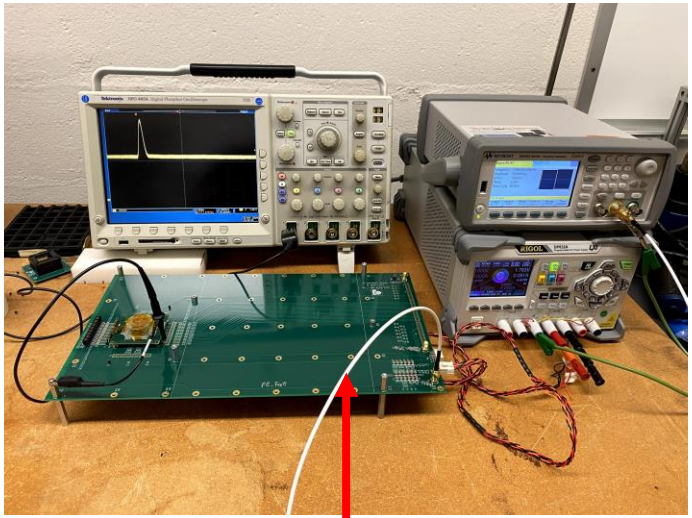
- Goal of P4 LArASIC
  - Eliminate the ledge effect shown on P2 LArASIC in ProtoDUNE operation (Success)
  - Fix the bandgap cold startup issue to improve cold yield (Success)
  - Add Single-Ended to Differential Converter (SEDC) for differential interface to ColdADC (High current draw with SEDC)
  - Improve uniformity of output DC baseline by introducing 16x RQI (reset quiescent current) subtraction in the second stage (CA2n) of the charge amplifier (Random non-operational channels observed in LN2)
- Goal of P5 LArASIC
  - Remove RQI subtraction to fix a few non-operational channels in LN2 (Success)
  - Modify SEDC buffer for stable and low noise operation (Success)
  - Modify Test Charge Injection Pulser DAC in terms of its linearity (Success)
  - Retain improvements achieved in P4 (ledge effect elimination, bandgap cold startup) (Success)
- Goal of P5A LArASIC
  - Explore different ESD protection schemes (Success)
  - Further investigate the RQI subtraction issue (Success, issue located)
- Goal of P5B LArASIC
  - Apply ESD scheme with higher discharge tolerance (Engineering run)

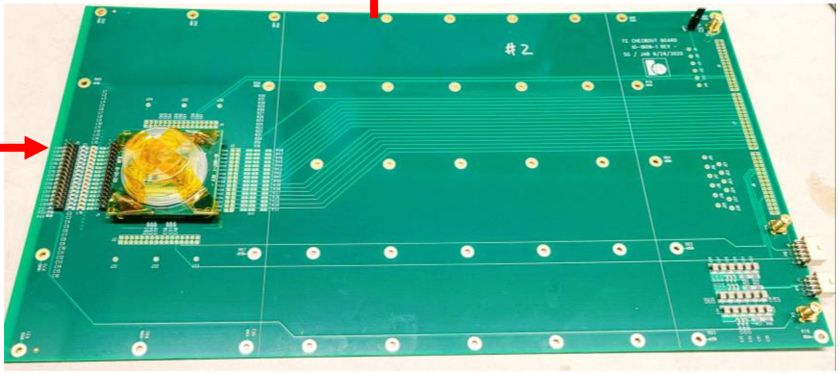
Measurements of P4 LArASIC (1)

- LArASIC checkout test setup



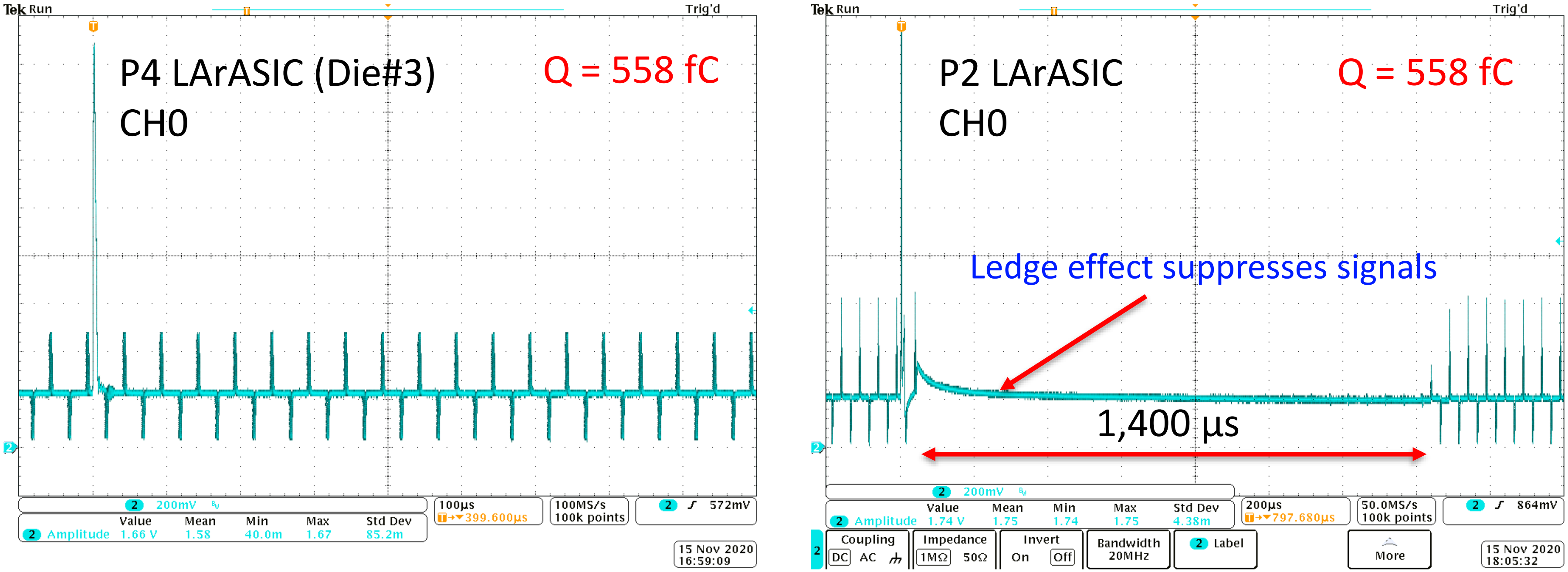






Measurements of P4 LArASIC (2)

P4 LArASIC: Eliminate the ledge effect (Success)



	Value	Mean	Min	Max	Std Dev
2 Amplitude	1.66 V	1.58	40.0m	1.67	85.2m

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	Value	Mean	Min	Max	Std Dev
2 Amplitude	1.74 V	1.75	1.74	1.75	4.38m

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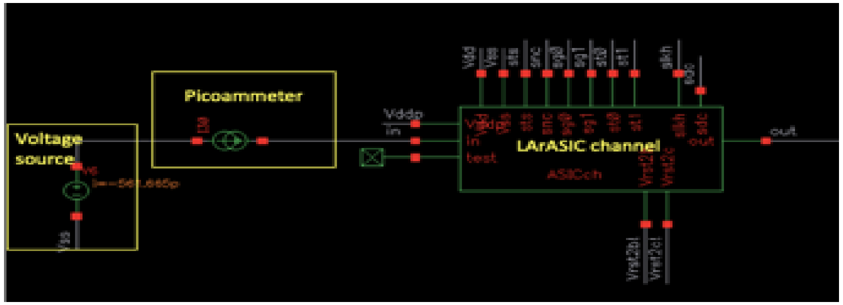
LN2, 200 mV BL, 14 mV/fC gain, 1.0 µs t_p, 500 pA I_{RQI}

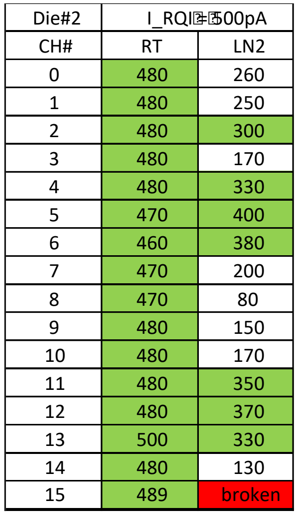
- No ledge effect is observed with P4 LArASIC even injected charged > 2pC
  - Large charge pulser is injected through LArASIC input directly
  - ASIC internal calibration pulser is enabled as well to monitor ledge effect

Measurements of P4 LArASIC (3)

- **No BGR startup issue is observed at LN2** (Success)
  - 10 dies, 30+ packaged chips
- Baseline measurements of P4 LArASIC at LN2
  - 900 mV BL setting: 915 ± 10.1 mV (vs. P3 900 mV BL setting: 898.9 ± 12.9 mV)
  - 200 mV BL setting: 216 ± 7.6 mV (vs. P3 200 mV BL setting: 243.8 ± 16.0 mV)
  - A few non-operational channels observed in LN2
    - The large variation of RQI at LN2 may cause the 16x RQI subtraction in the second stage (CA2n) of the charge amplifier to become larger than available current in the circuit, so the preamplifier is disabled
- The large variation of RQI at LN2 temperature unfortunately cannot be simulated with available models



A SMU (source measure unit) is used to measure the RQI of the input channel. channel. When $V_{in} > V_{th}$, the feedback network of the first stage (CA1) of the charge amplifier is switched off, RQI is measured with the picoammeter.



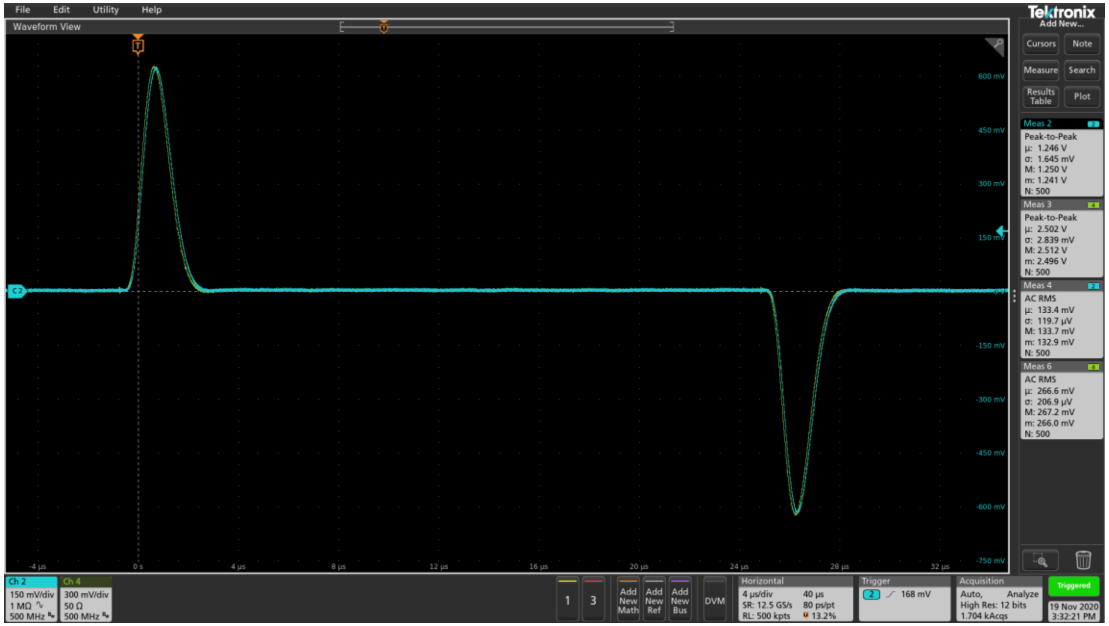
Die#2	I_RQI ±500pA	
CH#	RT	LN2
0	480	260
1	480	250
2	480	300
3	480	170
4	480	330
5	470	400
6	460	380
7	470	200
8	470	80
9	480	150
10	480	170
11	480	350
12	480	370
13	500	330
14	480	130
15	489	broken

Green: channel alive
Broken: channel damaged
Empty: channel non-operational

RT	479 ± 8 pA
LN2	276 ± 97 pA

Measurements of P4 LArASIC (4)

High Current Draw with SEDC (Fixed in P5)



Meas 2 (2)
Peak-to-Peak
µ: 1.246 V
σ: 1.645 mV
M: 1.250 V
m: 1.241 V
N: 500

Meas 3 (4)
Peak-to-Peak
µ: 2.502 V
σ: 2.839 mV
M: 2.512 V
m: 2.496 V
N: 500

Meas 4 (2)
AC RMS
µ: 133.4 mV
σ: 119.7 µV
M: 133.7 mV
m: 132.9 mV
N: 500

Meas 6 (4)
AC RMS
µ: 266.6 mV
σ: 206.9 µV
M: 267.2 mV
m: 266.0 mV
N: 500

Ch 2: 150 mV/div, 1 MΩ, 500 MHz
Ch 4: 300 mV/div, 50 Ω, 500 MHz
Horizontal: 4 µs/div, 40 µs, SR: 12.5 GS/s, 80 ps/pt, RL: 500 kpts, 13.2%
Trigger: 2, 168 mV
Acquisition: Auto, Analyze, High Res: 12 bits, 1.704 kAcqs
19 Nov 2020
3:32:21 PM

Oscilloscope measurements of P4 LArASIC differential output with SEDC buffer turned on. Blue trace of oscilloscope channel 2 has 150 mV/div, is the measurement of single ended output OutP from the analog monitoring pin. Green trace of oscilloscope channel 4 has 300 mV/div, is the measurement of differential output with a differential probe.

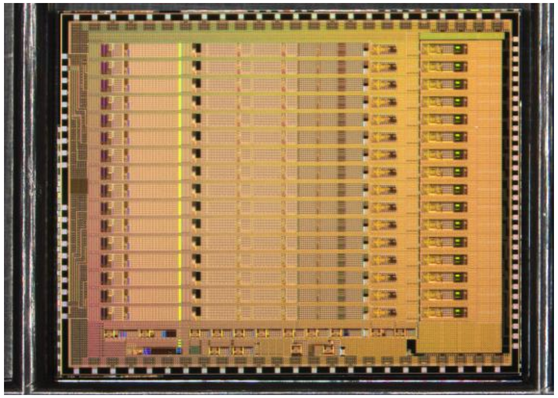
Issue observed: The P4 LArASIC with SEDC turned on consumes a large power of ~16 mW/ch instead of ~12 mW/ch due to insufficient phase margin.

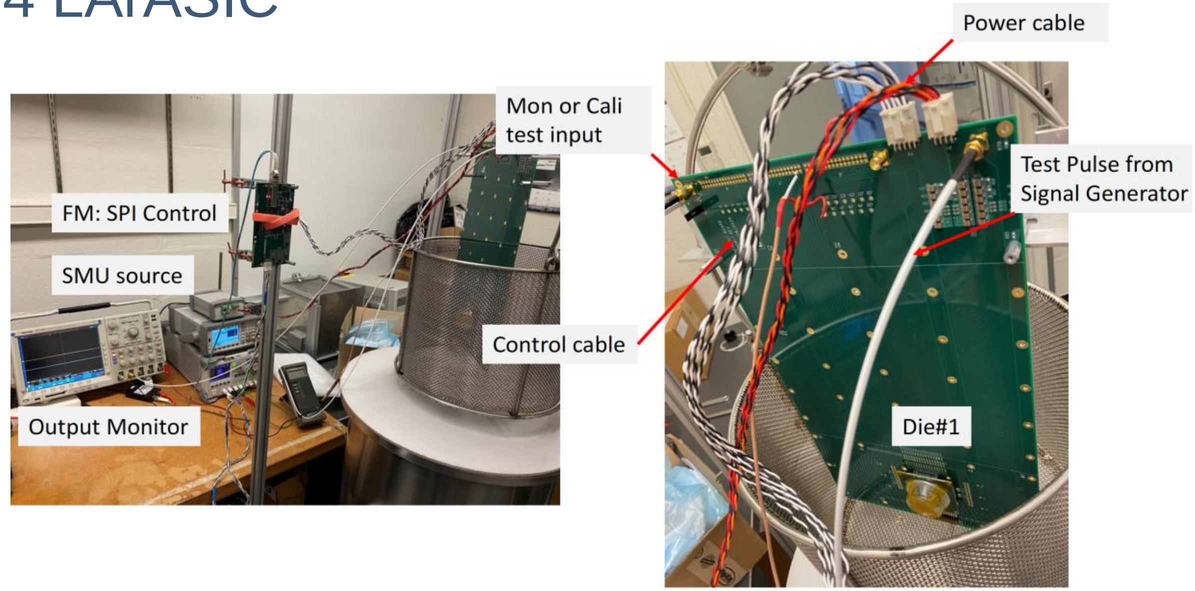
→ The lab test shows this could be mitigated by adding decoupling capacitors and using a reduced VDDO power rail.

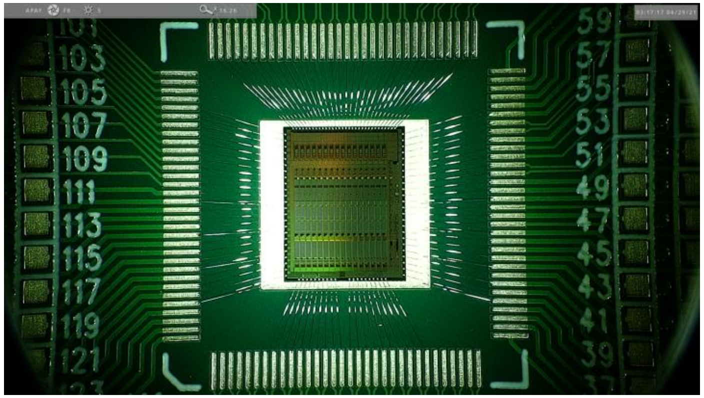
→ The problem was reproduced in simulation by adding a few Ω resistors on VDDO (buffer power) and VSSO (buffer ground).

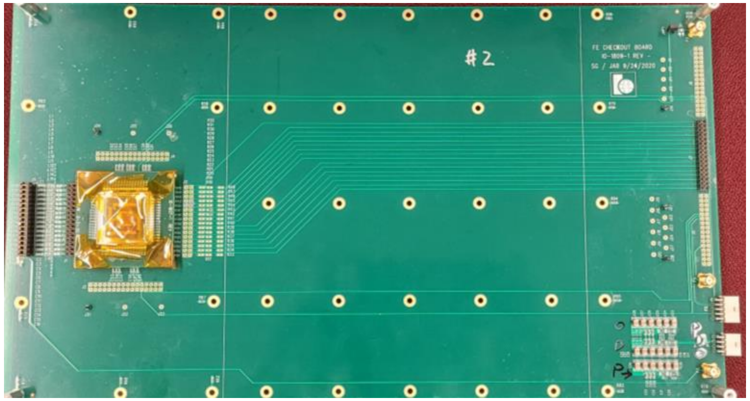
Measurements of P5 LArASIC (1)

- Same test setup as P4 LArASIC







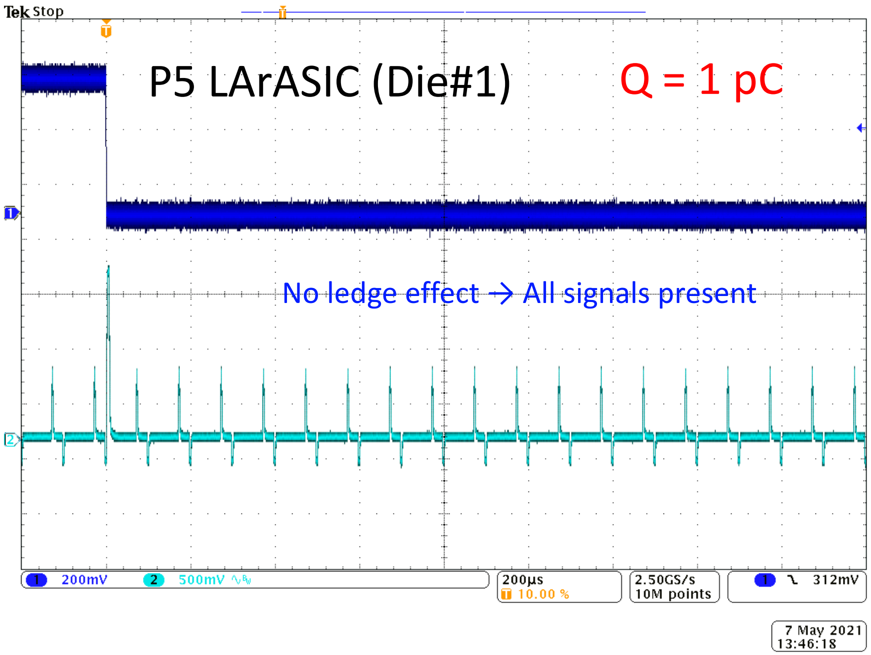


Measurements of P5 LArASIC (2)

P5 LArASIC: Eliminate the ledge effect (Success)

The ledge effect observed in ProtoDUNE operation has been addressed in P4 LArASIC. The P5 LArASIC has been tested to confirm the ledge effect remains solved.

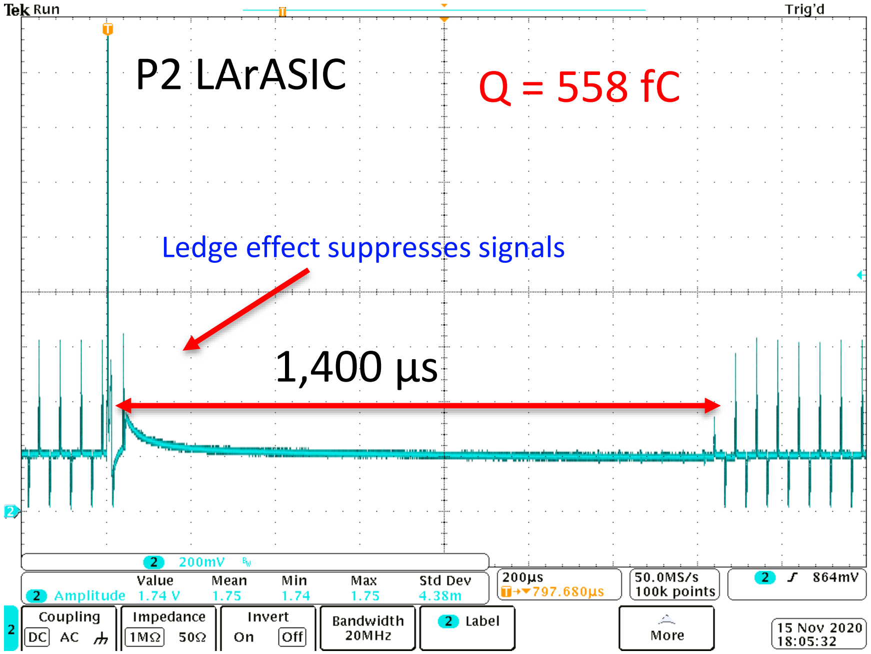
LN2, 200 mV baseline, 14 mV/fC, 1.0 µs, 500 pA



P5 LArASIC (Die#1)

Q = 1 pC

No ledge effect → All signals present



	Value	Mean	Min	Max	Std Dev
2 Amplitude	1.74 V	1.75	1.74	1.75	4.38m

P2 LArASIC

Q = 558 fC

Ledge effect suppresses signals

1,400 µs

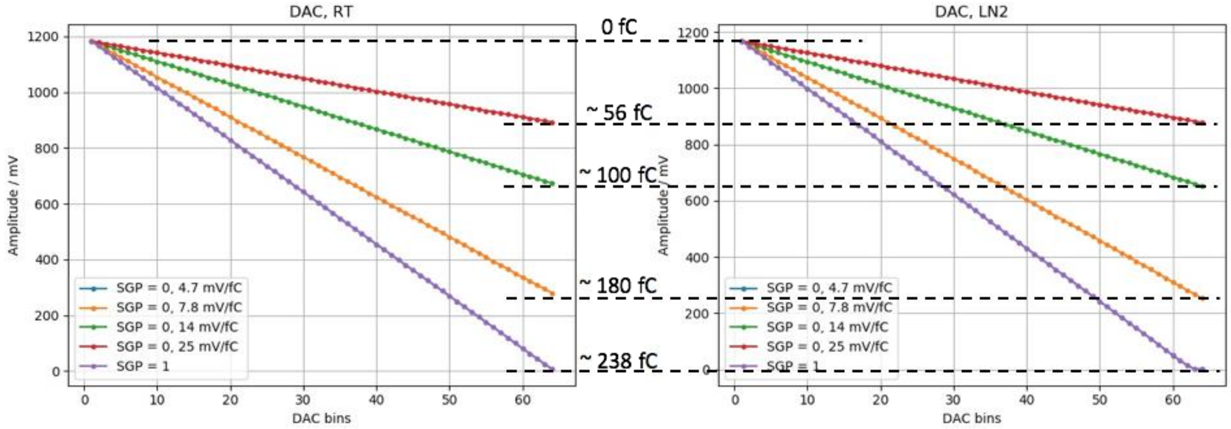
Ledge effect is not observed even with input charge > 2 pC

Measurements of P5 LArASIC (3)

- **No BGR startup issue is observed at LN2** (Success)
  - Many dies, 10+ packaged chips
- Baseline measurements at LN2 (Success)
  - Baseline variation is comparable to P4 with little impact on 1.4V dynamic range
    - 900 mV BL setting: 922 ± 7.3 mV (vs. P4 900 mV BL setting: 915 ± 10.1 mV)
    - 200 mV BL setting: 244 ± 7.1 mV (vs. P4 200 mV BL setting: 216 ± 7.6 mV)
- All channels alive at RT also survive at LN2 (Success)
  - Alive with 4 RQI (leakage) current settings (100pA, 500pA, 1nA, 5nA)
- The SEDC buffer works as expected (Success)
  - No excess current draw. The power consumption is ~5.5 mW/ch without buffer, ~9 mW/ch with single ended buffer turned on, and ~10.5 mW/ch with differential buffer turned on
  - No need external filtering circuit between LArASIC and ColdADC
  - Similar noise performance w/o SEDC

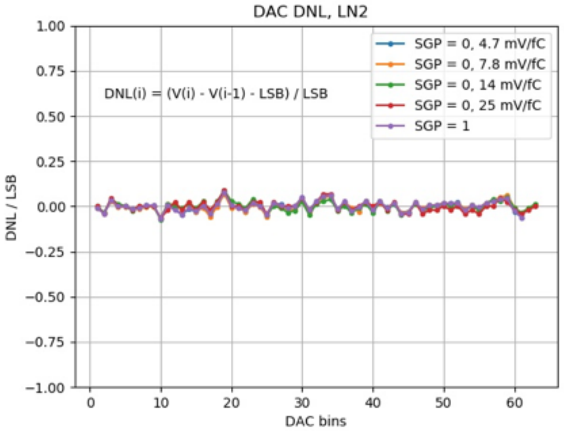
Measurements of P5 LArASIC (4)

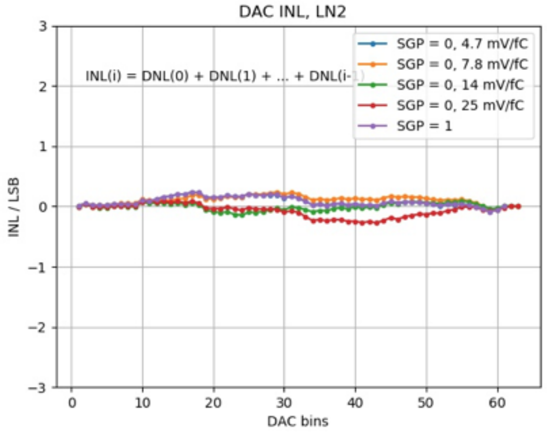
- DAC works well (Success)



Cover different dynamic ranges, and configurable through SGP bit

When SGP = 0, the DAC conversion slope follows the gain settings of channel 0, covering ~56 fC @ 25 mV/fC, ~100 fC @ 14 mV/fC, ~180 fC @ 7.8 mV/fC and ~238 fC @ 4.7 mV/fC

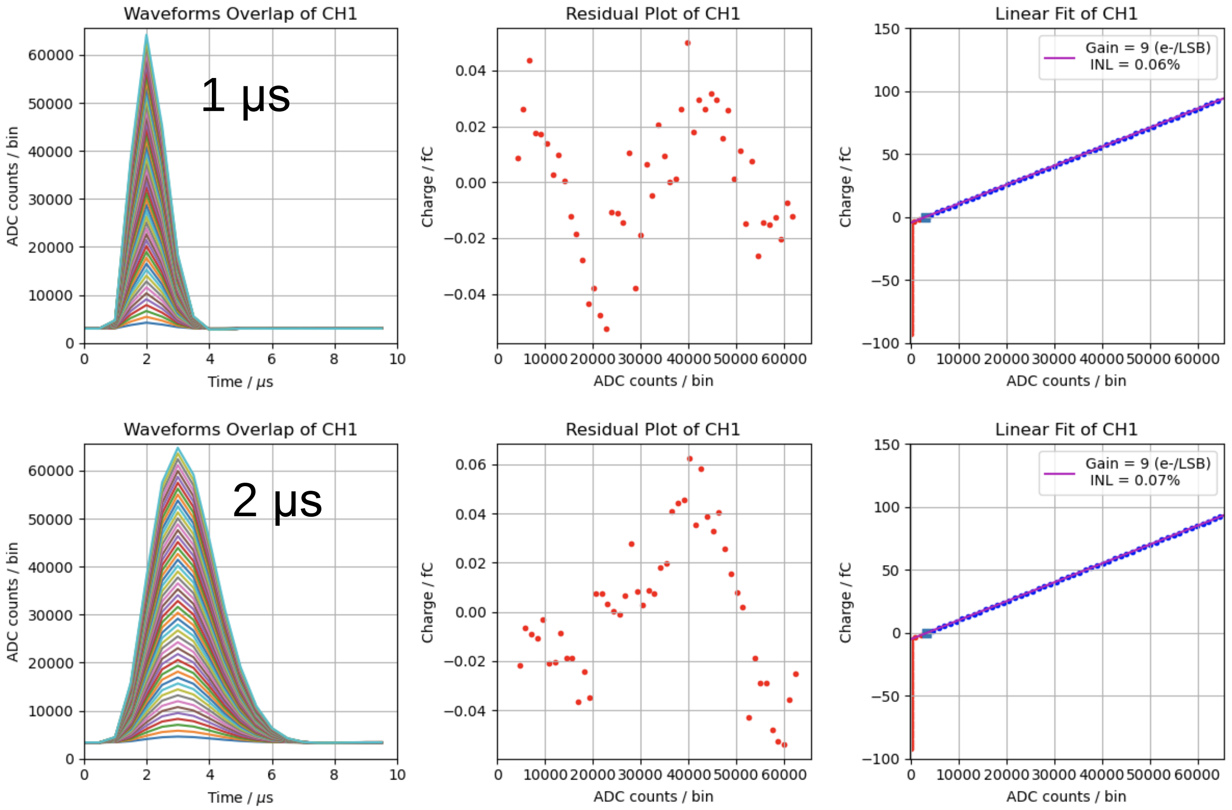




The DAC has DNL below ± 0.1 LSB, and INL below ± 0.5 LSB measured at LN2 temperature

Measurements of P5 LArASIC (5)

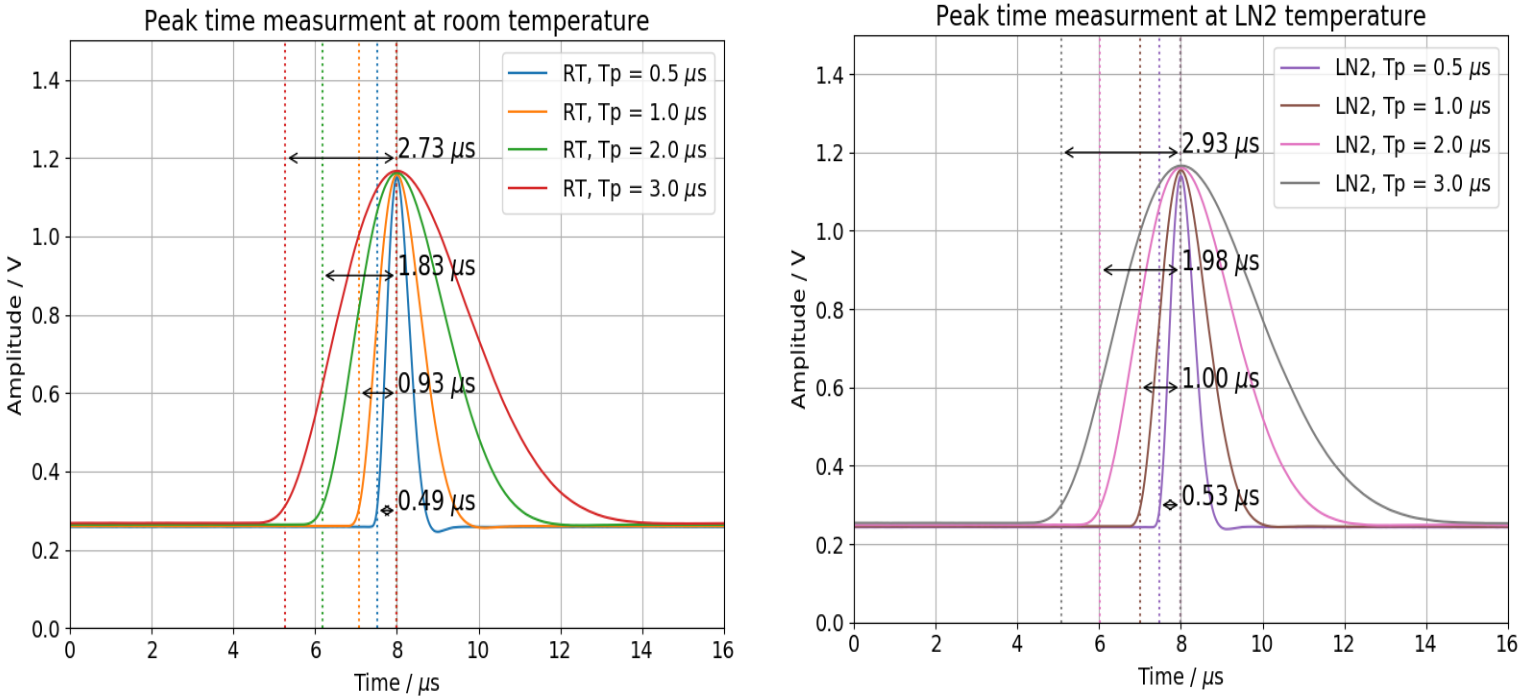
- Non-linearity < 0.1% in 90 fC range at LN2 (Success)
  - Gain = 14 mV/fC, peaking time = 1 μs or 2 μs



Signal generator Keysight 33600A is used to inject calibration pulses with precise amplitude. Voltage resolution of 33600A is 14-bit and the accuracy of amplitude is ± 1 mVp-p. Previous measurements with P2 LArASIC in 2019 show that the non-linearity of 33600A output is < 0.05%.

Measurements of P5 LArASIC (6)

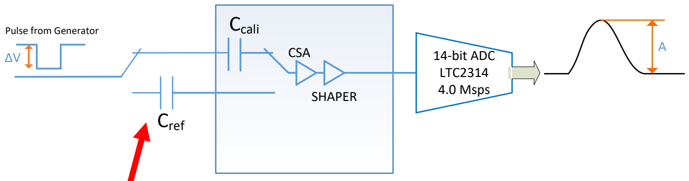
- **Peaking time meets design specification**
  - The peaking time doesn't change significantly before saturation occurs
  - The peaking time is independent from the gain configuration
  - The peaking time is independent from the baseline setting

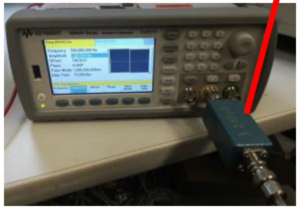


Peaking time measurement with data collected by oscilloscope. Each waveform is averaged 64 times, and a lowpass filter with 10 MHz cutoff has been applied offline. The peaking time is calculated from 5% to 100% peak amplitude.

Measurements of P5 LArASIC (7)

- Calibration capacitor measurement
  - MIM capacitor (Metal-Insulator-Metal) stable at RT and LN2





C_{ref} = 1.023 pF (calibrated by standard 1.0 pF capacitor and LCR meter)

Chip#	Channel	C_cali (RT)	C_cali (LN2)
P5 Chip 20	1	0.18714	0.184761
	2	0.186065	0.184628
	4	0.18611	0.184037
	5	0.186805	0.184264
P2 Chip 3716	1	0.190428	0.18995
	2	x	0.188295
	15	x	0.190759

- ➢ Channel to channel dispersion on the same chip is small (~ 1%)

- If ΔV is constant
  - $C_{cali} : C_{ref} = A_{cali} : A_{ref}$
  - LCR and precise 1.0 pF standard capacitor are used to calibrate C_{ref}
    - C_{ref} is always put in room environment

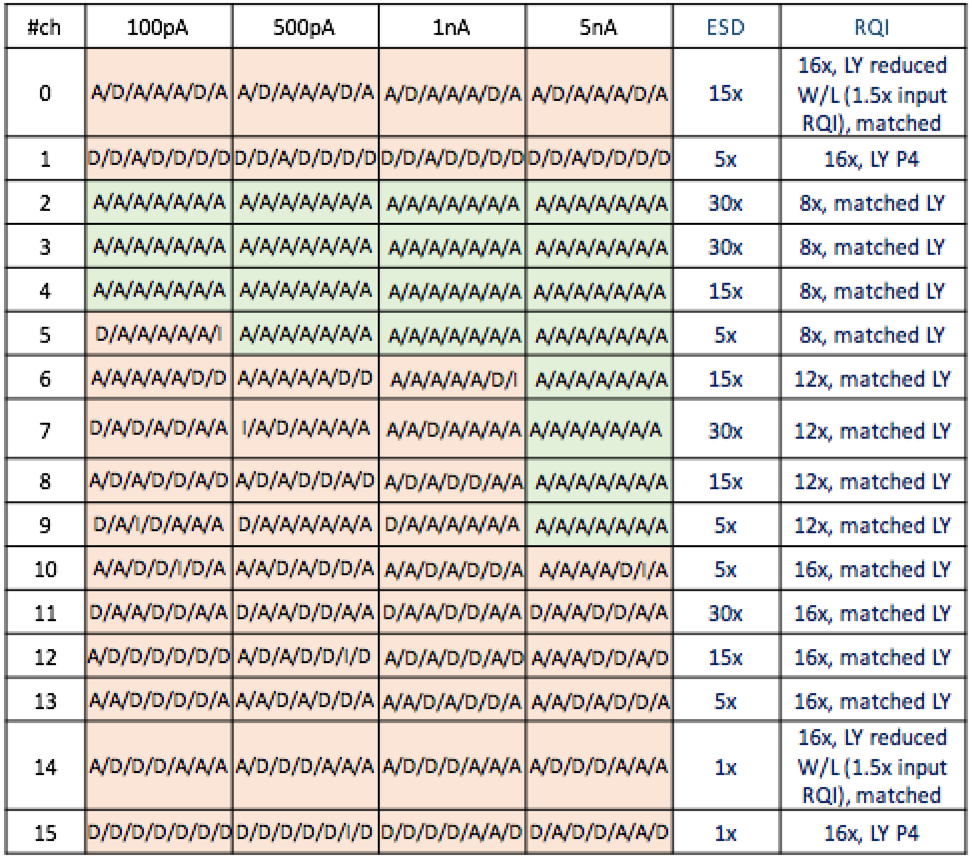
P5 Chip#	**Channel**	**C_cali (at LN)**
3	10	0.184628
6	15	0.184841
13	5	0.185199
14	10	0.186519
16	10	0.187015

- ➢ Chip to chip dispersion (even same batch) can be > 2%
  - QC test should include calibration capacitor measurement

Measurements of P5A LArASIC (1)

- **Even 8x RQI subtraction can't guarantee all channels alive**

LN2, Die# 01/02/03/04/05/06/07

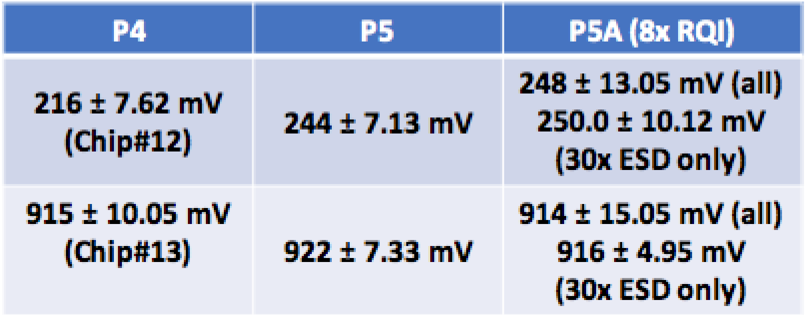


#ch	100pA	500pA	1nA	5nA	ESD	RQI
0	A/D/A/A/A/D/A	A/D/A/A/A/D/A	A/D/A/A/A/D/A	A/D/A/A/A/D/A	15x	16x, LY reduced W/L (1.5x input RQI), matched
1	D/D/A/D/D/D/D	D/D/A/D/D/D/D	D/D/A/D/D/D/D	D/D/A/D/D/D/D	5x	16x, LY P4
2	A/A/A/A/A/A/A	A/A/A/A/A/A/A	A/A/A/A/A/A/A	A/A/A/A/A/A/A	30x	8x, matched LY
3	A/A/A/A/A/A/A	A/A/A/A/A/A/A	A/A/A/A/A/A/A	A/A/A/A/A/A/A	30x	8x, matched LY
4	A/A/A/A/A/A/A	A/A/A/A/A/A/A	A/A/A/A/A/A/A	A/A/A/A/A/A/A	15x	8x, matched LY
5	D/A/A/A/A/A/I	A/A/A/A/A/A/A	A/A/A/A/A/A/A	A/A/A/A/A/A/A	5x	8x, matched LY
6	A/A/A/A/A/D/D	A/A/A/A/A/D/D	A/A/A/A/A/D/I	A/A/A/A/A/A/A	15x	12x, matched LY
7	D/A/D/A/D/A/A	I/A/D/A/A/A/A	A/A/D/A/A/A/A	A/A/A/A/A/A/A	30x	12x, matched LY
8	A/D/A/D/D/A/D	A/D/A/D/D/A/D	A/D/A/D/D/A/A	A/A/A/A/A/A/A	15x	12x, matched LY
9	D/A/I/D/A/A/A	D/A/A/A/A/A/A	D/A/A/A/A/A/A	A/A/A/A/A/A/A	5x	12x, matched LY
10	A/A/D/D/I/D/A	A/A/D/A/D/D/A	A/A/D/A/D/D/A	A/A/A/A/D/I/A	5x	16x, matched LY
11	D/A/A/D/D/A/A	D/A/A/D/D/A/A	D/A/A/D/D/A/A	D/A/A/D/D/A/A	30x	16x, matched LY
12	A/D/D/D/D/D/D	A/D/A/D/D/I/D	A/D/A/D/D/A/D	A/A/A/D/D/A/D	15x	16x, matched LY
13	A/A/D/D/D/D/A	A/A/D/A/D/D/A	A/A/D/A/D/D/A	A/A/D/A/D/D/A	5x	16x, matched LY
14	A/D/D/D/A/A/A	A/D/D/D/A/A/A	A/D/D/D/A/A/A	A/D/D/D/A/A/A	1x	16x, LY reduced W/L (1.5x input RQI), matched
15	D/D/D/D/D/D/D	D/D/D/D/D/I/D	D/D/D/D/A/A/D	D/A/D/D/A/A/D	1x	16x, LY P4

A= alive
D= dead
I = Intermittent (alive/dead)

Another ~10 P5A dies have been tested shows similar result.

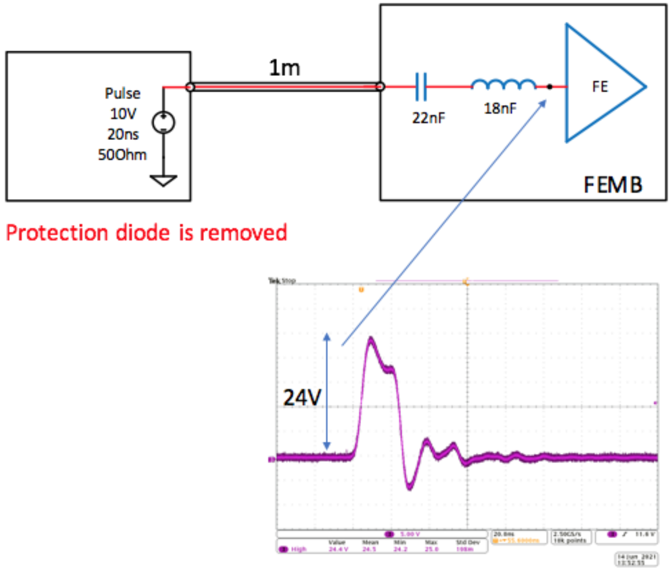
RQI subtraction doesn't help minimize the baseline dispersion in LN2



P4	P5	P5A (8x RQI)
216 ± 7.62 mV (Chip#12)	244 ± 7.13 mV	248 ± 13.05 mV (all) 250.0 ± 10.12 mV (30x ESD only)
915 ± 10.05 mV (Chip#13)	922 ± 7.33 mV	914 ± 15.05 mV (all) 916 ± 4.95 mV (30x ESD only)

Measurements of P5A LArASIC (2)

- ESD protection measurements



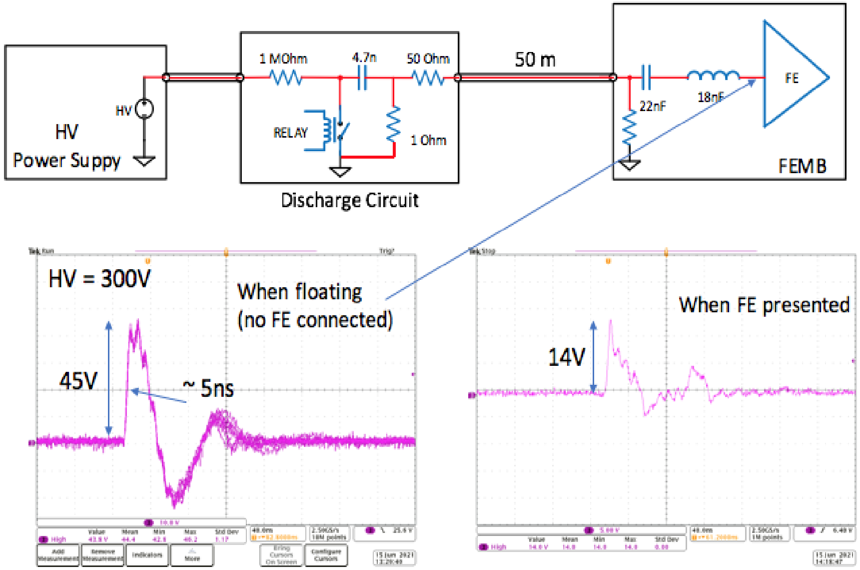
If FE is not presented (RT)

With a pulser to generate **10 V 20 ns** pulse and inject to the P5A LArASIC input, then check how many pulses the channel with different ESD protections can tolerate before damage occurs. Input leakage current measured by SMU can be used to characterize the level of damage, and it can detect **minor deterioration** before the channel behaves completely abnormally.

- **Tolerance of discharge duration**
  - Channels with 1x ESD protection can survive 1 or a few pulses
  - Channels with 5x ESD protection can survive more than 900k pulses
  - Channels with 15x ESD protection can survive more than 1,500k pulses
  - Channels with 30x ESD protection can survive more than 2,500k pulses

Measurements of P5A LArASIC (3)

- ESD protection measurements



With a HV power supply to generate 5 ns pulse and inject to the P5A LArASIC input, then check how large of the pulse amplitude the channel with different ESD protections can tolerate before damage occurs. Three different P5A dies #03, #03_02 and #03_03 were measured with a consistent result.

- **Tolerance of discharge amplitude**

	RT		LN2	
LArASIC	-HV (+Pulse)	+HV (-Pulse)	-HV (+Pulse)	+HV (-Pulse)
P4, 1x	+31 V		+59 V	-76 V
P5, 1x	+31 V	-44 V	+59 V	-91 V
P5A, 1x	+45 V		+45 V	-83 V
P5A, 5x	+37 V	-53 V	+75 V	-83 V
P5A, 15x	+62 V	-86 V	+103 V	-140 V <5 pls
P5A, 30x	+86 V	-143 V <100 pls	+154 V <5 pls	-172 V <25 pls

Note: Noise measurement confirmed 30x ESD has little contribution to noise. The dominant noise is from detector capacitance.

It is decided to implement 30x ESD in P5B.

Content

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- **Full Chain Measurements**
  - P4 LArASIC + P2 ColdADC
  - P5 LArASIC + P2 ColdADC
- System Tests
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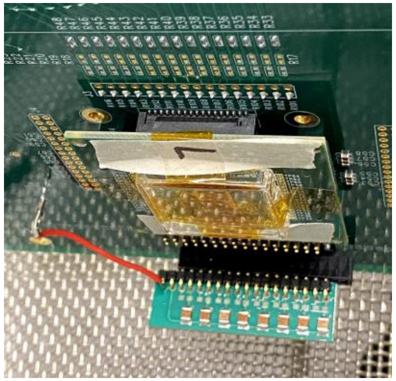
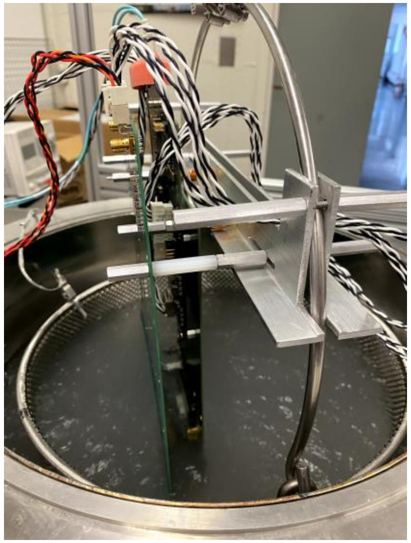
P4 LArASIC + P2 ColdADC Full Chain Test (1)

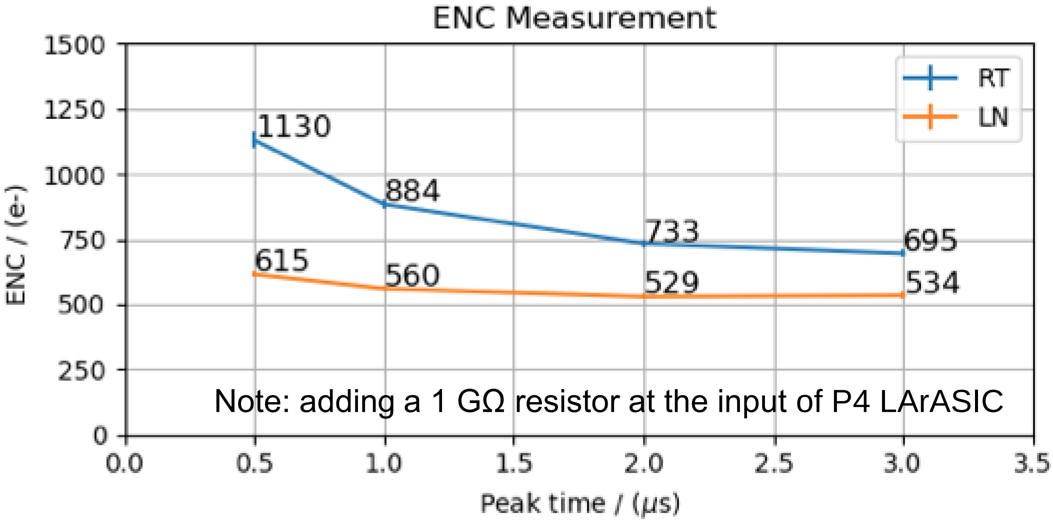


P4 LArASIC with 150 pF



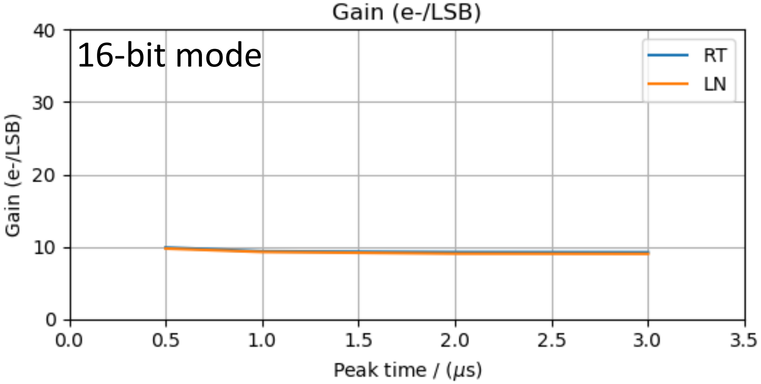
Evaluation in LN2
with P2 ColdADC

Achieve expected noise and gain performance



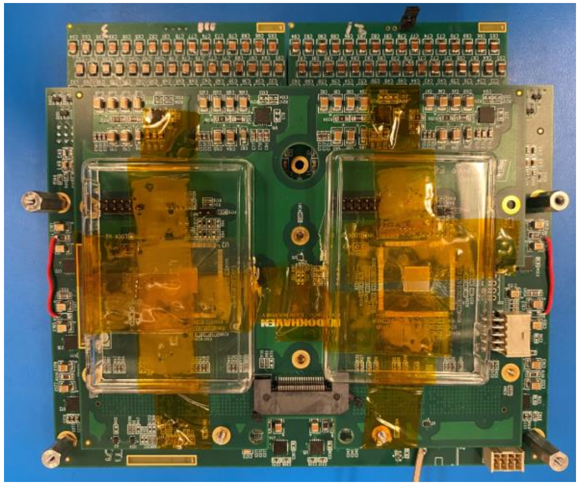
Note: adding a 1 GΩ resistor at the input of P4 LArASIC

900 mV BL, 14 mV/fC gain, SE output w/o buffer, 16-bit ADC mode
ENC ~ 600 e^- @ t_p = 1 μs with C_d = 150 pF and stable gain



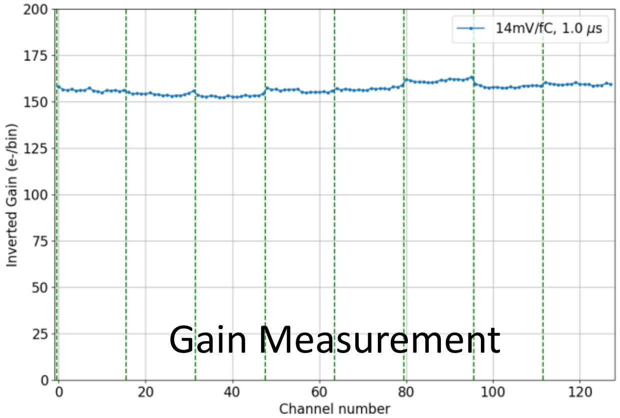
P4 LArASIC + P2 ColdADC Full Chain Test (2)

- Configuration
    - LArASIC: Single-ended, 14mV/fC, buf off, 200mV BL
    - ColdADC: Single-ended, default reference, auto-calibration
    - COLDATA: Enable LArASIC internal calibration



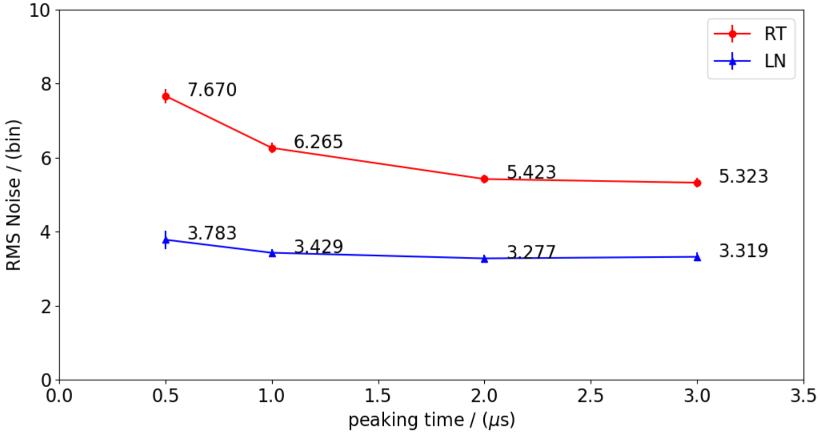
Mezzanine FEMB

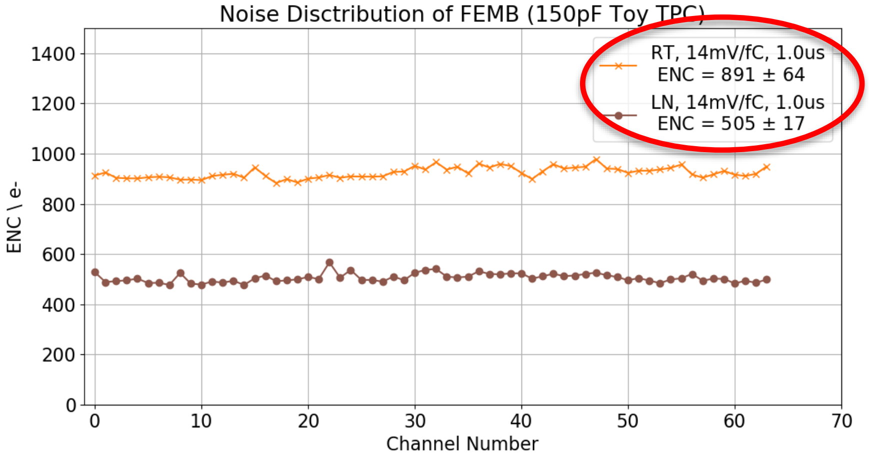
(8x P4 LArASIC + 8x P2 ColdADC + 2x P2 COLDATA)



Gain Measurement

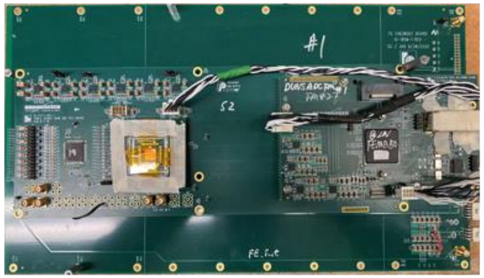
RMS Noise Measurement



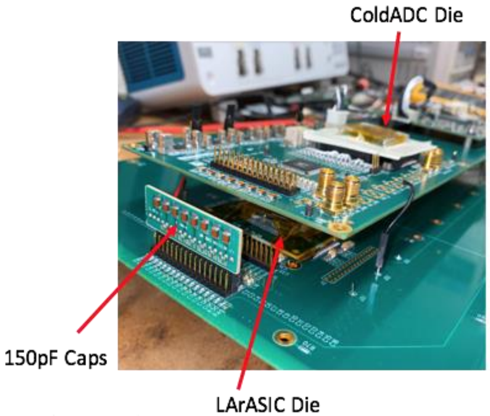


Noise is comparable with ProtoDUNE and SBND FEMBs

P5 LArASIC + P2 ColdADC Full Chain Test (1)



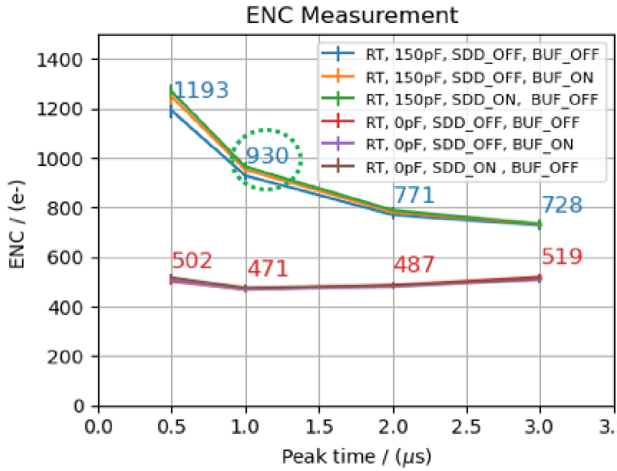
LArASIC P5 + ColdADC P2 full chain test board assembly

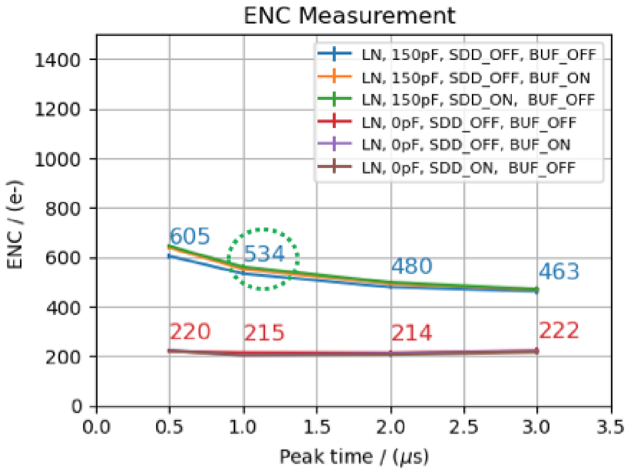


P5 LArASIC and P2 ColdADC full chain test board assembly

- P5 LArASIC single chip test board
- P2 ColdADC test board
- ProtoDUNE FPGA mezzanine

14mV/fC, 200mV BL, ADC 16-bit mode

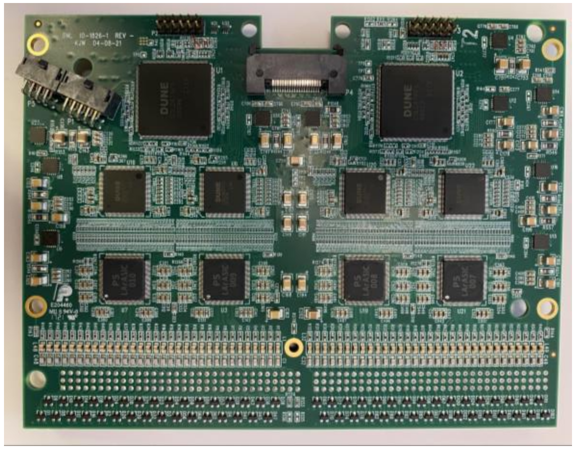


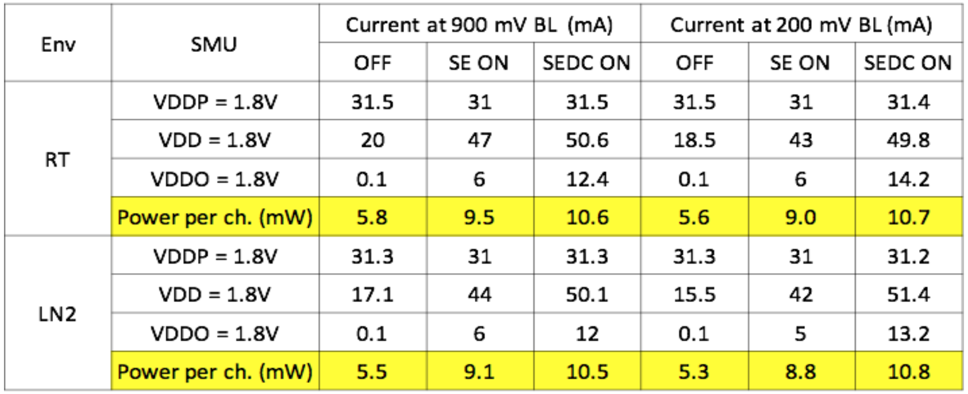


- With 14 mV/fC gain and 200 mV baseline settings, the P5 LArASIC has ENC ~930 e^{-} at room temperature, and ~530 e^{-} at LN2 temperature
- Very small difference is observed with different output buffer configurations

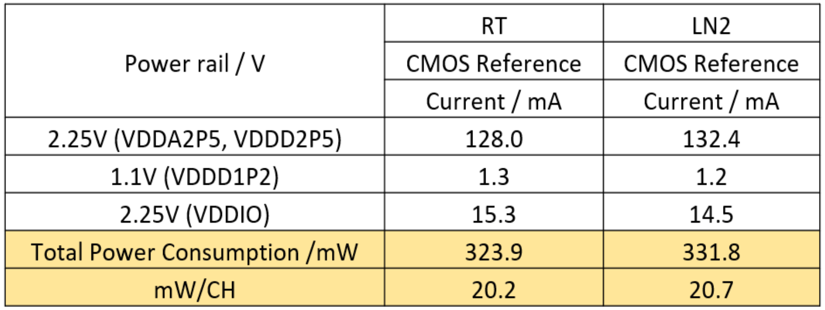
P5 LArASIC + P2 ColdADC Full Chain Test (2)

- The first version of the monolithic FEMB
  - 8x P5 LArASIC + 8x P2 ColdADC + 2x P3 COLDATA

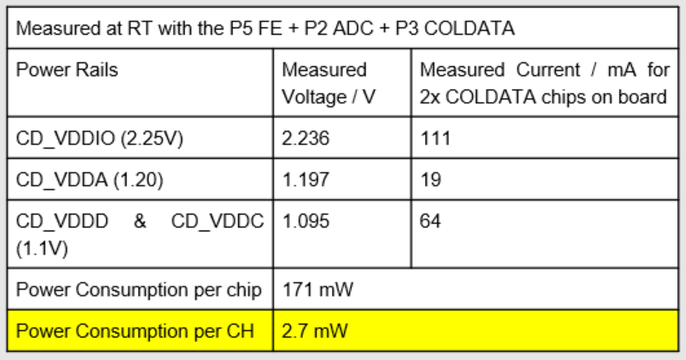




Env	SMU	Current at 900 mV BL (mA)			Current at 200 mV BL (mA)		
		OFF	SE ON	SEDC ON	OFF	SE ON	SEDC ON
RT	VDDP = 1.8V	31.5	31	31.5	31.5	31	31.4
	VDD = 1.8V	20	47	50.6	18.5	43	49.8
	VDDO = 1.8V	0.1	6	12.4	0.1	6	14.2
	Power per ch. (mW)	5.8	9.5	10.6	5.6	9.0	10.7
LN2	VDDP = 1.8V	31.3	31	31.3	31.3	31	31.2
	VDD = 1.8V	17.1	44	50.1	15.5	42	51.4
	VDDO = 1.8V	0.1	6	12	0.1	5	13.2
	Power per ch. (mW)	5.5	9.1	10.5	5.3	8.8	10.8



Power rail / V	RT	LN2
	CMOS Reference	CMOS Reference
	Current / mA	Current / mA
2.25V (VDDA2P5, VDDD2P5)	128.0	132.4
1.1V (VDDD1P2)	1.3	1.2
2.25V (VDDIO)	15.3	14.5
Total Power Consumption /mW	323.9	331.8
mW/CH	20.2	20.7

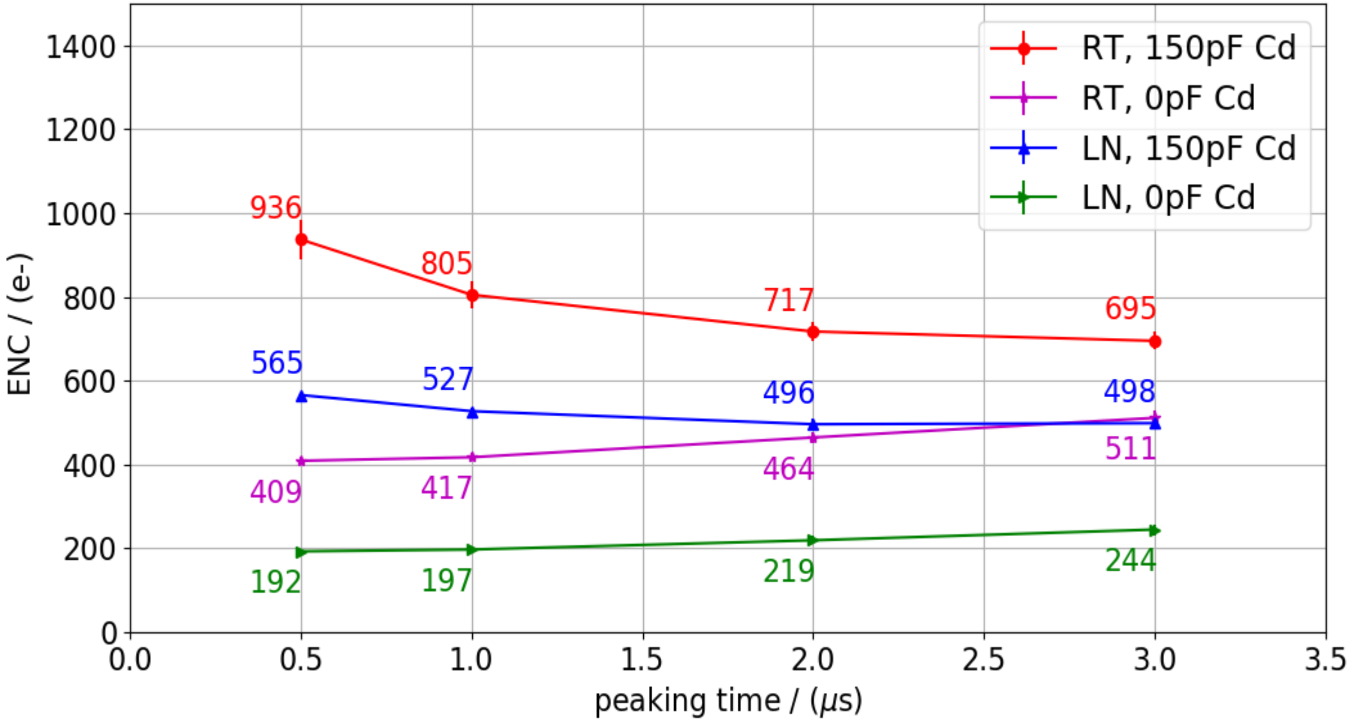


Measured at RT with the P5 FE + P2 ADC + P3 COLDATA		
Power Rails	Measured Voltage / V	Measured Current / mA for 2x COLDATA chips on board
CD_VDDIO (2.25V)	2.236	111
CD_VDDA (1.20)	1.197	19
CD_VDDD & CD_VDDC (1.1V)	1.095	64
Power Consumption per chip	171 mW	
Power Consumption per CH	2.7 mW	

The power consumption is ~29 mW/ch with single ended output without buffer, and ~34 mW/ch with differential output and SEDC buffer turned on. Considering the power consumption in voltage regulators, with ~300 mV voltage drop of voltage regulators, **the total power consumption of a monolithic FEMB is less than ~45 mW/ch, or a total ~5.8 W.**

P5 LArASIC + P2 ColdADC Full Chain Test (3)

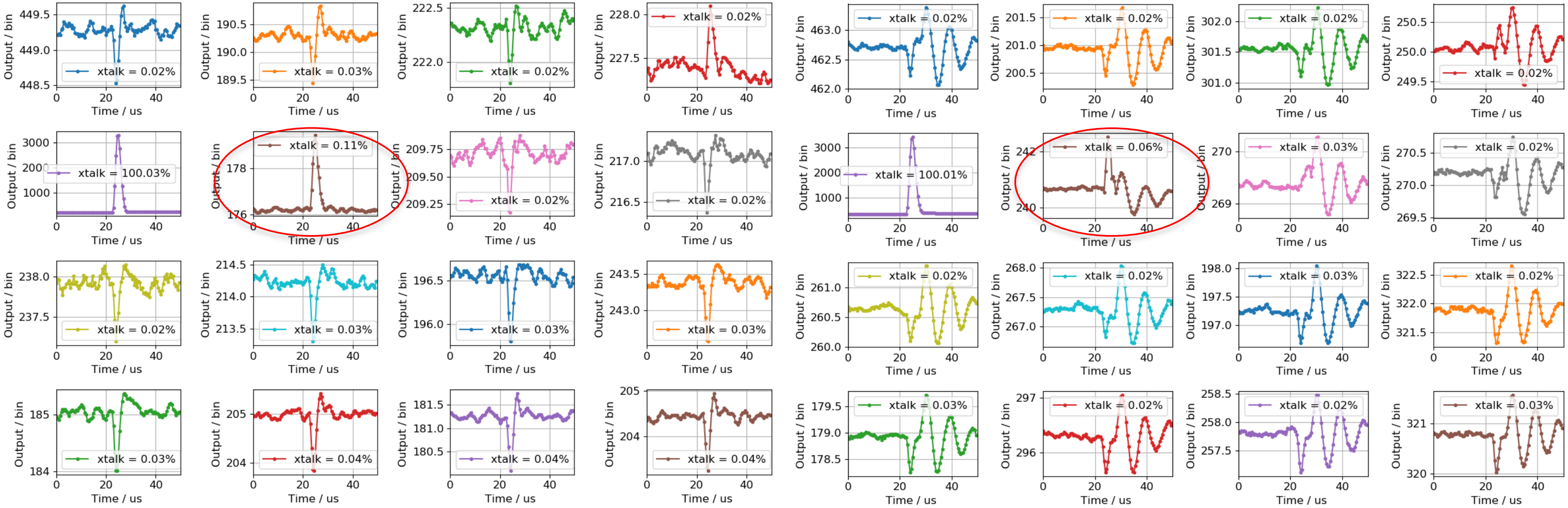
Noise performance of monolithic FEMB with P5 LArASIC, P2 ColdADC and P3 COLDATA at both room temperature and LN2 temperature. Input is loaded with 150pF C_d or floating (0 pF). Uniform inverted gain 160 e^-/bit is used for room temperature data, and 154 e^-/bit used for LN2 data.



ENC is ~520 e^- with 1 μs peaking time and 150 pF detector capacitance at LN2 temperature.

P5 LArASIC + P2 ColdADC Full Chain Test (4)

- Crosstalk < 0.2% with differential interface between LArASIC and ColdADC
  - With external ~70fC injected on CH4 among CH0 - CH15, waveforms displayed for all 16 channels of a LArASIC
    - External charge: 72fC = 60 mV from Signal Generator * 1.203pF reference capacitor
  - Slightly larger crosstalk level with single-ended interface between LArASIC and ColdADC at LN2
  - The measurement shows the crosstalk of the full readout chain is < 0.1% at LN2.



At room temperature

At LN2

Note: The crosstalk plot shown in “LArASIC Development and Characterization Tests” in EDMS was generated with the internal calibration pulse. The periodic test pulse from COLDATA has a visible impact on the channels even if the calibration circuits are disabled.

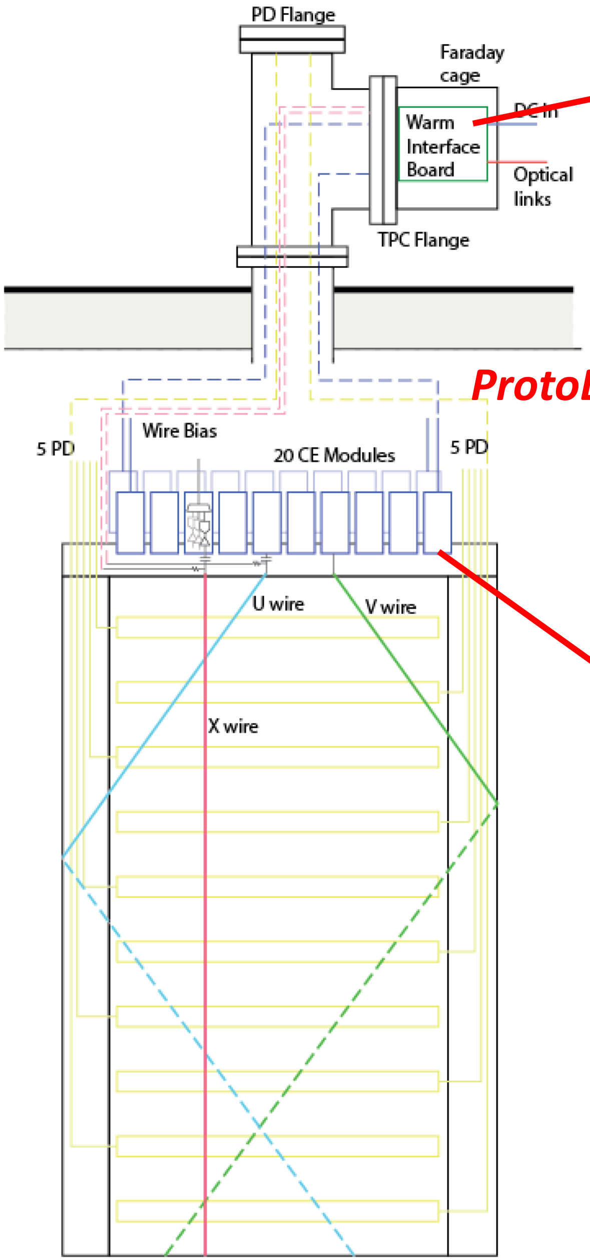
Content

- LArASIC Requirements and Specifications
- Measurements to confirm design changes
- Full Chain Measurements
- **System Tests**
  - Integral System Design Concept
  - 40% APA integration test at BNL
  - ICEBERG
- Summary

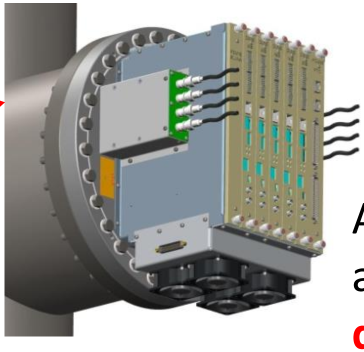
Integral System Design Concept

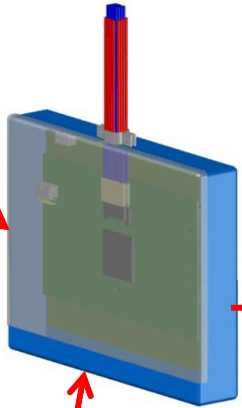
A necessary (but not sufficient!) condition to achieve a good performance, **the integral design concept** of APA + CE + Feed-through, plus Warm Interface Electronics with **local diagnostics** and strict isolation and **grounding rules** will have to be followed

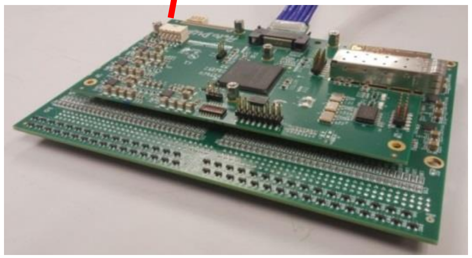
BNL: 40% APA test stand (LN_2)
CERN: Cold box test stand (Cold N_2 gas)
Fermilab: ICEBERG test stand (LAr)

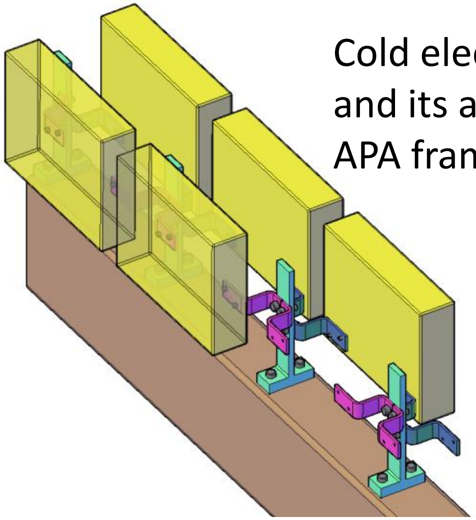


ProtoDUNE-SP





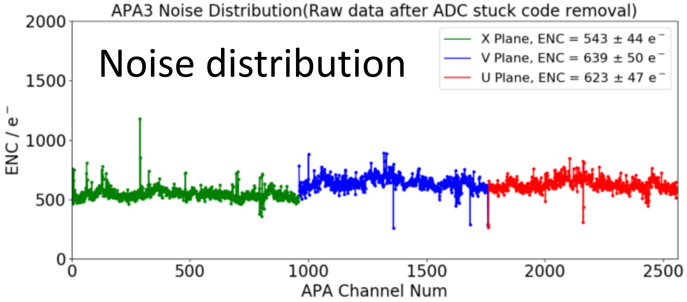


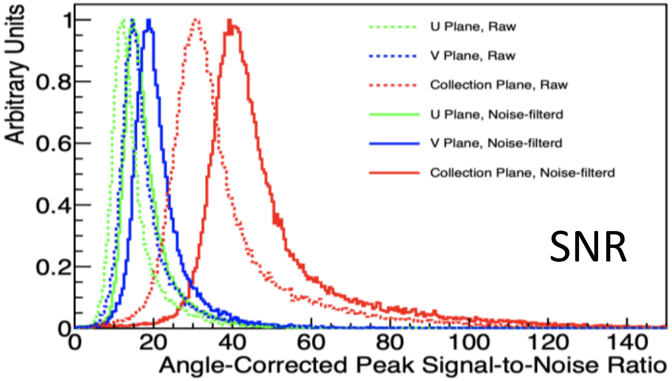


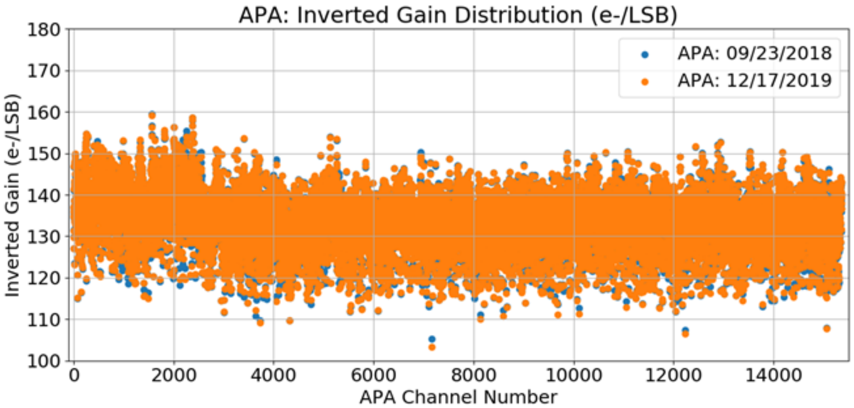
Cold electronics module and its attachment to the APA frame

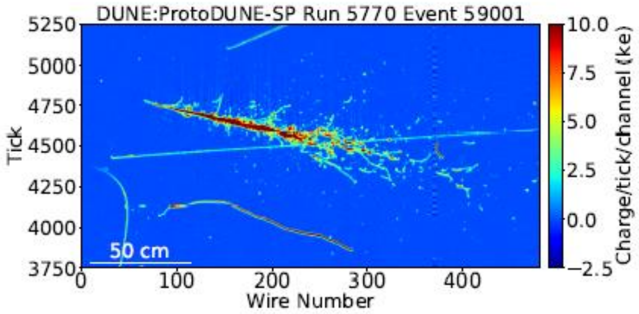
Performance of the ProtoDUNE-SP

- **High yield**
  - 99.74% (15,320 of 15,360) of TPC channels are active
    - Only 4 inactive cold electronics channels when commissioning started
    - 2 more inactive cold electronics after > 1 year running
- **Low noise**
  - 92.83% TPC channels are good with excellent noise performance
    - Raw data: Collection ENC ~560 e^-, Induction ENC ~670 e^-
- **Good stability**
    - No measurable degradation is observed over a year
    - MicroBooNE LArASIC < 0.2% over 3-4 years



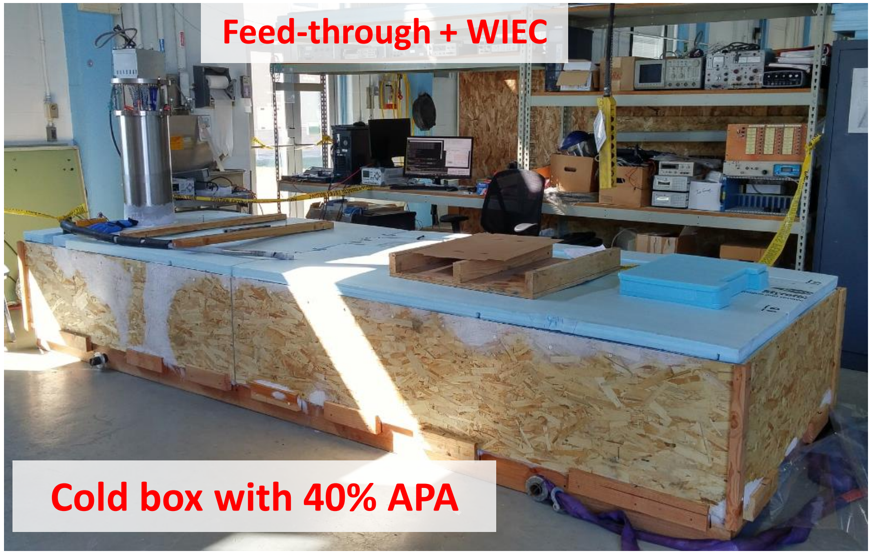






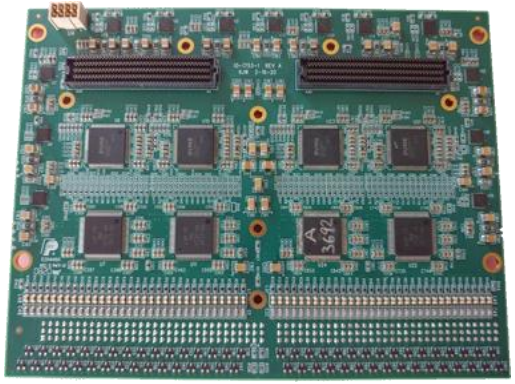
A 6 GeV/c electron candidate

40% APA Integration Test at BNL (1)

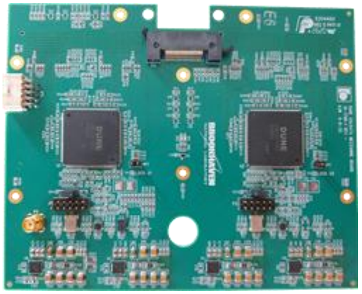


40% APA: 2.8m x 1.0m, 1,024 wires

DUNE Zynq+ WIB

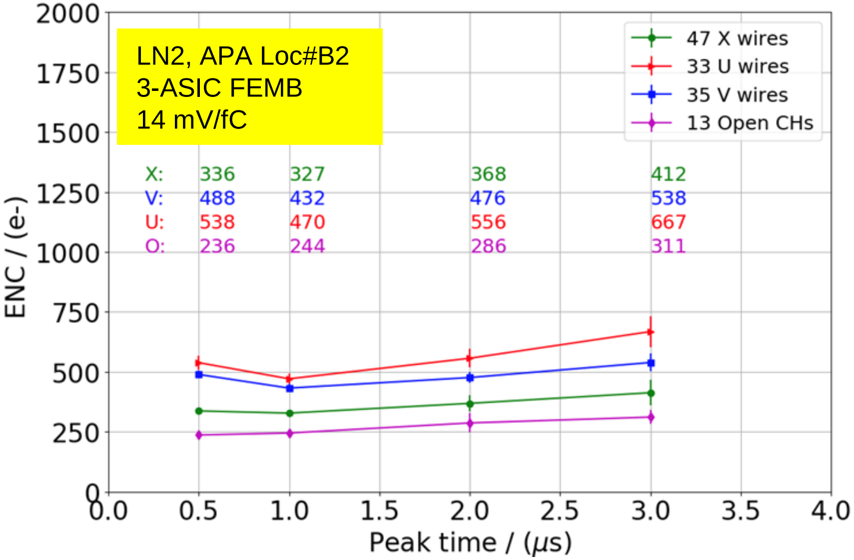


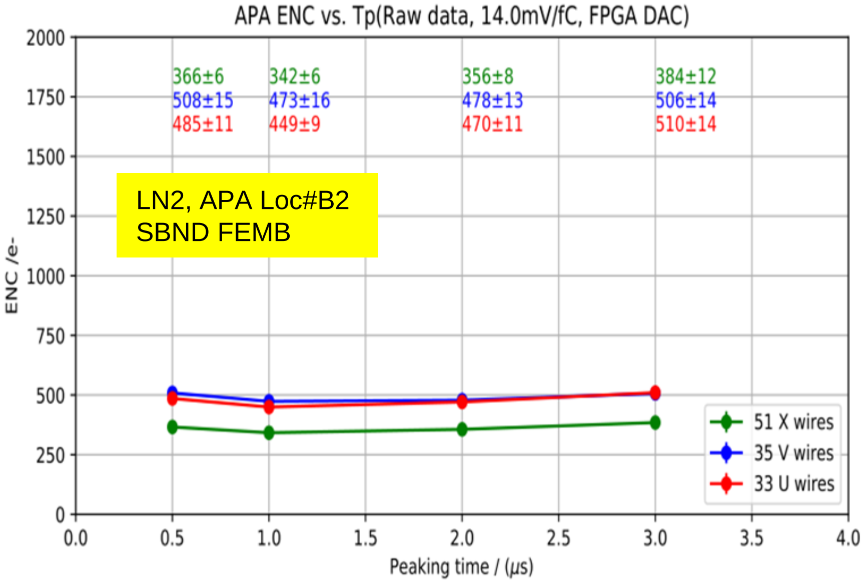
Analog Motherboard
(P2 LArASIC + P1 ColdADC)



COLDATA Mezzanine
(P2 COLDATA)

40% APA Integration Test at BNL (2)

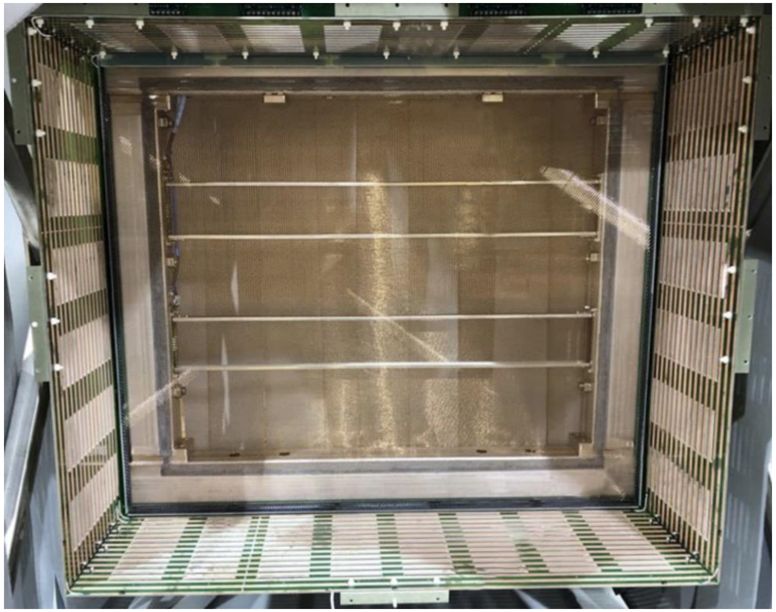




- Noise levels measured in the 40% APA are in line with those obtained with SBND FEMBs (COTS ADCs)
- Promising noise projection
  - DUNE-SP U/V plane : ENC ~ 600 e^- w/o offline filtering
  - DUNE-SP X plane: ENC ~ 500 e^- w/o offline filtering

ICEBERG Test at Fermilab (1)

Outside of ICEBERG



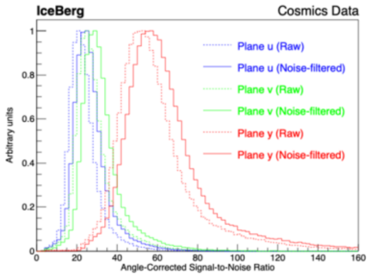
Inside of ICEBERG

COTS-ADC FEMB in Run4

3-ASIC FEMB in Run5

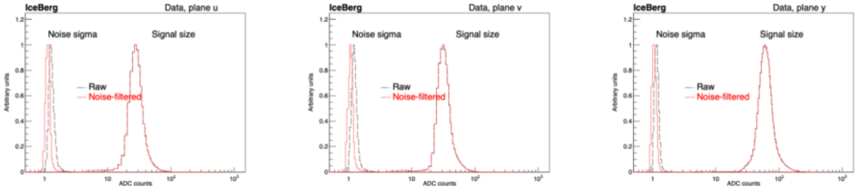
ICEBERG Test at Fermilab (2)

Run4 (COTS ADC) 7080-7210

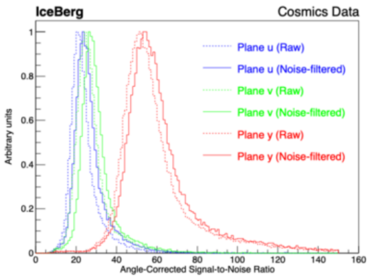


Plane	Most probable value	
	Raw data	Noise-filtered
Induction U	21.2 ± 0.0	24.2 ± 0.0
Induction V	24.8 ± 0.0	28.3 ± 0.1
Collection Y	51.9 ± 0.1	56.7 ± 0.1

Plane	Average	
	Raw data	Noise-filtered
Induction U	23.8 ± 0.0	27.2 ± 0.0
Induction V	28.6 ± 0.0	32.8 ± 0.0
Collection Y	59.5 ± 0.0	64.8 ± 0.0

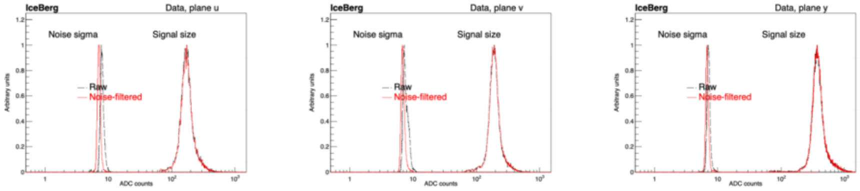


Run5 (3-ASIC) 8898-8947

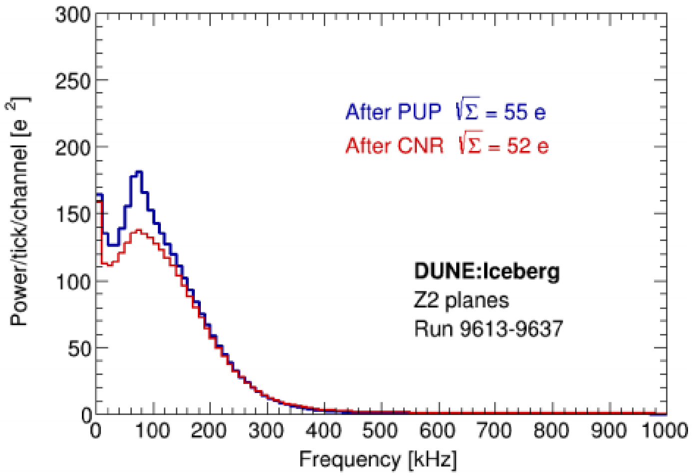


Plane	Most probable value	
	Raw data	Noise-filtered
Induction U	21.4 ± 0.1	23.9 ± 0.1
Induction V	24.8 ± 0.1	27.3 ± 0.1
Collection Y	51.9 ± 0.1	54.7 ± 0.1

Plane	Average	
	Raw data	Noise-filtered
Induction U	24.3 ± 0.1	27.1 ± 0.1
Induction V	27.6 ± 0.0	30.6 ± 0.1
Collection Y	59.6 ± 0.1	62.4 ± 0.1



- FEMBs with 3 ASIC solution have same level of noise compared to ProtoDUNE FEMBs, few % higher than SBND FEMBs based on COTS ADC
- As in ProtoDUNE removal of coherent noise reduces overall noise level at the 5-10% level
- Coherent noise mostly concentrated at low frequency (< 200 kHz)
  - Continuous effort to mitigate the coherent noise



Response to Charge Questions for LArASIC

- Have the issues with the baseline shifts been addressed by the latest iteration of this chip? (**Yes**)
  - Baseline distortion caused by Packaging has been fixed in P3 version
    - Modify DC circuits for collection mode similar as the induction mode
  - Presented in DUNE PDR: TPC electronics ASIC/FEMB (02/2020)
    - https://indico.fnal.gov/event/22423/
- Initial operation of ProtoDUNE-SP has indicated some problems with baseline restoration that in principle had been addressed in the version of the ASIC being used. Is the source of these problems understood? (**Yes**)
  - Ledge effect has been eliminated
- Was there any improvement in the ESD protection of LArASIC? (**Yes**)
  - A promising ESD protection scheme shown in P5A
  - P5B will use the best ESD protection scheme in P5A

Summary

- System noise < 1000 e- [SP-FD-2] (**Achievable**)
- FE peaking time adjustable from 1 to 3 μs [SP-FD-13] (**Confirmed**)
- Signal saturation level ~500,000 e- (80 fC) [SP-FD-14] (**Confirmed**)
  - **Gain of the front-end amplifier ~ 10 mV/fC [SP-ELEC-2, 2284]**
- Dead channels < 1% [SP-FD-28] (**Achievable**)
- Cold electronics power consumption < 50 mW/channel [SP-FD-21] (**Confirmed**)
- Two baselines in the front-end amplifier [SP-ELEC-1, 2283] (**Confirmed**)
- Input capacitance to front-end ASIC should be optimized for 120 to 210 pF [SP-ELEC-12] (**Confirmed**)
- Channel-to-channel crosstalk < 1% (goal of < 0.1%) [SP-ELEC-11] (**Confirmed**)
- Monotonic saturation recovery [SP-ELEC-10] (**Confirmed**)
  - No ledge effect up to 2 pC

Backups

Lifetime Study

- LArASIC is designed for long lifetime at cryogenic temperatures, with minimum gate length of 270 nm in TSMC 180 nm technology.
  - To alleviate the lifetime risk, custom ASIC should be designed for one or two orders of magnitude longer lifetime than 30 years, by selection of Vdd and L, essentially to get out of the region of degradation measurable after 30 years
- LArASIC lifetime measurement will be performed with the single chip test board.
  - In the exploratory phase, we have to define criteria of lifetime from the stress test with elevated supply voltage.
  - After that, in the validation phase, we need to collect data by testing more chips to validate what we would have learned in the exploratory phase.
- It is expected that the lifetime measurement will be completed before the PRR

- **CMOS in DC operation**

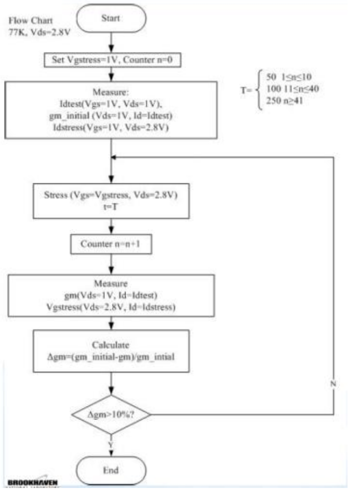
→ ALT at any temperature (well-established by foundries) transistor is placed under a severe electric field stress (large V_{DS}), to reduce the lifetime due to hot-electron degradation to a practically observable range.

→ ALT is widely used by industry

→ Lifetime is projected by empirical equation $log_{10}\tau \propto 1/V_{ds}$

- **CMOS in AC operation**

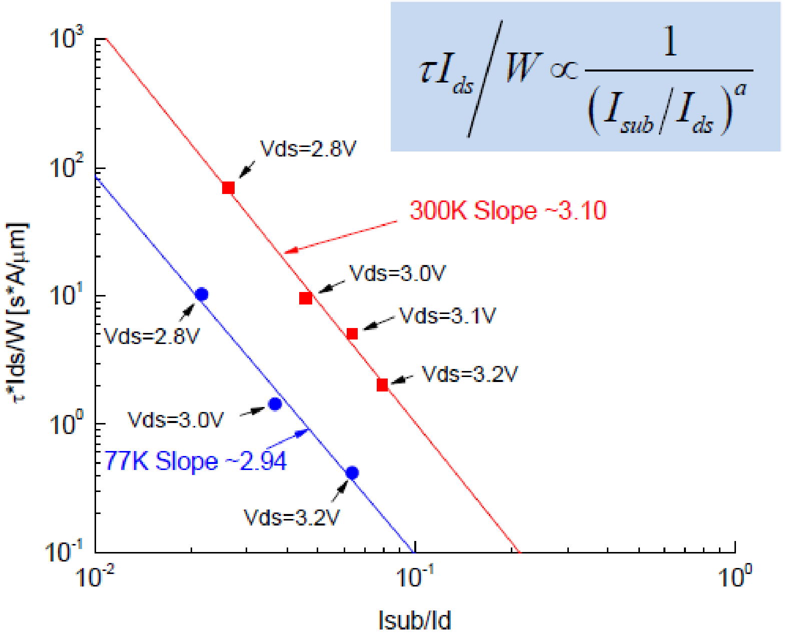
→ Lifetime of digital circuits (ac operation) is extended by the inverse duty factor $4/(f_{clock}{*}t_{rise})$ compared to dc operation. This factor is large (>100) for deep submicron technology and clock frequency needed for TPC



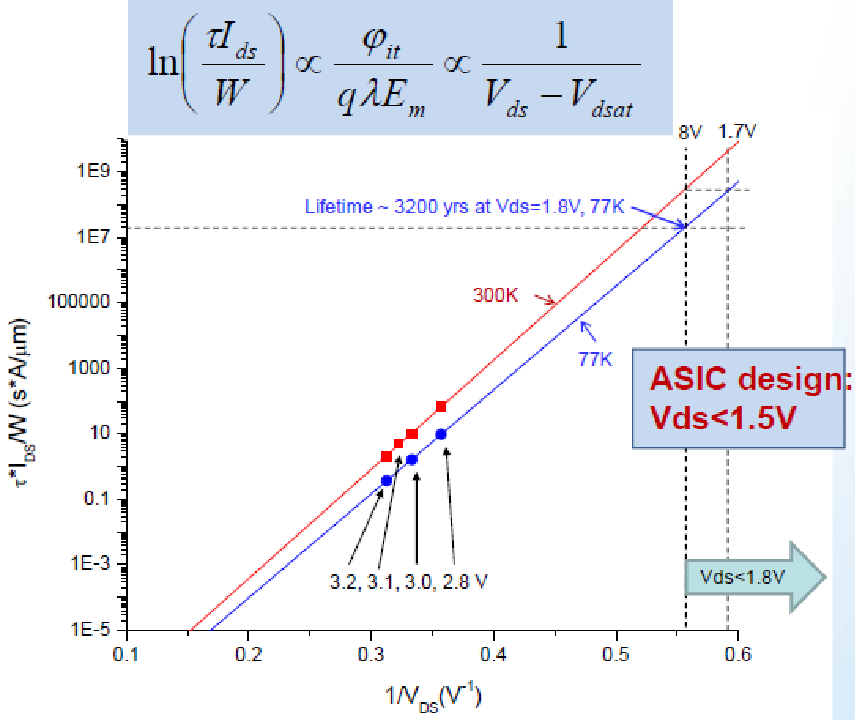
Appendix

Accelerated Lifetime Measurements (180 nm)

Measurement Type I: **“Stress Plot”**



$$\tau I_{ds}/W \propto \frac{1}{(I_{sub}/I_{ds})^a}$$



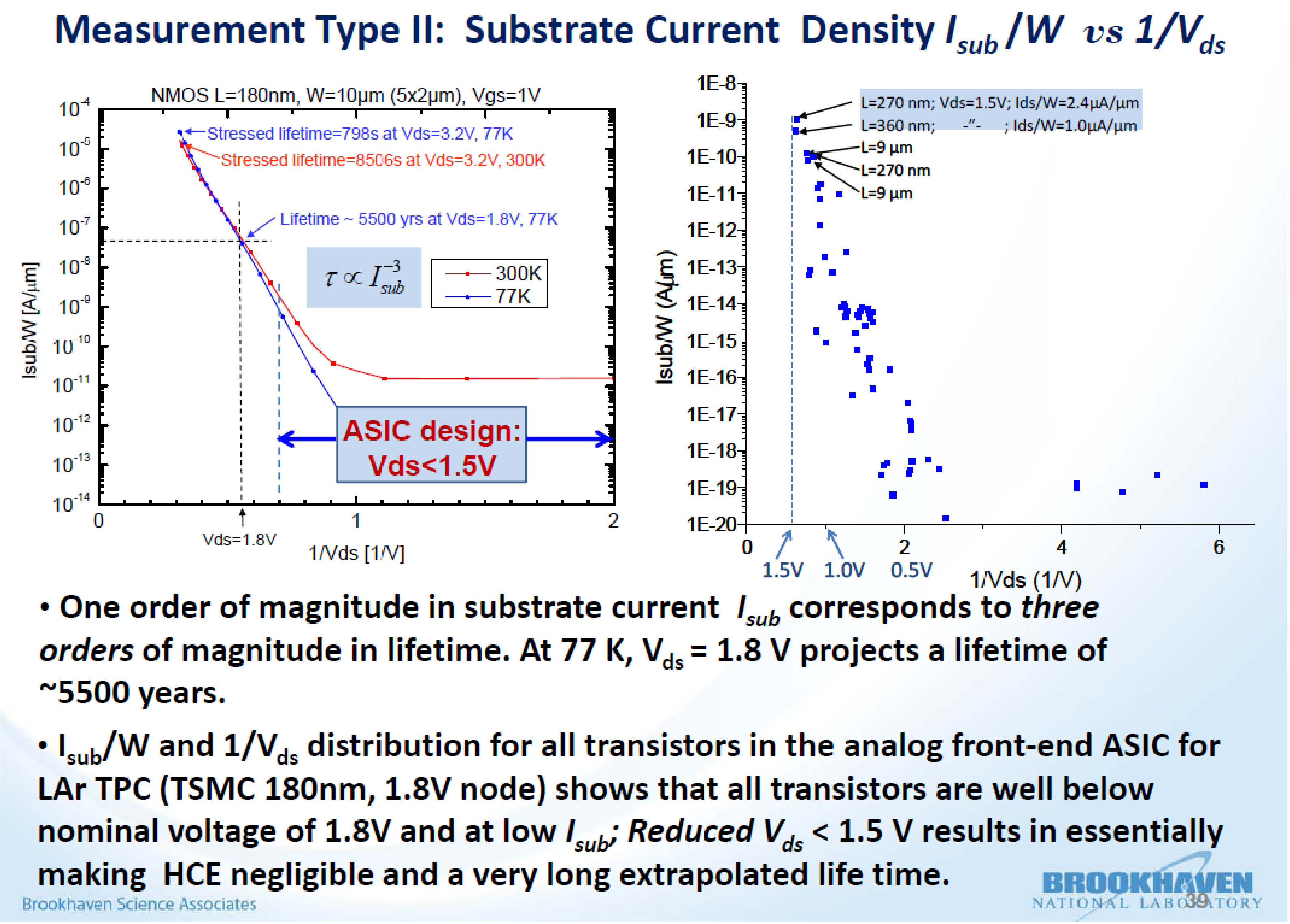
$$\ln\left(\frac{\tau I_{ds}}{W}\right) \propto \frac{\varphi_{it}}{q\lambda E_m} \propto \frac{1}{V_{ds}-V_{dsat}}$$

ASIC design: Vds<1.5V

- *If the measured points at both 300K and 77K are close to the characteristic slope for the interface state generation,* $a = \varphi_{it}/\varphi_i \approx 3$ *, it confirms that the degradation follows basic relations for interface state creation. Substrate current must be measured for this stress plot.*

- *The lifetime prediction plot (right) can be derived from the stress plot (left), or from direct measurements of* τ *vs.* V_{ds}*, without measuring the substrate current*

Appendix



Measurement Type II: Substrate Current Density I_{sub}/W vs $1/V_{ds}$

- One order of magnitude in substrate current I_{sub} corresponds to *three orders* of magnitude in lifetime. At 77 K, V_{ds} = 1.8 V projects a lifetime of ~5500 years.

- I_{sub}/W and $1/V_{ds}$ distribution for all transistors in the analog front-end ASIC for LAr TPC (TSMC 180nm, 1.8V node) shows that all transistors are well below nominal voltage of 1.8V and at low I_{sub}; *Reduced* V_{ds} < 1.5 V results in essentially making HCE negligible and a very long extrapolated life time.