Answers to the questions from the review committee

DUNE TPC Electronics ASIC Team
BNL, FNAL, LBNL
22 July 2021

Question #1

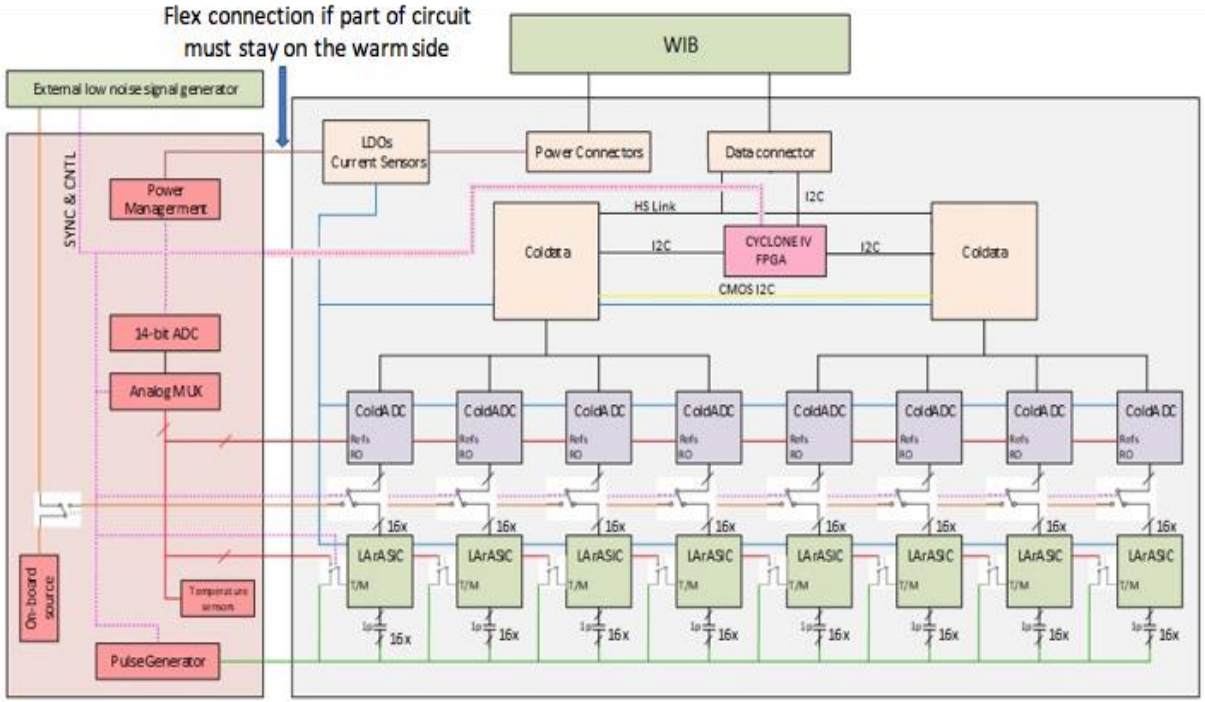
- A presentation of the QA/QC plan would be welcome. The plan is quite detailed in the document you posted in EDMS but we'd like to have more details about the actual tests you plan to do for the ERs and what could be the evolution for the production. We believe that the experience gained with ProtoDUNEII might allow simplification of the production tests after the full characterization has been done.

- Marco Verzocchi (FNAL)

ASIC QC Plan

- All ASICs to have a unique identifier on the package, COLDATA chips will also have E-fuses burnt during the QC process
- Plan on testing all ASICs both at room temperature and in LN_2 prior to installing them on the FEMBs
- All ASICs to be place into sockets by pick and place robotic system
- Test boards will be first at room temperature, then immersed in LN_2, then warmed up back to room temperature in a controlled way to prevent condensation / ice from forming on the ASICs/sockets (this is a source of damage)
- Test board design is inspired by FEMB design and by test boards used for ProtoDUNE and for initial testing of ASICs during their development

Test Board (i)



- Block diagram very similar to FEMB, but I2C/clock lines do not go straight to COLDATA (see next slides), are instead intercepted by FPGA
- Additional hardware on the test board (or on ancillary board) to perform functions that are needed during QC process

Test Board (ii)

- What is the purpose of the extra FPGA on the test card ?
  - On the FEMBs there is a primary COLDATA (LVDS I2C communication with the WIB, receives 62.5 MHz clock from the WIB, controls secondary COLDATA via CMOS I2C communication, controls 4 ColdADC and 4 LArASIC chips) and a secondary COLDATA (receives I2C via the relay from the primary COLDATA, controls 4 ColdADC and 4 LArASIC)
    - Don’t know at the time of QC whether COLDATA will be installed as primary or secondary on the FEMB, need to test them for both configurations
  - We need extra hardware (controlled via I2C) for measuring power consumption of individual chips, controlling switches that allow us to send external calibration pulses to LArASIC/ColdADC and which voltage references to send back to an additional ADC
  - With the additional FPGA we can expand the I2C address space and control / read out the extra hardware (switches, additional ADC, current monitors)

QC measurements – LArASIC (i)

1. Power on/off cycles (at least 5)
2. Measure power consumption in 3 rails (V_{DDP}, V_{DDA}, V_{DDO}) for 2 baselines * 3 configurations of output buffer
3. Measure bandgap reference voltage
4. Record voltage from internal temperature sensor
5. Check programming/readback through SPI interface
6. Use external pulser signal to check each channel is connected
7. Measure noise on each channel with 150 pF capacitive load (14 mV/fC gain, 8 combinations: 2 baselines * 4 shaping times)
8. Measure pedestal and check that there isn't large dispersion (initially do all 128 combinations: 2 baselines, 4 gains, 4 shaping times, 4 bias currents, then reduce the number of combinations)

QC measurements – LArASIC (ii)

9. Measure linearity and gain of the amplifier using external pulse (min 14 bits), then repeat with internal DAC (6 bits). Perform the measurements with a limit number of settings (2 baselines, 2 shaping times, 2 gains, 1-2 bias currents). Calibrate internal pulser
10. Make measurement of internal calibration capacitor relative to known external calibration capacitance

Perform the entire sequence first at room temperature, then in LN_2

Chips failing tests at room temperature will not be tested in LN_2

QC measurements – ColdADC (i)

1. Power on/off cycles (at least 5)
2. Measure power consumption in 4 rails (V_{DDA2P5}, V_{DDD2P5}, V_{DDD1P2}, V_{DDIO})
3. Test I2C communication with chip
4. Test chip starts up in appropriate state after reset
5. Perform autocalibration procedure
6. Use sine wave from external generator with frequency of 150 KHz and amplitude of 1.45 V to verify all channels are functioning
7. Measure frequency of ring oscillator

Tests 1-7 are performed first at room temperature, then in LN_2

Following tests are performed in LN_2 only

QC measurements – ColdADC (ii)

Measure reference voltages for BGR and CMOS reference block

8. Determine dynamic range / check overflow is working with 2V sine wave or slow ramp
9. Make ADC performance both with single ended / differential input (determine INL, DNL, ENOB, noise) using 150 KHz sine wave (amplitude 95% of dynamic range). Use 14 bits readout, no offline non-linearity corrections
10. Measure cross-talk on a subset of the ASICs

Determine acceptance criteria at a later date (these may include checking calibration parameters, but not their stability, will test some reference chips several time, but cannot measure every chip multiple times – final calibration constants will be obtained from FEMB testing)

QC measurements – COLDATA (i)

1. Power on/off cycles (at least 5)
2. Measure power consumption in 5 rails (V_{DDIO}, $V_{DD\_LArASIC}$, V_{DDCORE}, V_{DDD},V_{DDA})
3. Test I2C both on LVDS lines and CMOS lines
4. Test chip starts up in appropriate state after reset
5. Assign (and read back) unique identifier by burning eFuses
6. Check clocks sent to ColdADC (62.5 MHz, 1.953125 MHz, check 32:1 ratio, check jitter)
7. Checking tuning parameters for PLL
8. Verify Fast Commands (Reset, Edge, Sync, Act)
9. Check data transmission to the WIB (data formats, eye diagram)
10. General purpose I/O bits on the FEMB

All measurements to be repeated in LN_2

Exact acceptance criteria will be defined after testing a sizeable number of ASICs from the engineering run

QC measurements – FEMB level

Many of the tests mentioned above for LArASIC/ColdADC are part of the calibration suite used at the FEMB level (both at room temperature and in LN_2)

The WIB will have the capability of sending a high precision calibration signal to the FEMB. That signal is input into LArASIC and can be used to verify (or derive) the offline correction (based on INL)

QC measurements – time required

Testing cycle:

- test at room temperature
- purge the volume containing the test board with gaseous N2
- fill with LN_2
- cold test
- warm up in a controlled way to avoid condensation

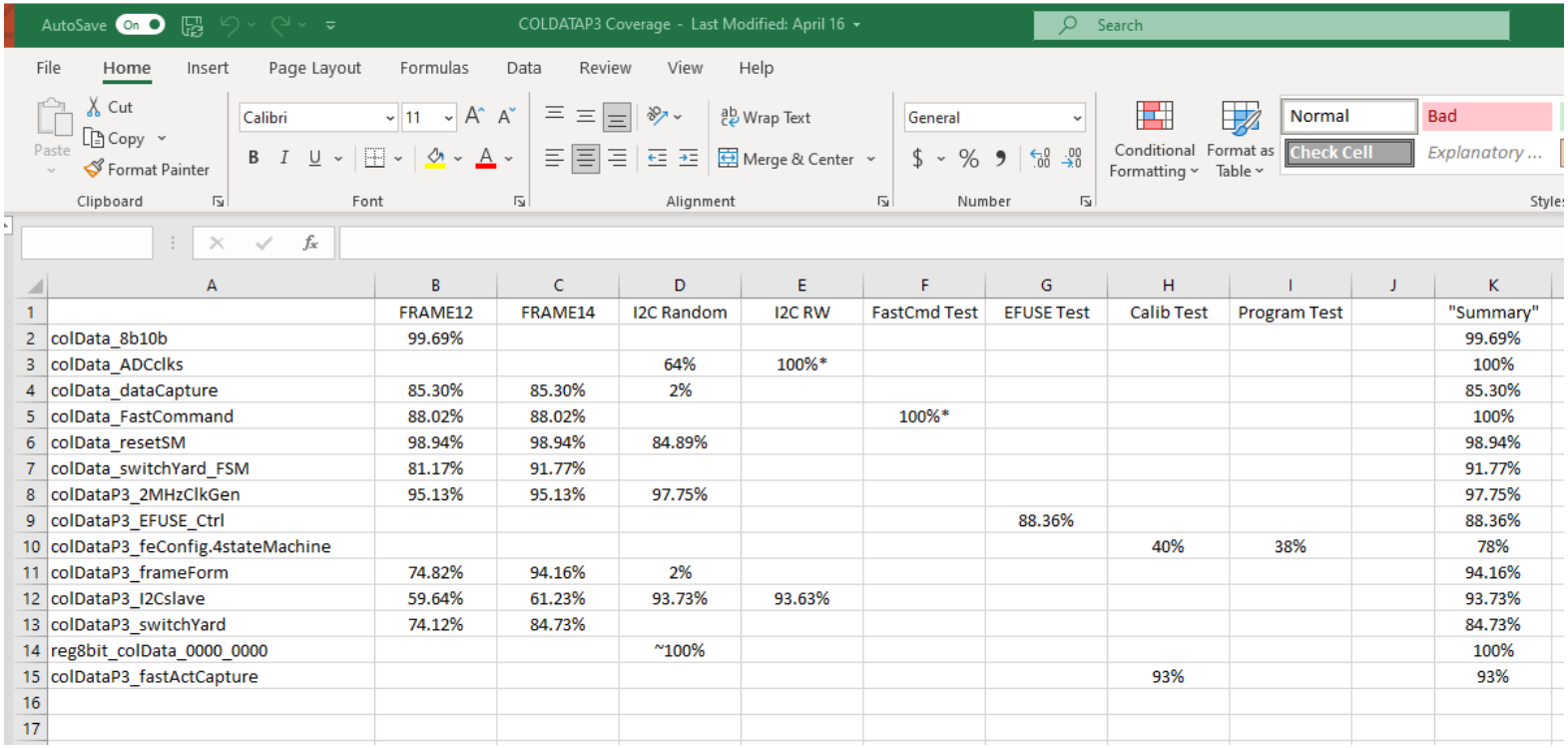
- Based on past experience the cycle time is driven by the cool-down / warm-up cycle
- We believe this can be done in about 90 minutes, will validate this assumption in 2022
- We need a total of 11 test sites (2 for each flavor of ASIC + 5 for the FEMBs) to keep the QC time in the 2.5 years range mentioned yesterday

Question #2

- The following points for COLDADC and COLDATA should be clarified:
  - Is there an estimation of the coverage that was achieved in simulation.
- Jim Hoff (Fermilab),
  - What is the IR drop that they have on the chip. In case it is marginal, it could affect the yield. TSMC specify that the static IR-drop in should be < 3% of VDD, and the dynamic < 15% of VDD. If it is a bit higher but controlled, it can be ok but it would be good to know.
- Sandeep Miryala (BNL) (only for ColdADC, we did not run IR drop analysis for COLDATA because there we did not observe any problem related to IR drop in first full prototype COLDATA p2)

COLDATAP3 Toggle Coverage

- Determining Functional Coverage of COLDATA was not a priority in the project. It is only in the more recent projects like CMS's ECON-T and ECON-D that Functional Coverage has been stressed. Therefore, Functional Coverage information is simply not available for COLDATAP3 (or earlier).
- Toggle Coverage asks the simple question "was this bit flipped?". It is easier to assemble and so I can provide the following data for COLDATAP3.
- I'm afraid that even Toggle Coverage is not available for COLDADC because we did not store that information in the databases.



	A	B	C	D	E	F	G	H	I	J	K
1		FRAME12	FRAME14	I2C Random	I2C RW	FastCmd Test	EFUSE Test	Calib Test	Program Test		"Summary"
2	colData_8b10b	99.69%									99.69%
3	colData_ADCclks			64%	100%*						100%
4	colData_dataCapture	85.30%	85.30%	2%							85.30%
5	colData_FastCommand	88.02%	88.02%			100%*					100%
6	colData_resetSM	98.94%	98.94%	84.89%							98.94%
7	colData_switchYard_FSM	81.17%	91.77%								91.77%
8	colDataP3_2MHzClkGen	95.13%	95.13%	97.75%							97.75%
9	colDataP3_EFUSE_Ctrl						88.36%				88.36%
10	colDataP3_feConfig.4stateMachine							40%	38%		78%
11	colDataP3_frameForm	74.82%	94.16%	2%							94.16%
12	colDataP3_I2Cslave	59.64%	61.23%	93.73%	93.63%						93.73%
13	colDataP3_switchYard	74.12%	84.73%								84.73%
14	reg8bit_colData_0000_0000			~100%							100%
15	colDataP3_fastActCapture							93%			93%
16											
17											

IR Drop Analysis on ColdADC P2 – Voltus-Fi

Sandeep Miryala & Grzegorz Deptuch

Brookhaven National Laboratory (BNL)

BROOKHAVEN NATIONAL LABORATORY

U.S. DEPARTMENT OF ENERGY

Fermilab DUNE

Motivation

- IR drop observed in COLDADC P1 testing
  - At RT power supply voltage needed to be increased by ~200mv to operate
- Tools
  - Voltus: IR drop analysis for digital dominant designs
  - Voltus-Fi: IR drop analysis for analog designs,
    Transistor level simulations for power analysis for analog block
    grid modelling
    Embedded in Virtuoso Analog Design Environment (ADE)
- What IR analysis has been done using Voltus-Fi
  - Performed on supply nets of COLDADCP2 analog top macro (SDC + ADC0 + ADC1 + CMOS BIAS) using Cadence Voltus-Fi
  - Performed for RT, LNT not done, but as a rule resistances of metal traces will be ~5 times less resistant at LN2T than at RT

Design Input Data Requirements

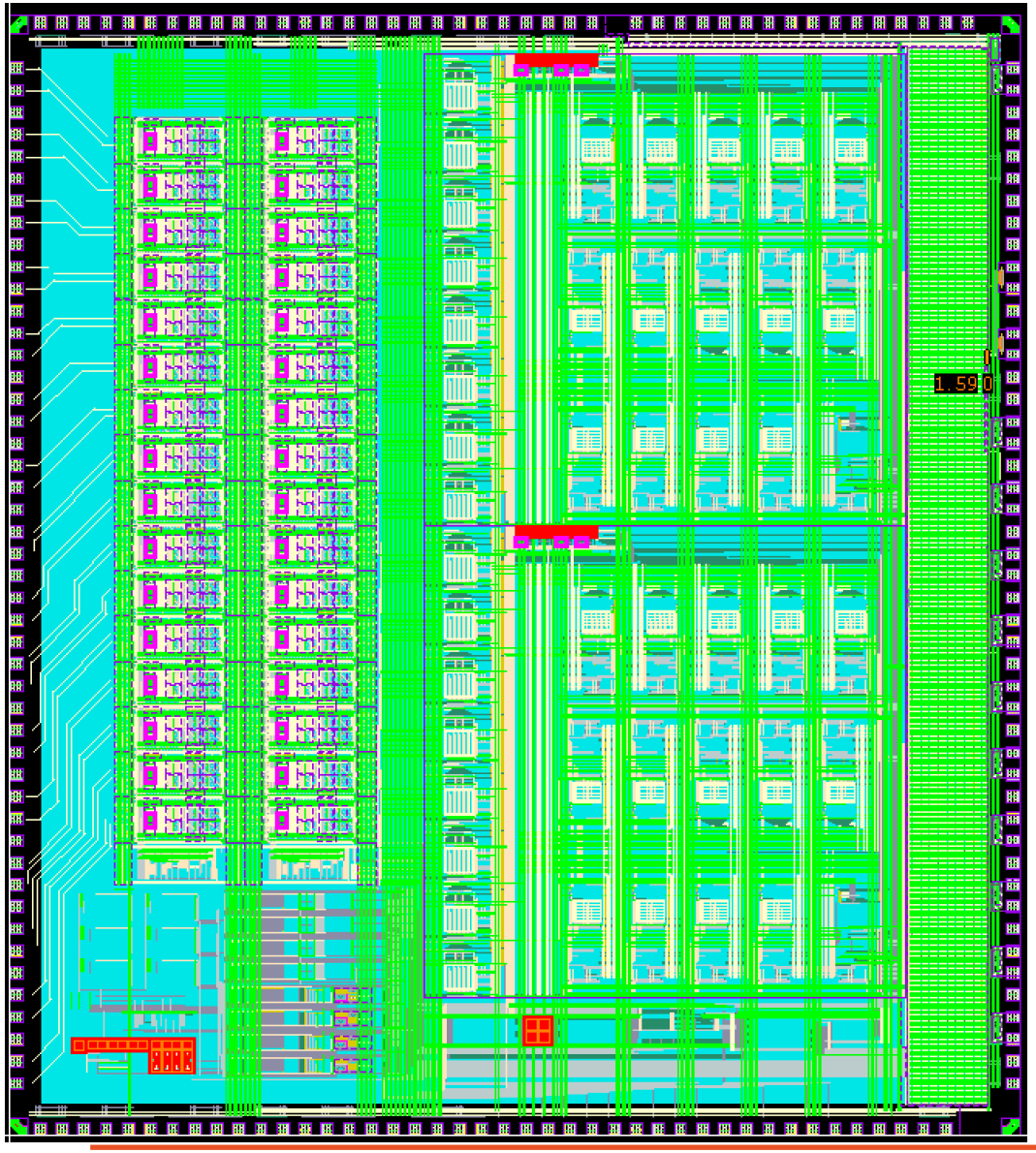
- **Design Data**
  - xDSPF of the design
    - Decoupled RC extracted for all nets, including PG nets
    - With physical information for layers
  - Testbench schematic or netlist
  - DFII schematic for Virtuoso® Analog Design Environment based simulation
  - DFII layout for results visualization and structural checks or GDSII of the design with layer map to pipe it in Virtuoso platform
- **Technology Data**
  - SPICE models and corners
  - DFII technology library
  - ICT file or qrcTechFile with EM models

Extracted using Quantus QRC

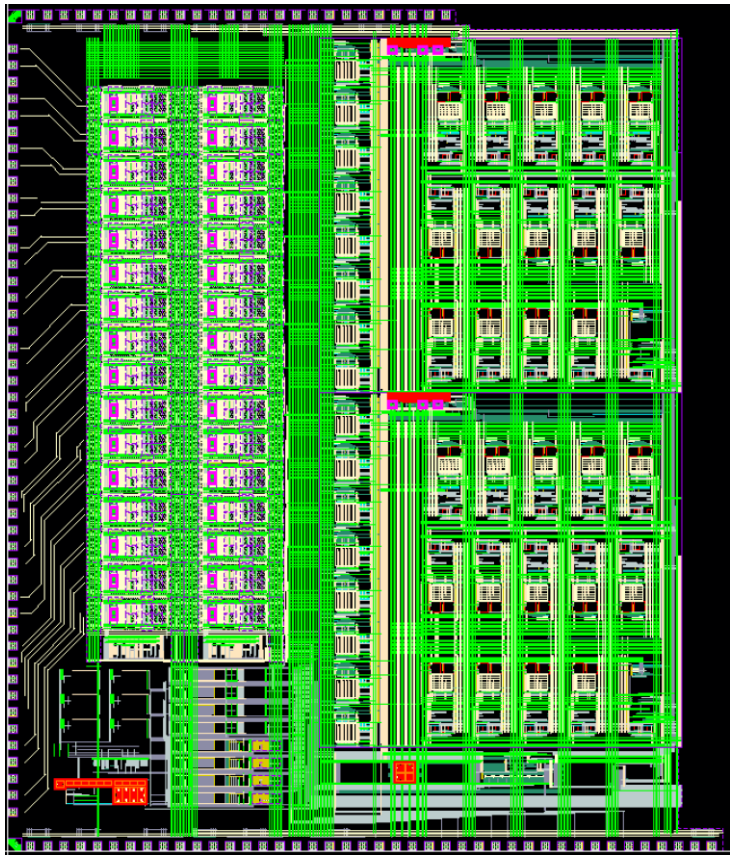
LBL provided testbench, schematic and layout

From 65nm PDK

COLDADCP2_CHIP



COLDADCP2_Analog_Top

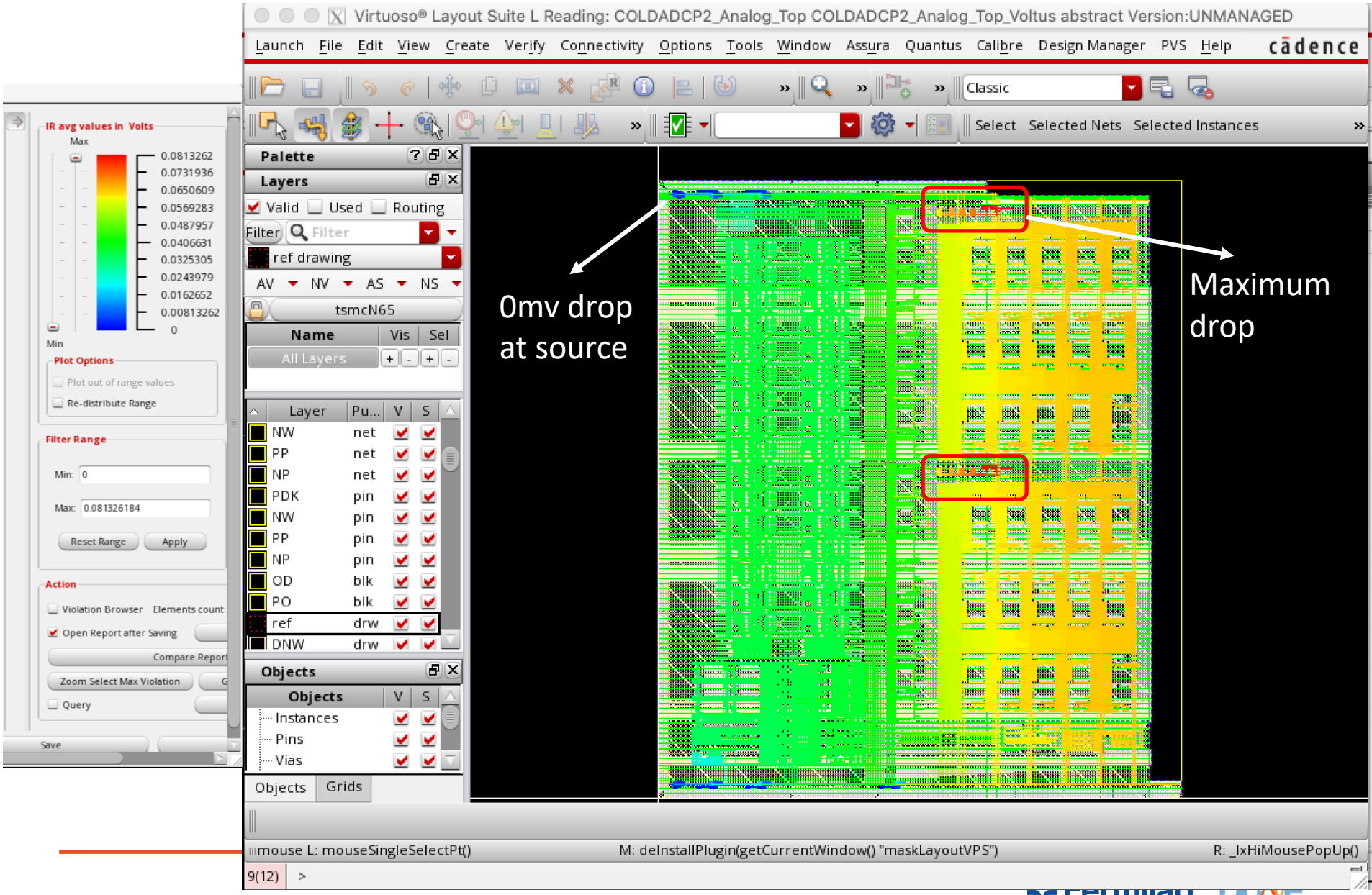


Simulation Information

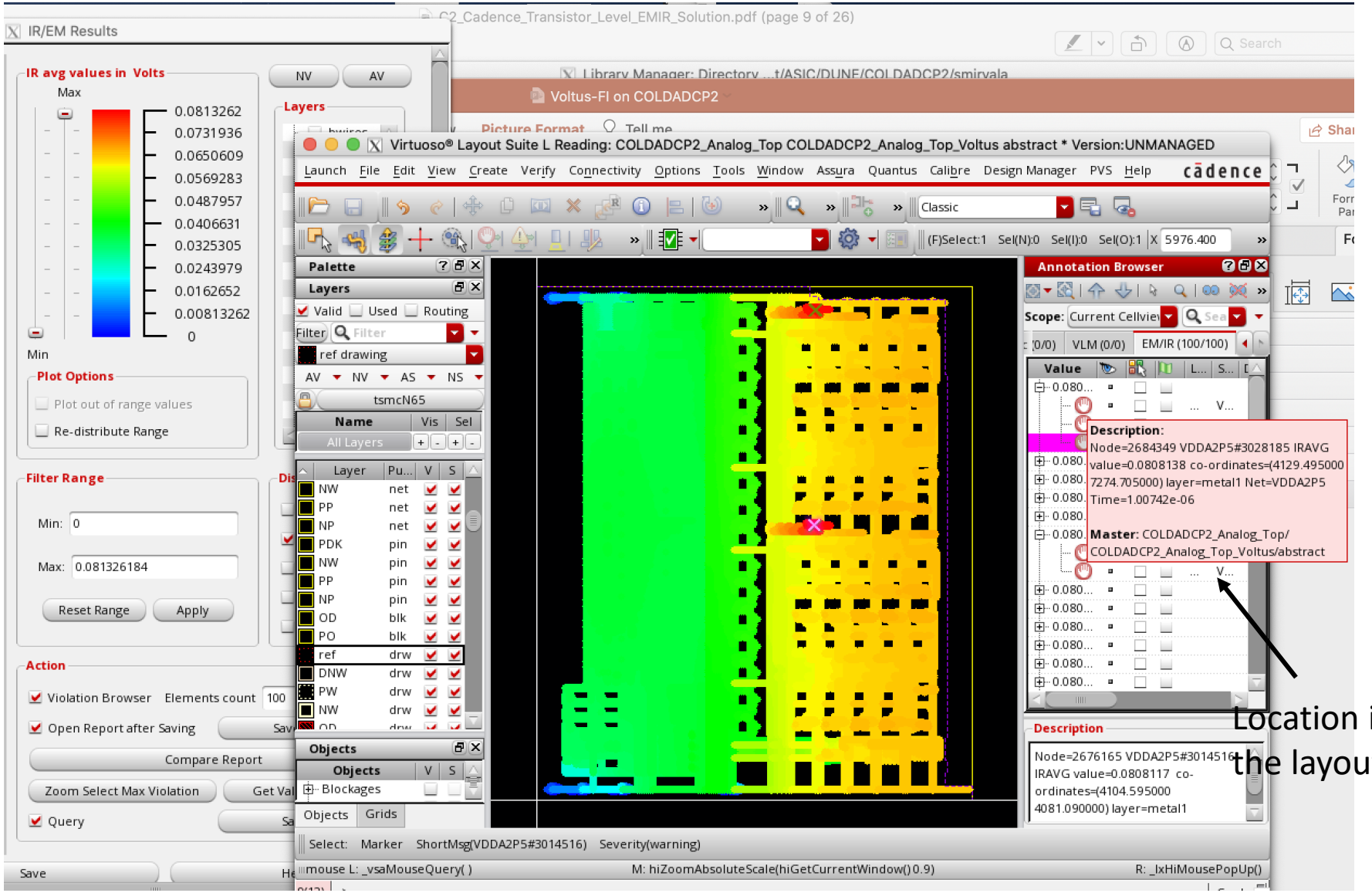
- Simulation time 0 to 1.1us
  - Selected APS and Iterated solver options
- EMIR analysis window 1us to 1.1us
  - Selected only analog supply and ground
  - ~2hr to analyze each power net
- DSPF information
  - ~6hr to generate DSPF

```
Element Inventory:
     Element     :     Total Number       Min Value        Max Value
     Net         :           215792       NoTaps:184476  NoEffectiveRes:191
971
     Nodes       :         23745198
       *|I       :          1628272
       *|P       :              717
       *|S       :         21900417
     Instance    :           548010
     Resistor    :         33992126          0.0001           3368.3
     Capacitor   :          8800495       1.007e-23       4.1257e-11
```

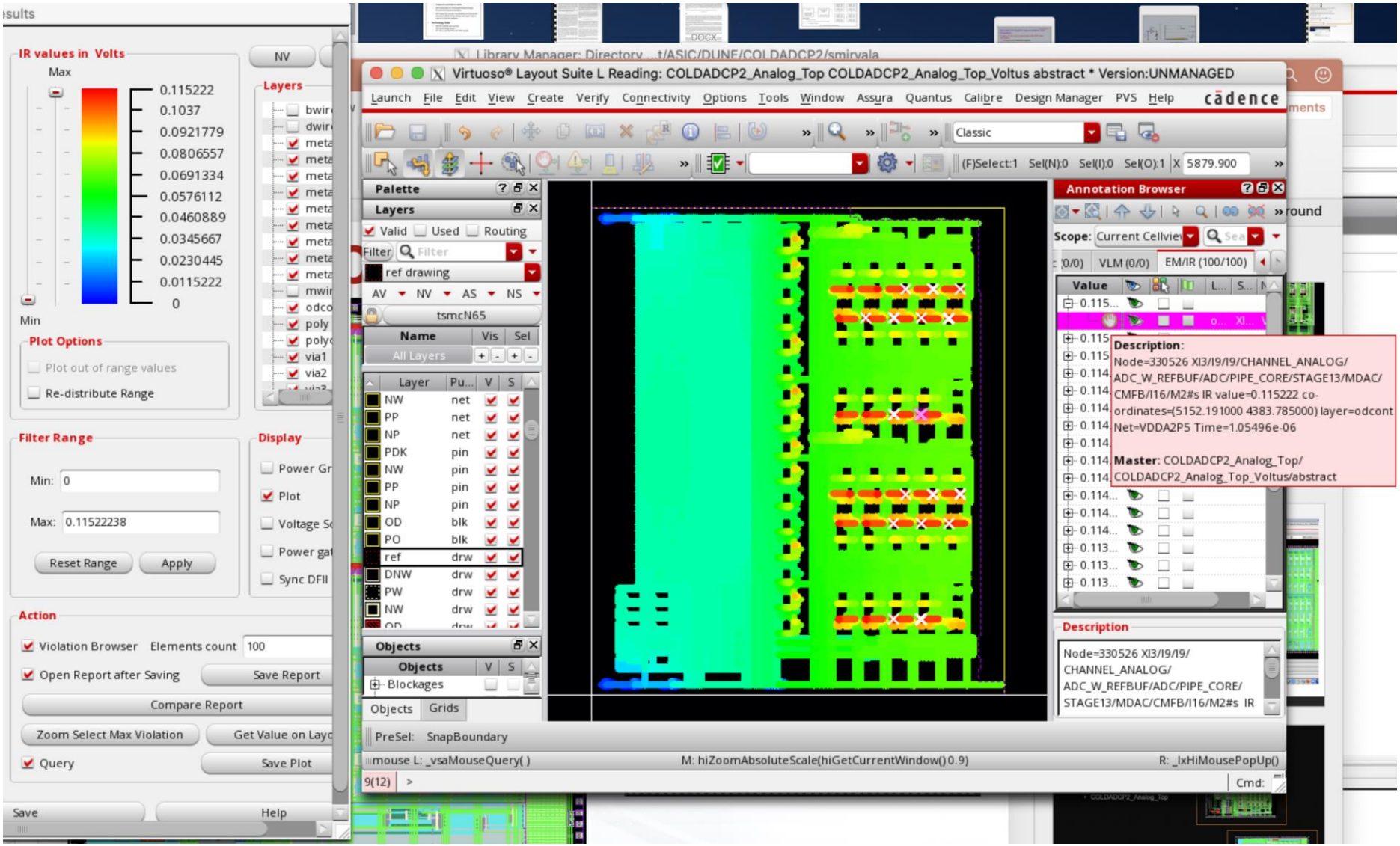
VDDA2P5 power supply net (Avg)



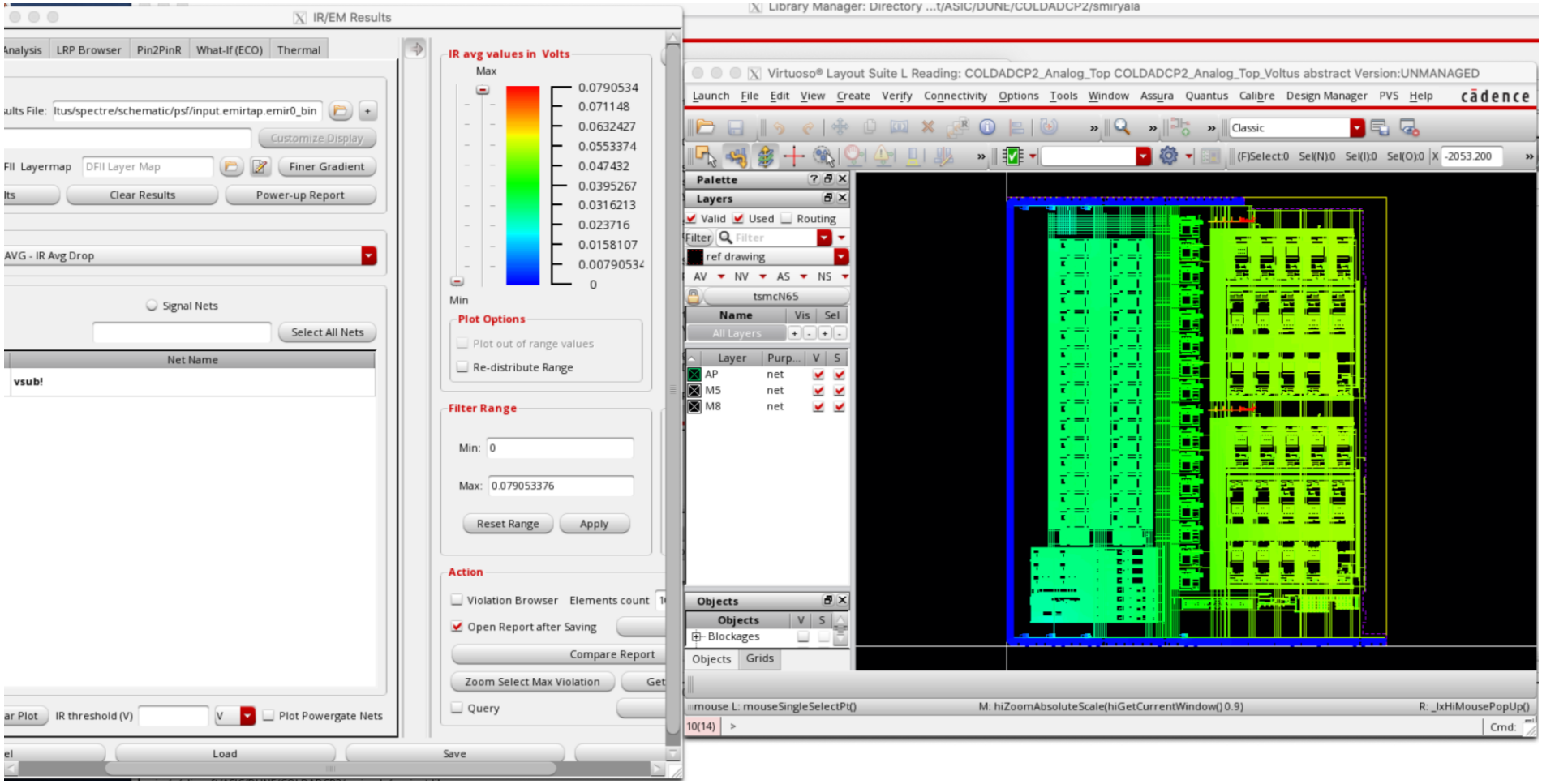
Location and Instances



Peak Drop and Instances



Vsub! Ground net (Avg)

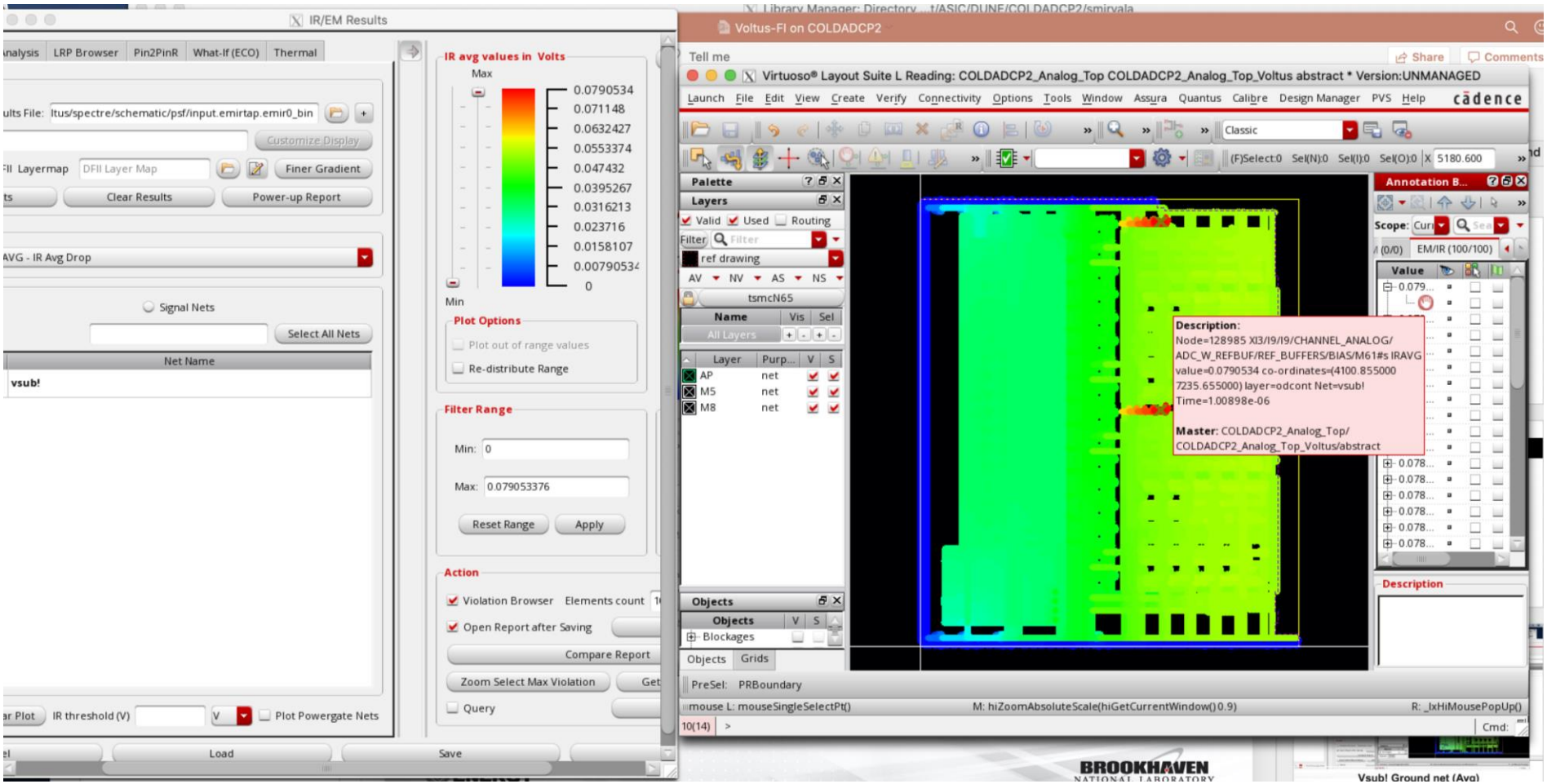


80 mV on VDDA2P5 + 80 mV on Vsub! = ~160 mV

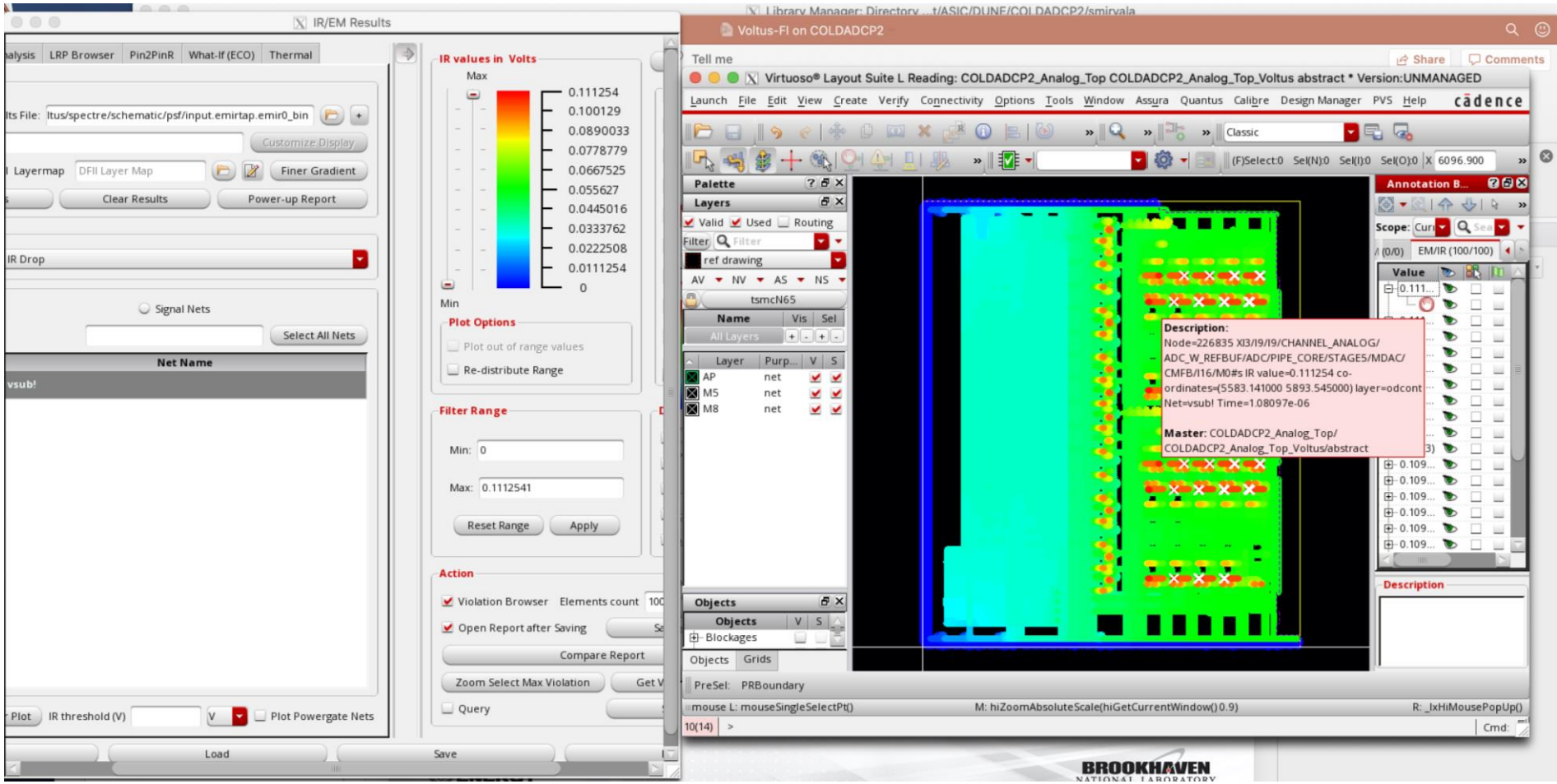
% IR drop = ~160mV/2.25V = ~7 %

Fermilab DUNE

Location and Instances



Peak Drop on Vsub!



Question #3

- On the full chain test (LArASIC p5 and COLDATA P2) are there any "simple" tests that confirm ADC functionality? It's understood that full characterization is not possible, but was it possible to confirm e.g. digital signals were produced, current drawn was as expected? Will full tests of LArASIC+COLDATA be possible in the FEMB?

- Shanshan Gao (BNL)

Question #3 - Answer

- Many simple tests of ColdADC can (and will) be performed again at the FEMB level
  - Power consumption (measure sum of all the ColdADC on a FEMB from the WIB)
  - I2C communication / resets
  - Can send out known analog pattern to check synchronization
  - Can send out known test pattern to check data transmission
  - Can monitor reference voltages for one ColdADC out of 8 on the FEMB
  - While we cannot do the ultimate characterization of the ADC on the FEMB, we want to investigate how precisely we can measure the full chain response using an external pulse (and use this procedure for the offline INL correction)

Question #4

- For the ADC specification and QA/QC, the documentation is good, but it may be useful to the team to add specs for clock jitter, supply voltage PSRR, calibration stability, acceptable calibration values, time needed to calibrate (it was said it is fast, but what is fast), eye opening. This could be used to refine QC plan, i.e. put thresholds on some parameters to accept/reject chips.

- Carl Grace (LBL)

Jitter specification

- Jitter Specification:

  The jitter in the ADC clock and limit the SNDR

  SNR (dBFS) < $-20\log(2\pi f_{in}\sigma)$, where fin is the maximum input frequency and σ is the rms clock jitter.

  For a 12-bit ADC, the ideal SNDR is about 72 dB and max f_{in} = 410 kHz (LArASIC BW with 0.5 µs shaping time)

  Solving for σ we have **rms jitter must be < 97.5 ps**

Shaping Time [µs]	Bandwidth [kHz]	Jitter spec [ps-rms]
0.5	410	97.5
1	216	185
2	110	363
3	73	548

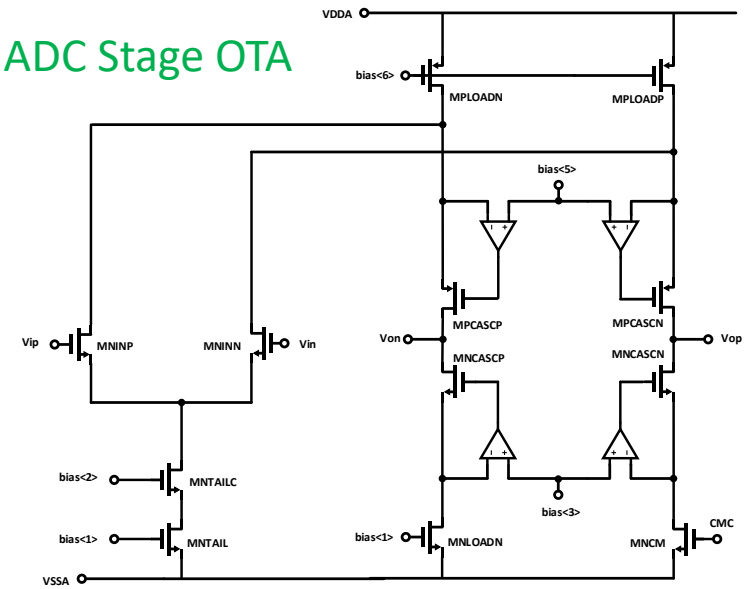
Question 4 Response (cont)

- PSRR Requirement:

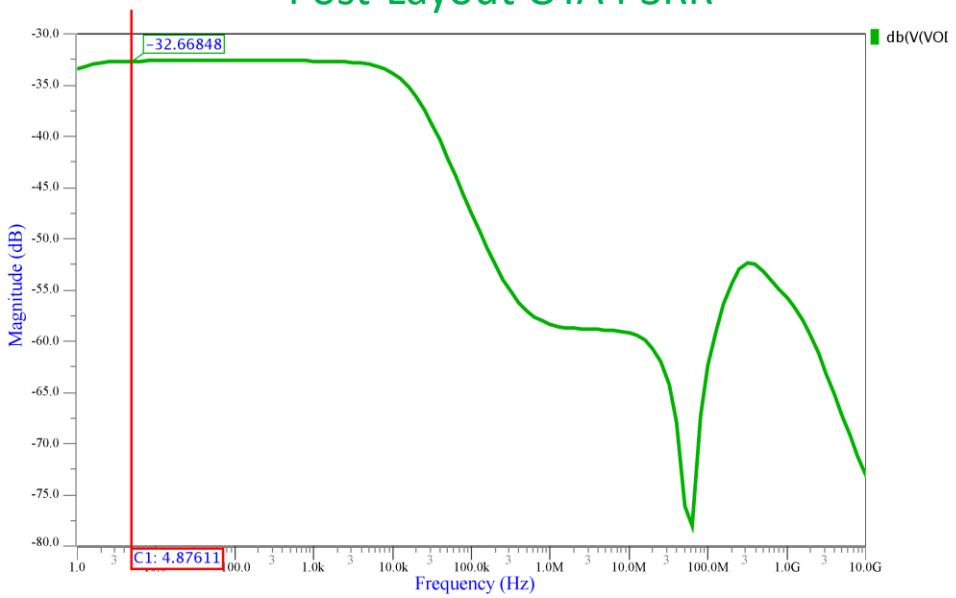
  ColdADC_P2 uses a fully differential analog signal path and is highly resistant to power supply interference.

  The most sensitive circuit is the ADC Stage OTA as it has less filtering than the reference buffers, so will have the worse PSRR

ADC Stage OTA



Post-Layout OTA PSRR



Question 4 Response (cont)

- PSRR Requirement (cont):

As shown in the extracted post-layout R+C+CC simulation, the low-frequency PSRR of the OTA is -32 dB or about a factor of 40.

We want to limit PSRR errors to approximately ¼ LSB. One LSB in ColdADC is 3 V / 4096 = 732 µV, so ¼ LSB is 183 µV.

Given the PSRR of the OTA, a low-frequency power supply perturbation of approximately 183 µV * 40 = 7 mV-rms. Therefore, the power supply rail should be stable to about 7 mV-rms (a quite relaxed specification).

We did not observe any errors attributable to power supply ripple or noise in the tests done at LBL. The power supply we are using in testing, the BK Precision 9129B power supply has noise < 1 mV-rms and ripple < 5 mV pp (1.8 mV-rms). Between the power supply and the ASIC we have 1 DC-DC converter (LMZ14203, ripple 8 mV pp), followed by an LDO (TPS74201, > 30 dB suppression above 20 KHz)

Question 4 Response (cont)

- PSRR Requirement (cont):

We have not done the same measurement with the full chain (Wiener PL506 → PTC → WIB → FEMB → ColdADC). In this case there are multiple DC-DC converters plus two LDOs in the power distribution chain. The last DC-DC converter has a ripple in the 5-10 mV pp range and it is followed by one LDO on the WIB (TPS74401) and one on the FEMB (TPS74201). Each LDO provides a 30 dB suppression above 20 KHz. The FEMB should be even less sensitive to voltage ripples on the power supplies.

Note: this is a settling requirement (not a maximum excursion requirement). If the ColdADC_P2 power supply is kicked by the clock (for instance) as long as it settles to within 7 mV of its nominal value (2.25 V) before sampling the error will be bounded by ¼ LSB.

Question 4 Response (cont)

- Calibration Stability
  - Chip to chip

    The calibration algorithm averages up to 2^{16} samples when calibrating coefficient weights. It is expected to be stable to within a few LSBs for the 1st and 2nd stage. After that, it should be highly stable.

    We are not ready yet to set an exact value of the specification to be used during the QC to identify flaky ADCs (we did not observe one like this during testing, but it is possible due to damage during processing).

  - Vs time

    We are not going to run the QC procedure twice at a distance of days / months before installing the chips on the FEMBs. We will be able to identify chips that have significant variations only when making the 2nd test at the FEMB level (this would require reworking FEMBs)
    In the limited testing done so far calibrations were stable vs time

Question 4 Response (cont)

- Calibration Time

  In its nominal configuration (and best practice) the calibration algorithm averages 2^{16} per measurements when calculating coefficient weights. There are 2 weights per stage, 2 measurements per weight (e.g. S0 & S1), and 7 calibrated stages.

  Therefore, ignoring a small amount of overhead, calibration requires $2*2*7*2^{16}$ or approximately 2M samples. Since the sampling rate is about 16 MS/s, each ADC takes about 125 ms to calibrate.

  It is best practice (to minimize digital activity) to calibrate one ADC at a time. In this case, a full ColdADC_P2 calibration would take 0.25 sec or actual calibration time plus however long it takes the test system to issue 4 slow control commands (2 calibrate and 2 stop calibrating commands), which is of the order of 40 µs. Overall calibration time may be dominated by control software.

  See the slides on the QC program for the time required to fully characterize a chip (this is expected to be in the 15-30 minutes)

Question 4 Response (cont)

- Eye Opening (64 Mb/s ColdADC to COLDATA communication)

  The LVDS drivers operation speed is very relaxed relative to the capabilities of the 65 nm process. We experienced no issues whatsoever with LVDS eye opening.

  The LVDS drivers on ColdADC_P2 will easily surpass the eye opening mask spec of any commercially available LVDS receiver (including embedded FPGA receivers), especially since the physical communication length is small.

- Eye opening (1.25 Gb/s COLDATA to WIB communication)

  So far measured at warm, eye opening increases when the cables are cold. Will perform measurements and establish acceptance criteria (to be measured during the QC process for COLDATA)

Question #5

- The simulation documentation shows very nice expected performance. What is the level of these simulation (schematic/layout? extracted R+C+CC?)? Are the results in Fig. 12 of the document on simulation of the ColdADC, for example, a full chip, transistor-level simulation? Is the input network simulated? Are there plans for additional simulation after submission?

- Carl Grace (LBL)

Question #5 Response

Most of the simulations showing circuit performance were done with extracted R+C+CC layout. Several of the “system level” simulations were made using an analytical model of the ADC and calibration algorithm in MATLAB

The input network was included (a simple model representing LArASIC’s output impedance) for the SHA simulations.

The simulation level for the various figures in the Simulation Document are captured on the next slide. There are no plans for further simulation.

Question #5 Response

- Summary of Simulation Level
  - Document: *ColdADC – Expected Performance from Simulation*

Figure(s)	Simulation Level	Comments
3	R+C+CC	SHA Functional Sim
4	Schematic	SHA switch on-resistance
5	R+C+CC	SHA Linearity
7	RTL	Clock phase generation
8	Schematic + Verilog-AMS	Bottom plot Verilog-AMS model
10	Schematic	ADC functionality
11	Schematic + RTL	Calibration functionality
12 & 13	MATLAB model	Expected performance (analytical)
16,17,20,23-25,29	R+C+CC	Block simulations
26 & 28	Schematic	Block Simulations

Question #6

- Concerning the tests done with the new prototype FEMB, were there injections on each channels ? Do you have a plot showing uniformity of response along channels

- Shanshan Gao (BNL)

Question #6

- Independent signal injection on each channel
  - Each FE channel can be calibrated independently. The test pulse can come either from outside of LArASIC or from the on-chip pulse generator. Each channel has a ~185fF calibration capacitor. There is one control bit for each channel to turn on/off the analog switch. By checking both with the internal pulser and with the external signal we can check for broken signal connections (packaging problems)
  - We can also detect broken connection via noise measurements when using the test load of 150 pF (see less noise if the connection is broken)

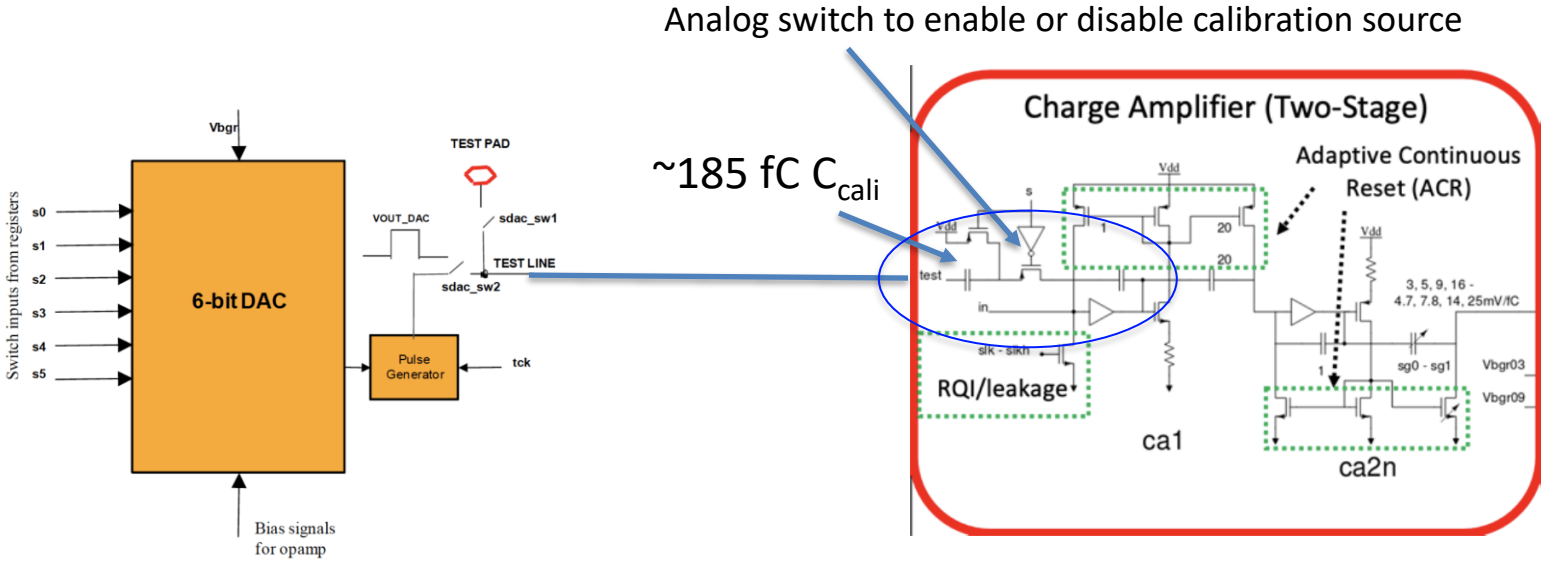
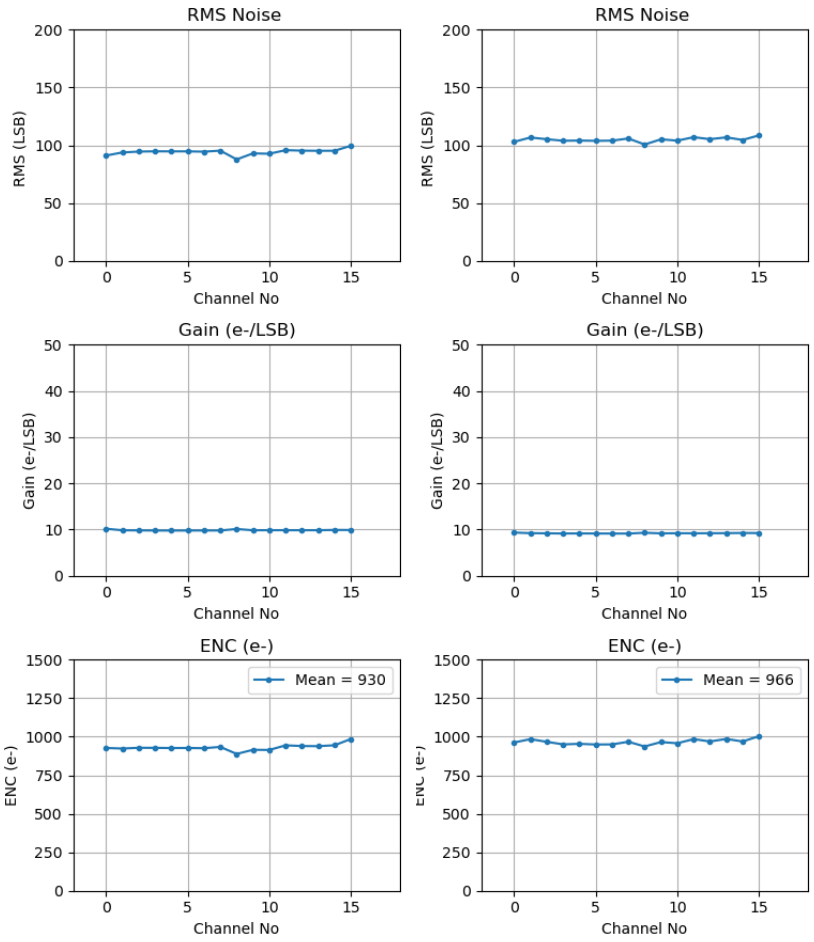


Fig. 14. On-chip DAC and pulse generator

Question #6

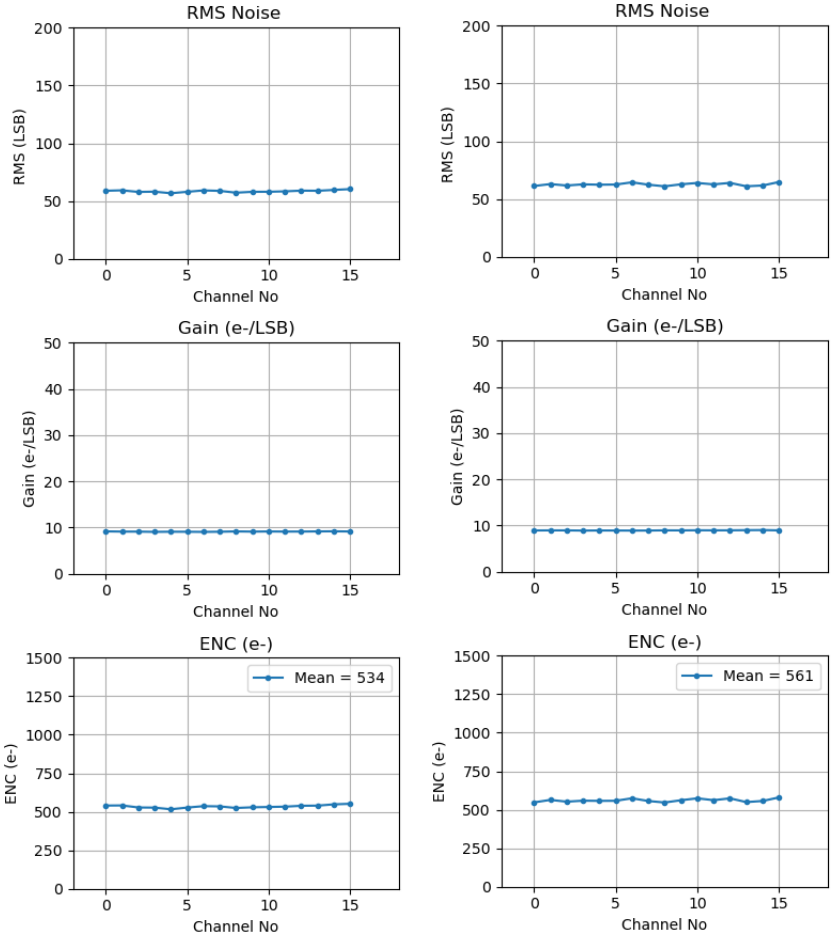
- Uniformity of response along channels
  - A full chain test done with test card with LArASIC p5 and ColdADC p2 (measurement in progress with FEMB)

single-ended | Differential



Measurement at RT

single-ended | Differential



Measurement at LN2