SiPM ganging

VD-PDS

DUNE VD PD workshop - July 26th, 2021

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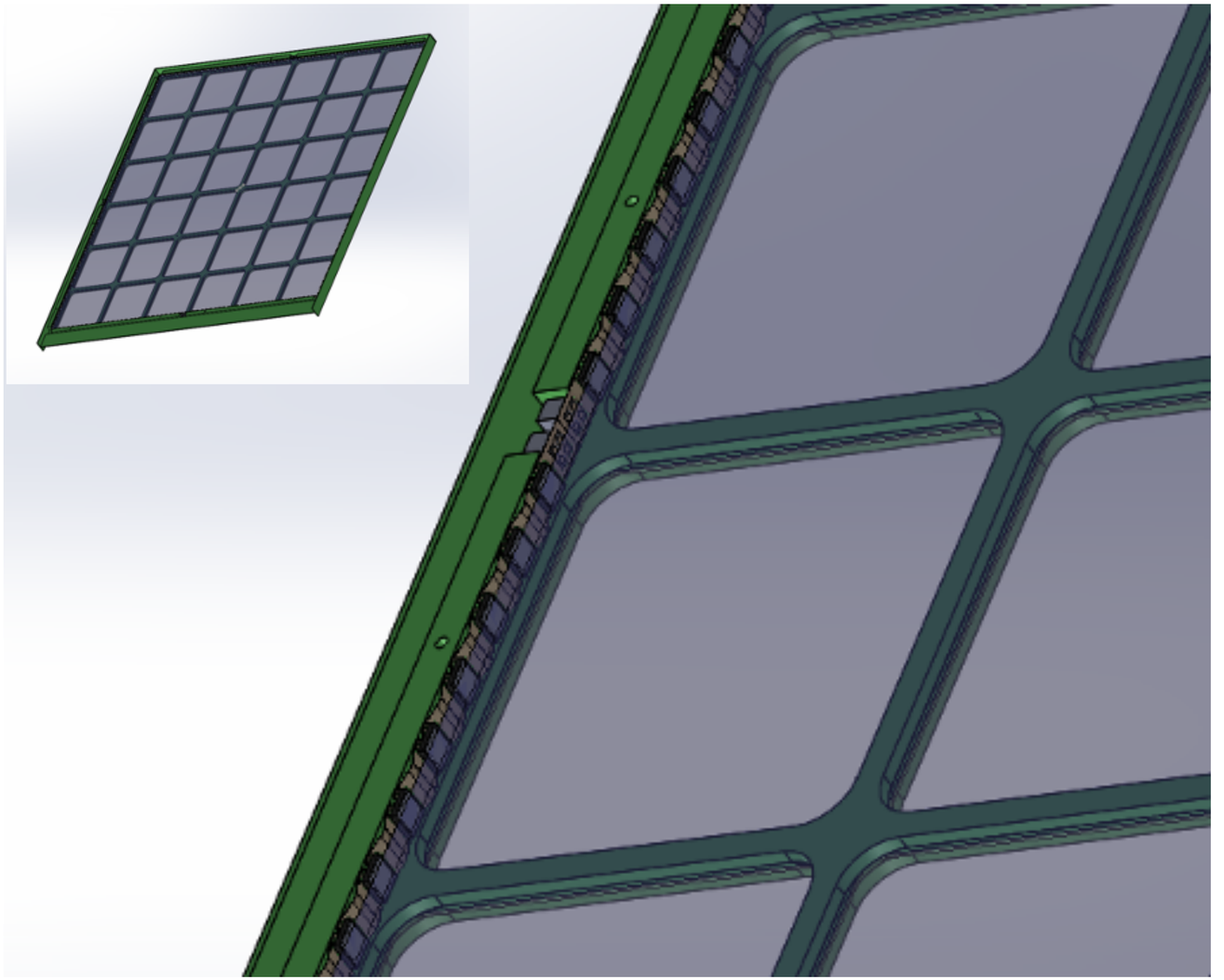
X-ARAPUCA tile

- Each X-ARAPUCA tile is populated with 160 SiPMs
- Organized in 8 groups of 20 SiPM.
- The 20 SiPM are passively summed in “hybrid" mode.
- The 8 groups then are summed in an active summing stage, using an OpAmp.



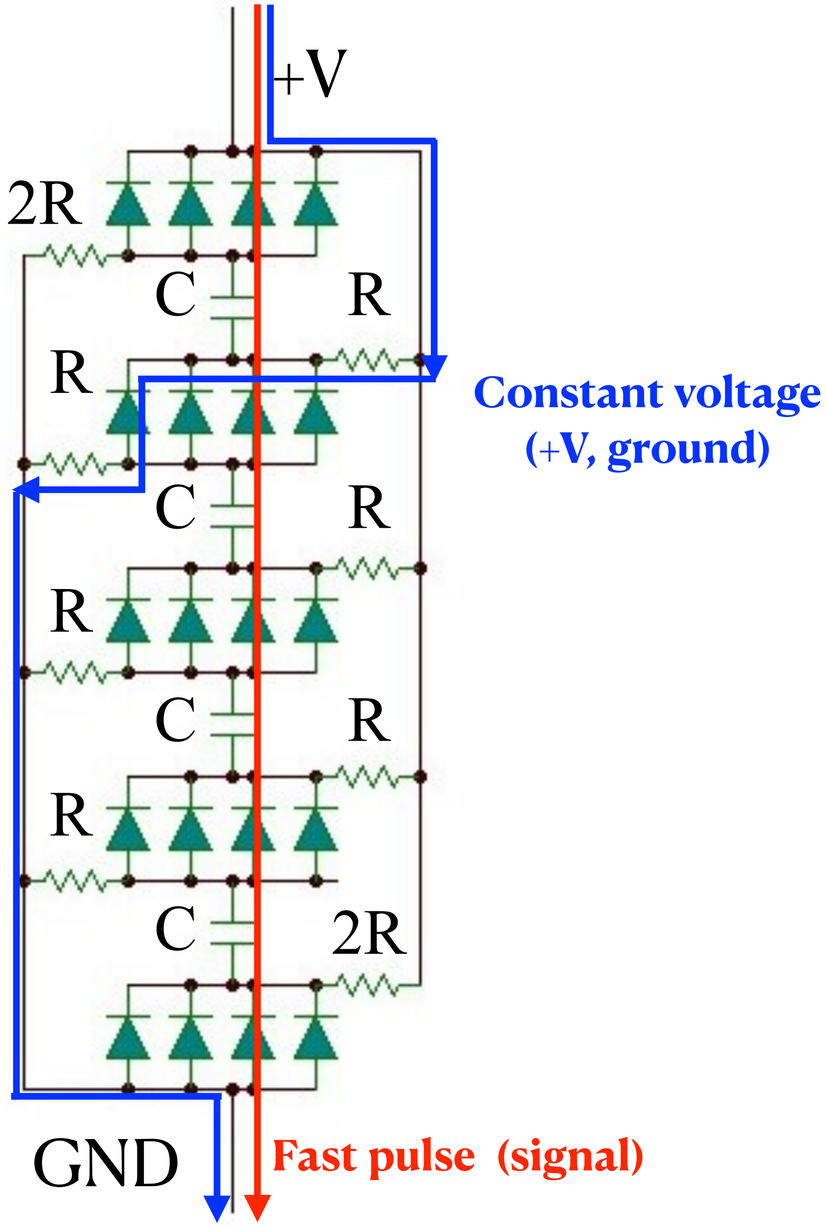
Hybrid circuit

The hybrid connection advantages:

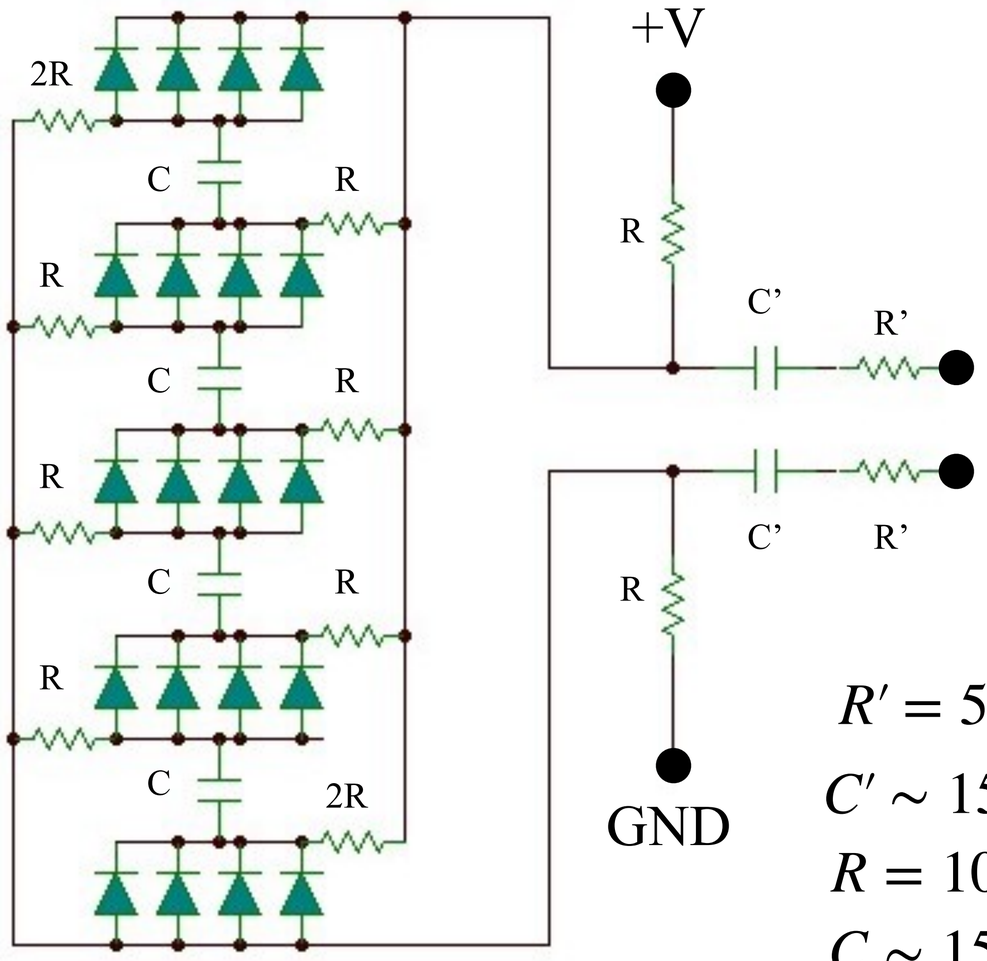
- Same potential on the surface of SiPM's.
- Small capacitance → short recovery time
- Same bias voltage of a single SiPM

DC current SiPM+2R ($R = 10\,k\Omega$).

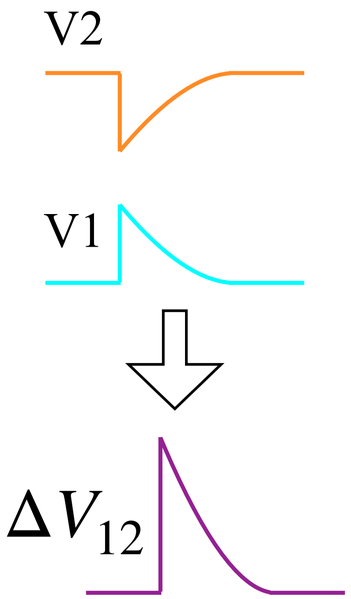
AC current SiPM + C ($C = 10\,nF$)



The 160 SiPM's from each X-ARAPUCA tile are arranged in 8 subgroups of 20 SiPM passively connected in "hybrid mode".

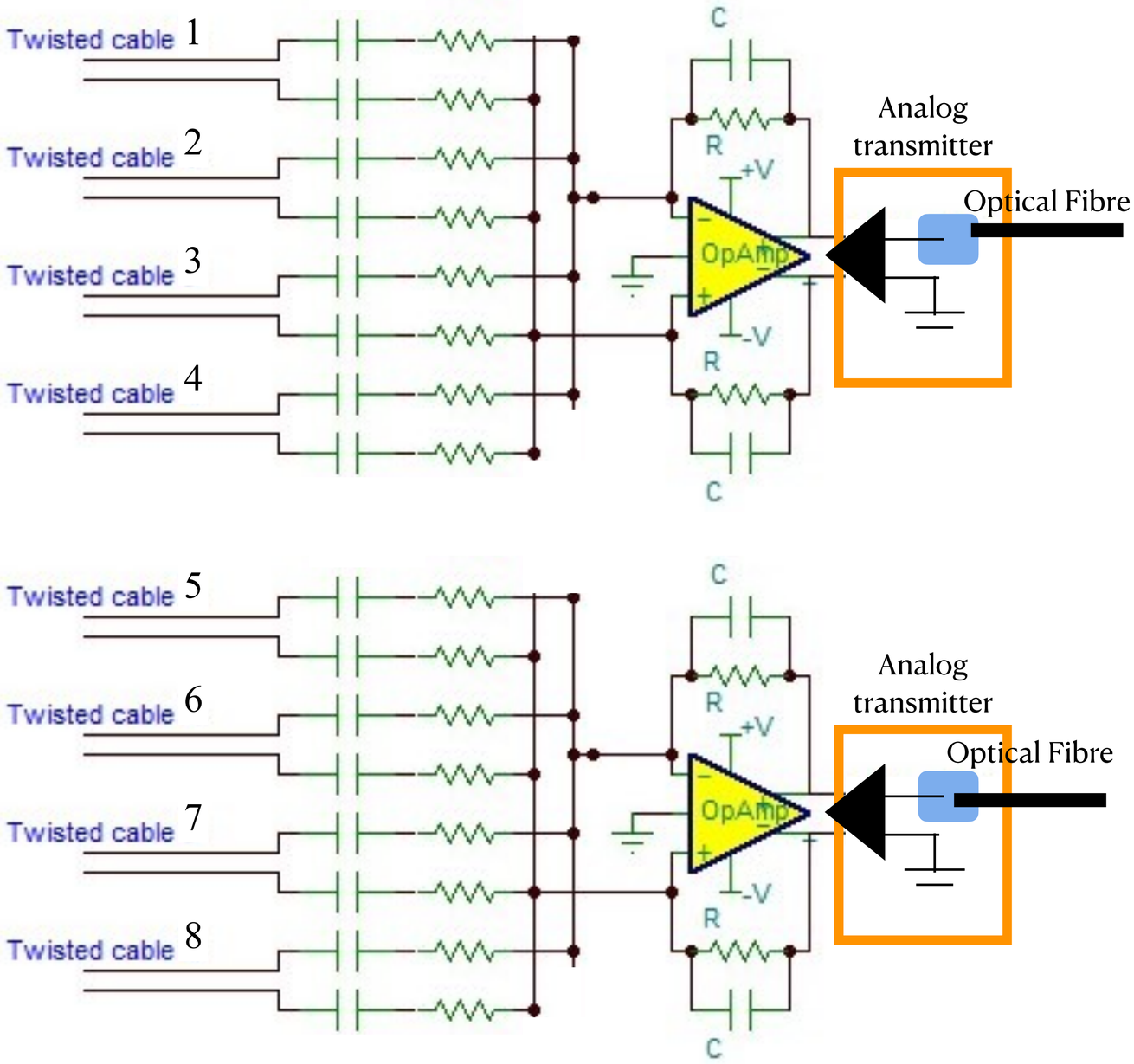


$$R' = 50\,\Omega$$
$$C' \sim 15\,nF$$
$$R = 10\,k\Omega$$
$$C \sim 15\,nF$$



RC stage before +V / GND provide the AC output. Signal can be read by both output.

Since the two outputs are specular, reading the signal in "differential" mode allows to increase the signal-noise ratio.



Active ganging

Each couple of outputs goes in an OpAmp stage: “active ganging stage”.

The OpAmp allows to sum multiple channels decoupling the capacitance of each channel.

At the same time it can provide a signal amplification (G ~ 10).

Increasing/tuning the signal in order to match:

- Transmitter full range
- SPE noise ratio
- Maximum number of photon collectable

Readout matching

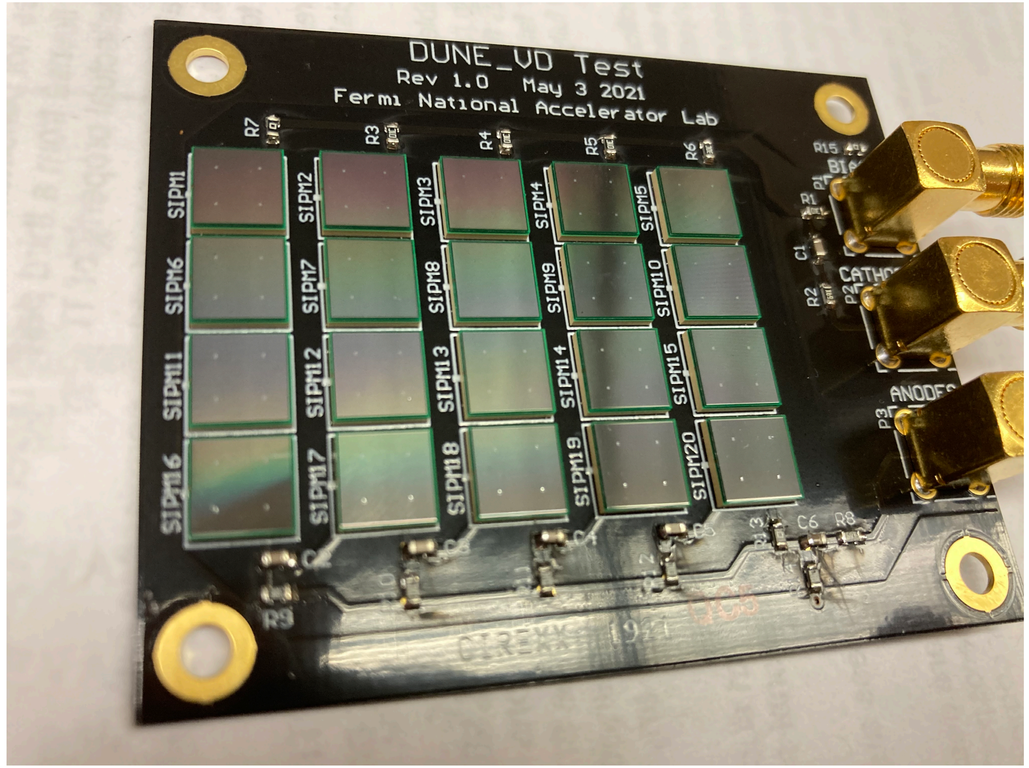
SiPM equivalent electric circuit has been developed by **Gustavo Cancelo (FCC)** to study the device response. A solution for unwanted effects (undershot, changes in recovery time, signal distortions) seems to be available.

The RC components, at the readout stage, have to be careful evaluated to match the timing response of the circuit (dependent by the hybrid configuration as well the SiPM equivalent impedance).

The model developed match with a SPICE simulation.

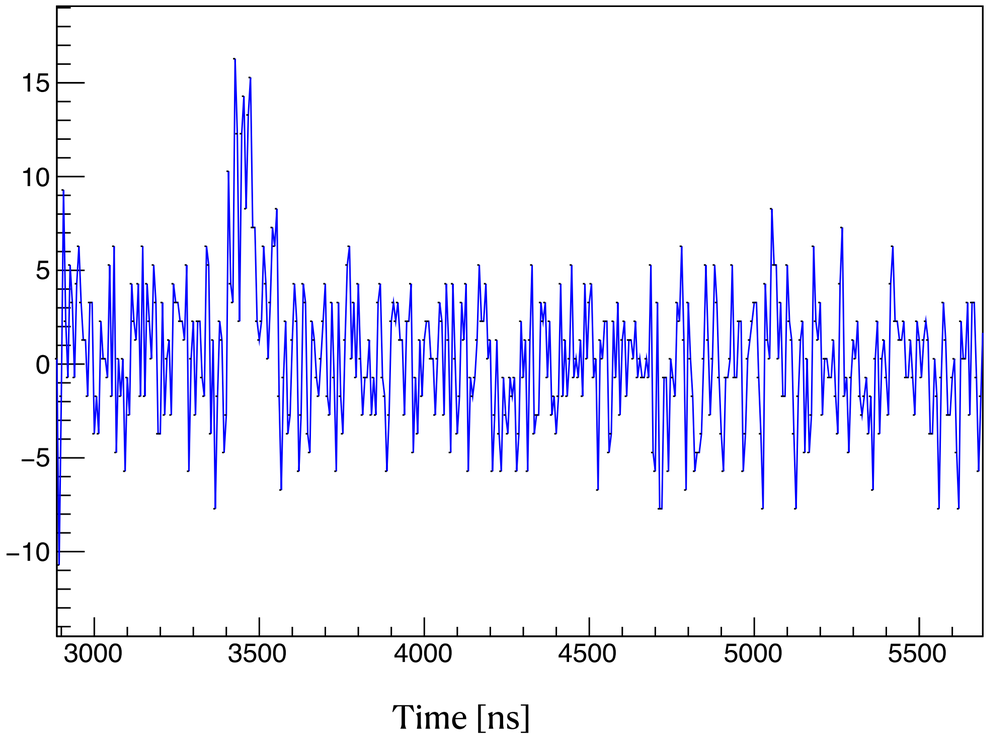
A “version-zero” of an hybrid circuit board (20 SiPM) is ready and it has been testing these days.

As first stage, we aim to define the hybrid circuit response in term of: SPE gain, signal amplitude, signal noise ratio, etc…

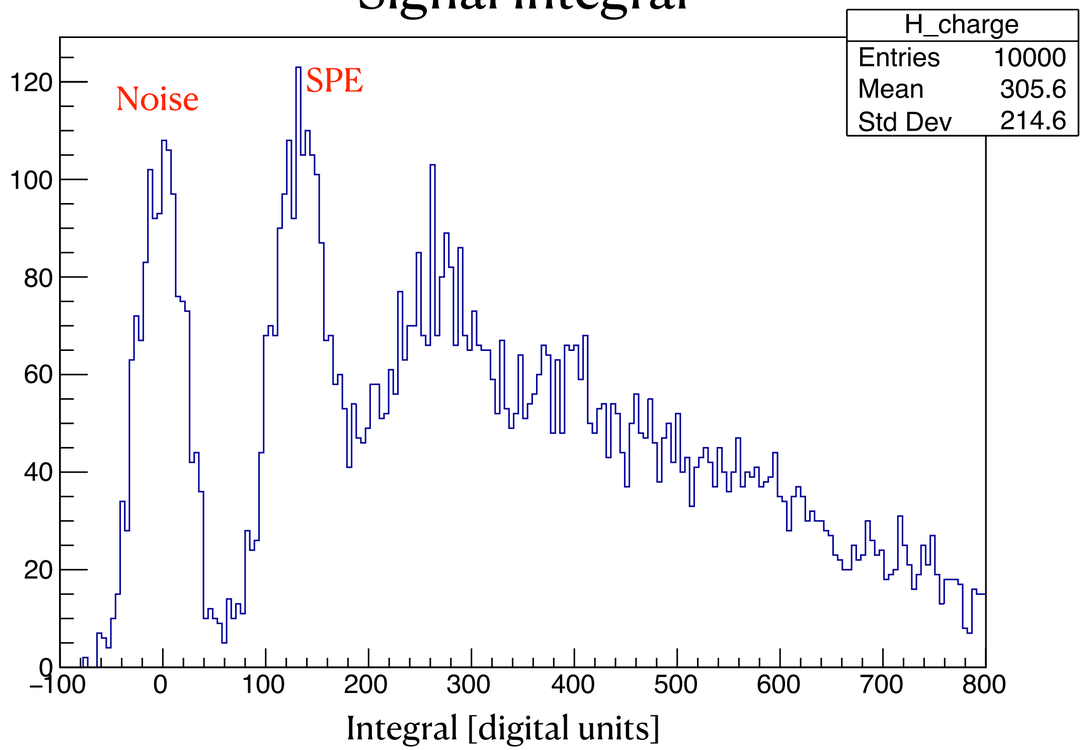


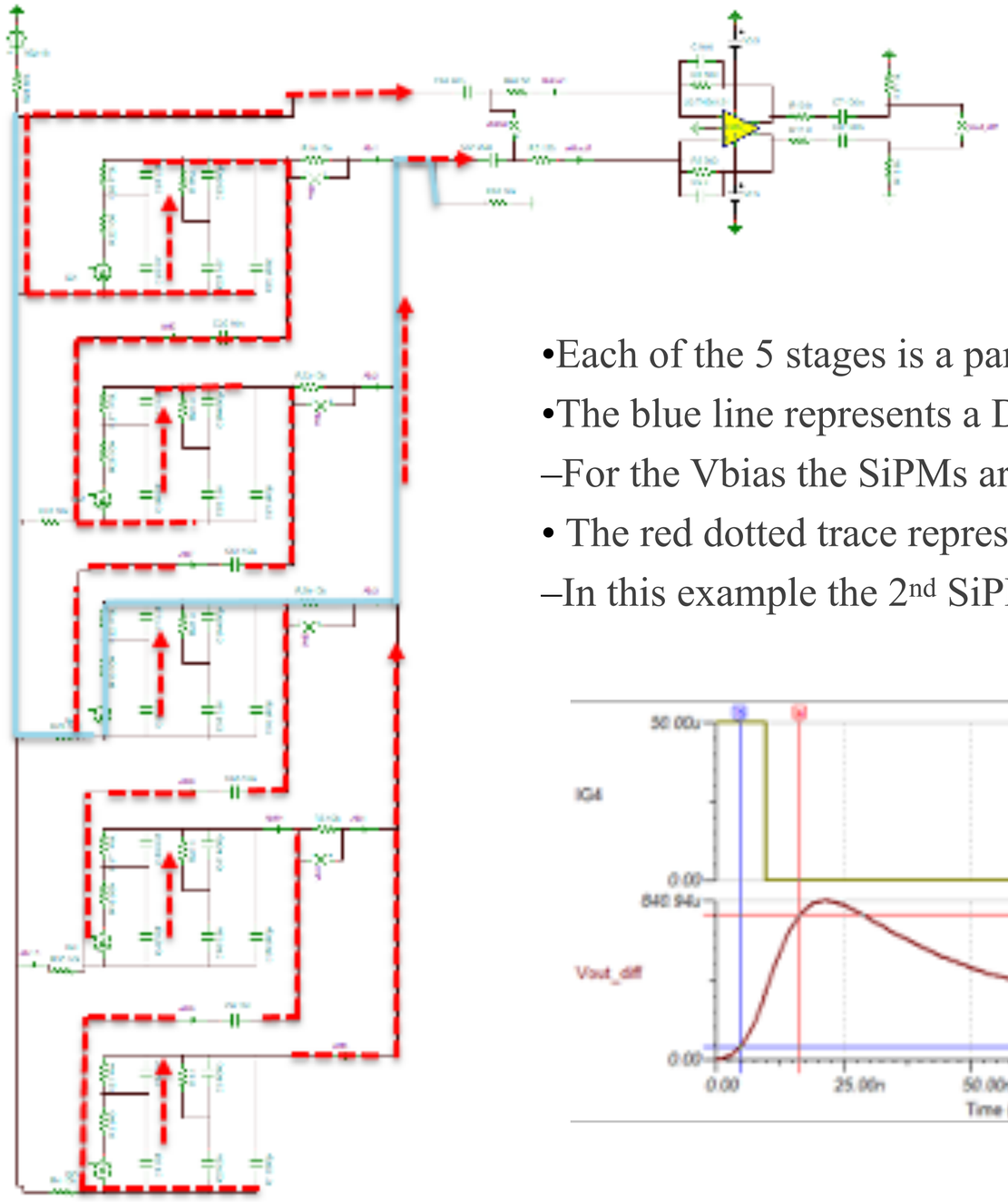
20 hybrid board first test (old SiPM version)

SPE signal



Signal integral





(5 x 4) hybrid x 4 (active ganging) simualtion

- Each of the 5 stages is a parallel of 4 SiPMs
- The blue line represents a DC bias path.
  - For the Vbias the SiPMs are in parallel, so Vbias hybrid is equal to the bias of a single SiPM.
- The red dotted trace represents the serial path of the signal.
  - In this example the 2nd SiPM fires and the signal goes through 1st stage.