Estimated FELIX FW resources required for VD
(with FW extensions to Ethernet)

Konstantinos Manolopoulos

Ethernet Based Readout for FD-VD

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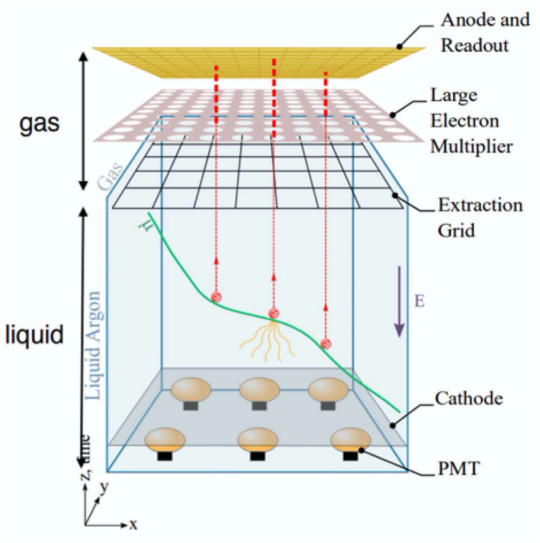
Science & Technology Facilities Council
Rutherford Appleton Laboratory

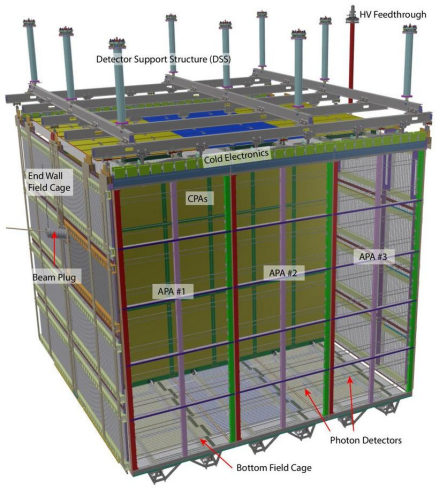
Outline

- System Requirements for Vertical Drift
- FELIX firmware resources
- DUNE Hit Finding firmware resources
- DUNE-FELIX firmware with ethernet extension
- Summary

System requirements for VD

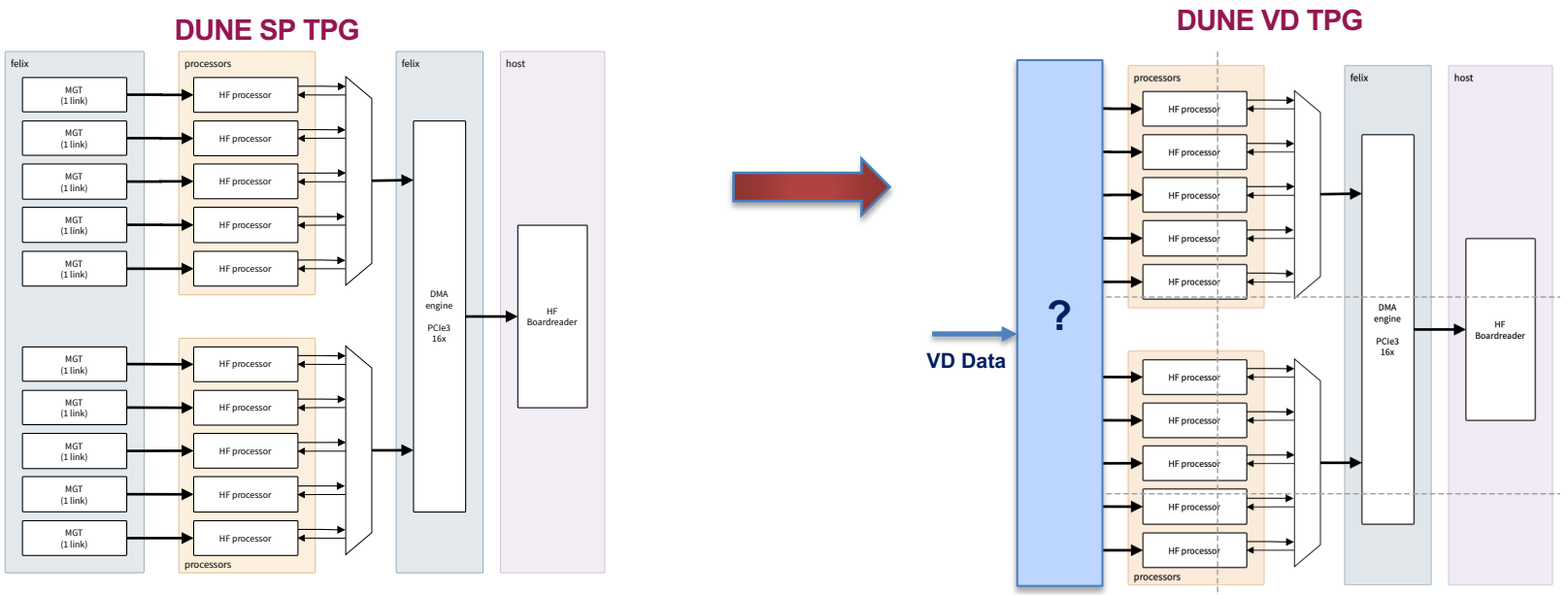
- Data arrive on UDP packets containing a set of frames of 64 channels
  - 1 channel = 14-bit ADC samples @2MSamples/s
  - 1 frame = 1clock tick
- 1 FPGA should accommodate 2560 channels
  - ~70% link utilization for a 100Gb link
- In DUNE Single Phase Trigger Primitive Generation firmware handles
  - 10 fibres per APA @9.6Gbps
  - Each fibre corresponds to 256 wires
  - 14-bit ADC samples@2MSamples/s
  - 10 “Hit Finder” processors operating in parallel (1 per fibre) @250MHz





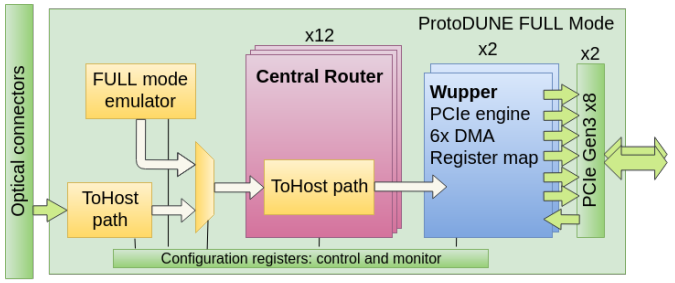
System requirements for VD

- This approach of parallel processing is ideal for FPGA implementation
- The concept is not tied to Single Phase electronics and can be used to process data from the Vertical Drift
- We do need understand the exact type of input we'll get from VD and decide how it can be used to feed data to the parallel HF processors



FELIX firmware resources

- Generic bi-directional i/f between frontend and pc
- 2 link protocols for data transfer
  - GBT/Versatile link
  - FULLmode protocol (single wide data stream)
- Jumbo Block Super Chunk (JBSC)
  - *Super Chunk: packed together Chunks to minimize memory-copy effort*
  - Transfer data to host with up to 4k DMA blocks

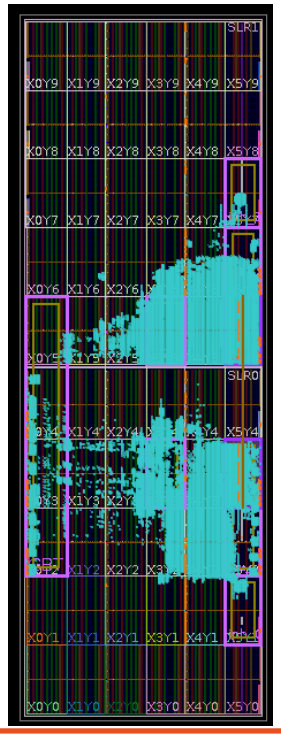


Target FPGA: xcku115-flvf1924-2-e

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	51183	663360	7.72
LUTRAM	367	293760	0.12
FF	90208	1326720	6.80
BRAM	275	2160	12.73
IO	133	728	18.27
GT	28	64	43.75
BUFG	46	1248	3.69
MMCM	5	24	20.83
PCIe	2	6	33.33



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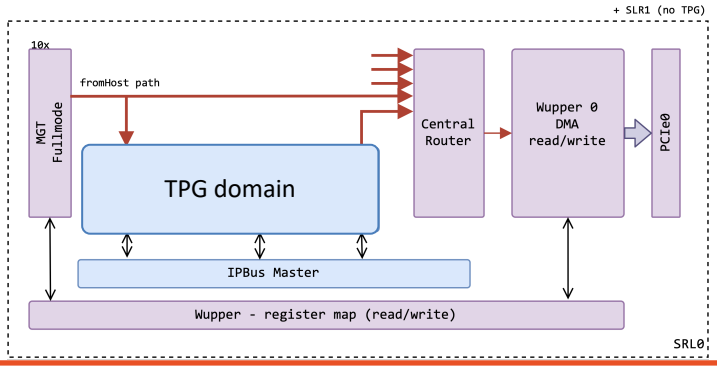
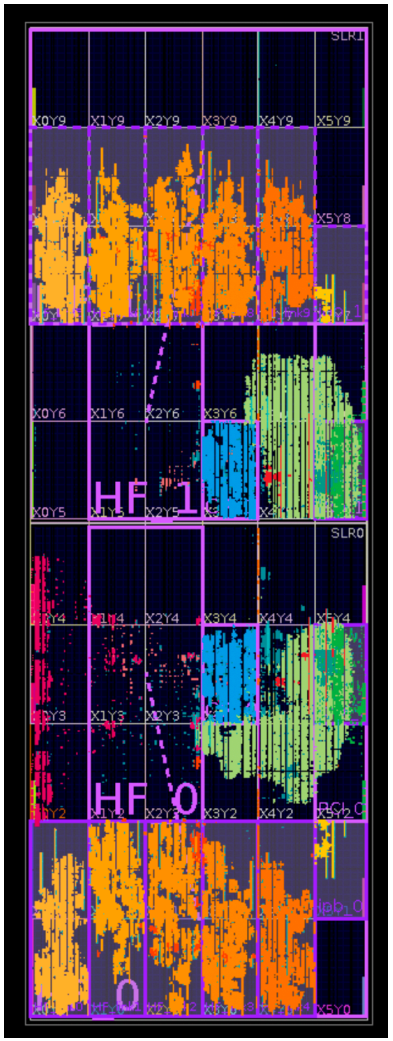
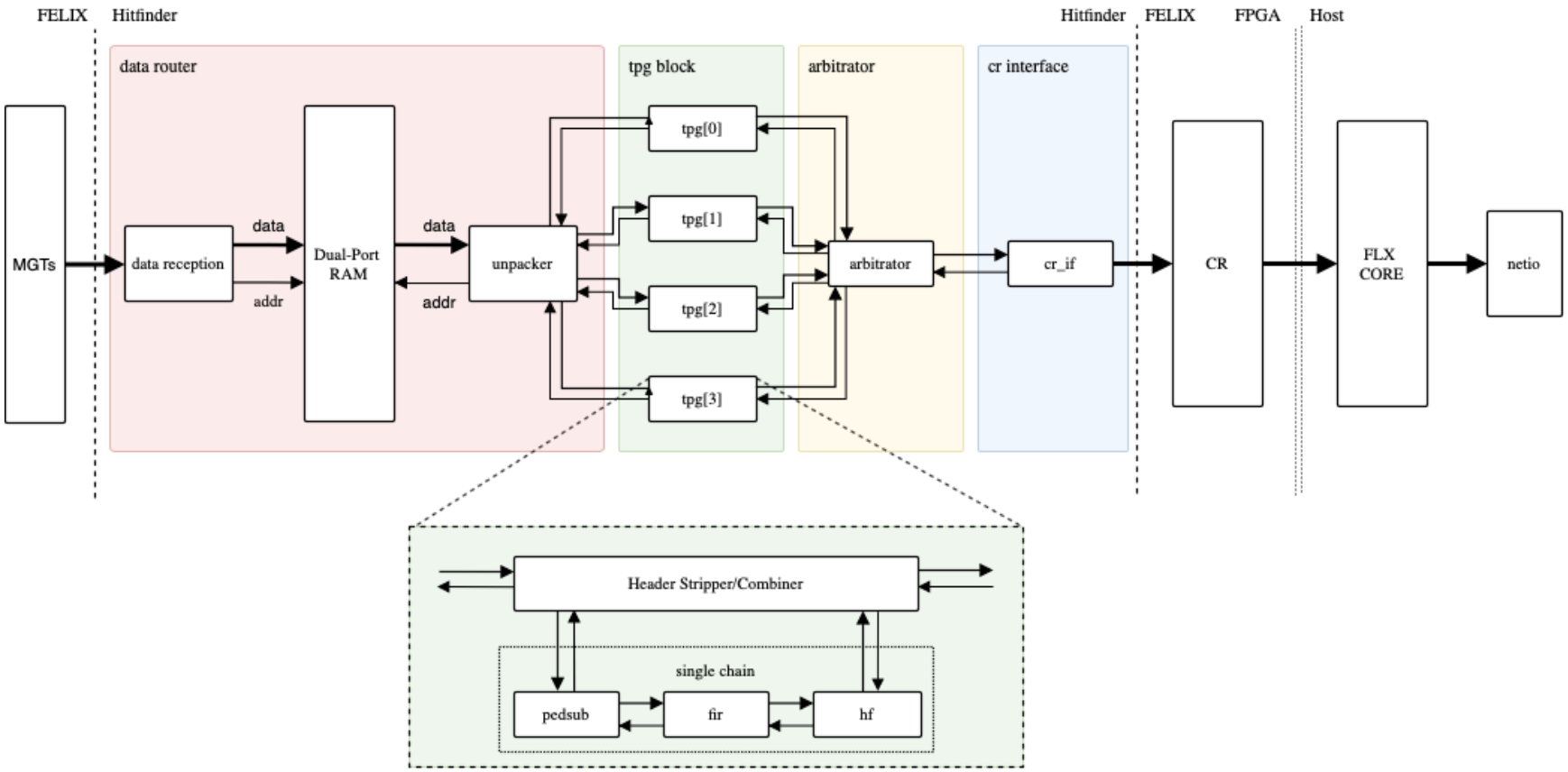
FELIX – DUNE TPG integration

- FELIX and TPG firmware domains kept separate
  - TPG as a “pod” inside the FELIX infrastructure
  - Added an IPbus-Wupper bridge block to use unmodified TPG firmware and software
- **Advantages**
  - Very thin layer of custom fw/sw (the bridge)
  - Full re-use of existing FELIX and TPG tools
  - Seamless switch between TPG dev boards and Felix
  - Minimal resource impact





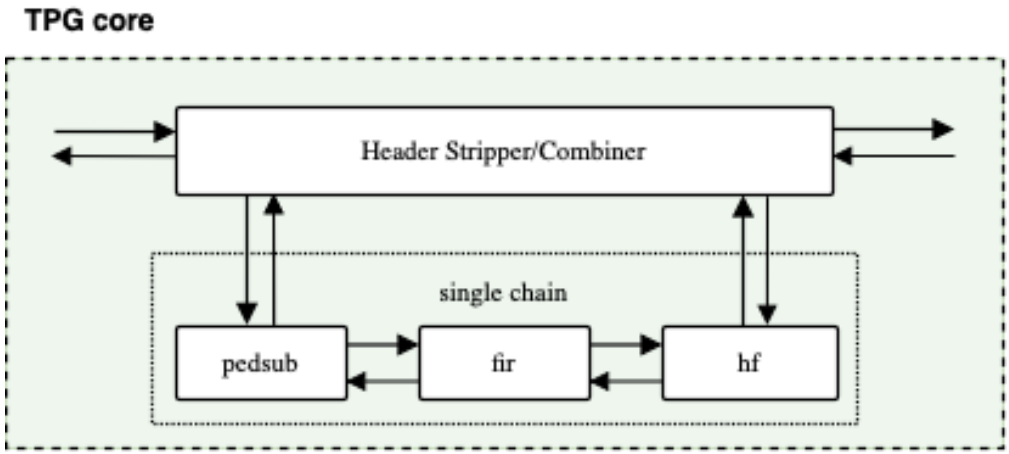
DUNE Hit Finding Processor Architecture



DUNE Hit Finding block diagram for 1 optical link

DUNE TPG Firmware

- Each Hit Finding processor uses 4 TPG cores
  - Each core processing 64 channels
  - Each core utilizes a *Pedestal Subtraction* block, a *32-tap FIR filter* and a *Hit Finder*
  - Currently using a fixed set of coefficients for all FIRs and have allowed Vivado to optimize some of the DSPs away
  - Max no of needed DSPs: 4 TPGs x 32 DSPs x 10 HF = 1280 DSPs



DUNE HF required resources

- DUNE-FELIX design is split in 2 Super Logic Regions (SLRs) with 5 optical link & 5 HF processors in each SLR

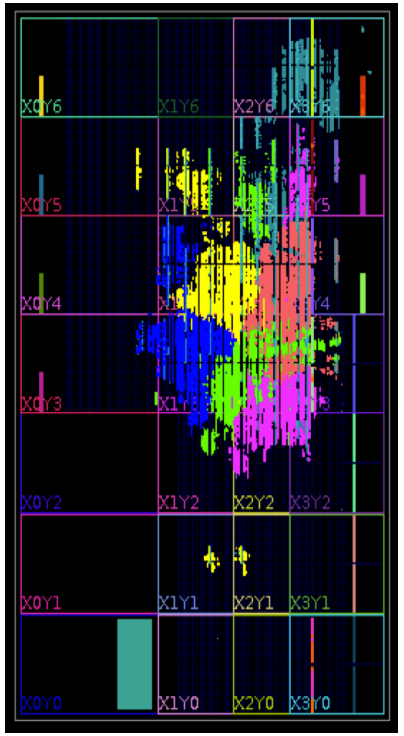
- Following table presents resource utilisation of 5 Hit Finding processors (FLX fw is not present)

Target FPGA: zu9eg (ZCU102 eval board)

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	33420	274080	12.19
LUTRAM	1061	144000	0.74
FF	60072	548160	10.96
BRAM	238	912	26.10
DSP	360	2520	14.29
IO	15	328	4.57
GT	1	24	4.17
BUFG	18	404	4.46
MMCM	2	4	50.00



DUNE-FLX firmware with Ethernet extension

- Minimal change needed: UDP→AXIs block implemented and integrated in the FLX fw
- Need to either use Xilinx MAC and PHY cores or to implement custom ones (not trivial!)
- Xilinx MAC/PHY cores depending on the FPGA series **are not always free**
  - In VU PHY is free but MAC with FEC is not
  - In VUP the 100G PHY and MAC with FEC are free
    - 10G PHY is also free but not 25G/40G/50G
  - In Versal the MAC/PHY are free for 10G/25G/40G/50G/100G
  - *If there's a need to use many 100G cores in a FPGA we may still need a soft PHY/MAC since the hard cores are limited*

DUNE-FLX firmware with Ethernet extension

- On VUP there are two options available
  - Use the RAL/TD 10G UDP core along with a custom Soft-MAC and the free Xilinx 10G PHY
  - Use the RAL/TD UDP core along with the free Xilinx 100G MAC/PHY

  Resource utilisation without PHY/MAC

Device	Rate	LUTs	Regs	BRAM
Virtex7	10G	5789	7045	19
Zync RFSoc US+	100G	12381	21573	57

- Bare in mind that moving between MACs (and to some extend PHYs) from different devices is not trivial
  - Testing the same system in different FPGAs/boards will require a lot of extra effort

Estimated total resources

- Bringing everything together the following table shows the estimated resources for
  - FELIX firmware +10 x Hit Finding processors + 1 x 100G UDP core

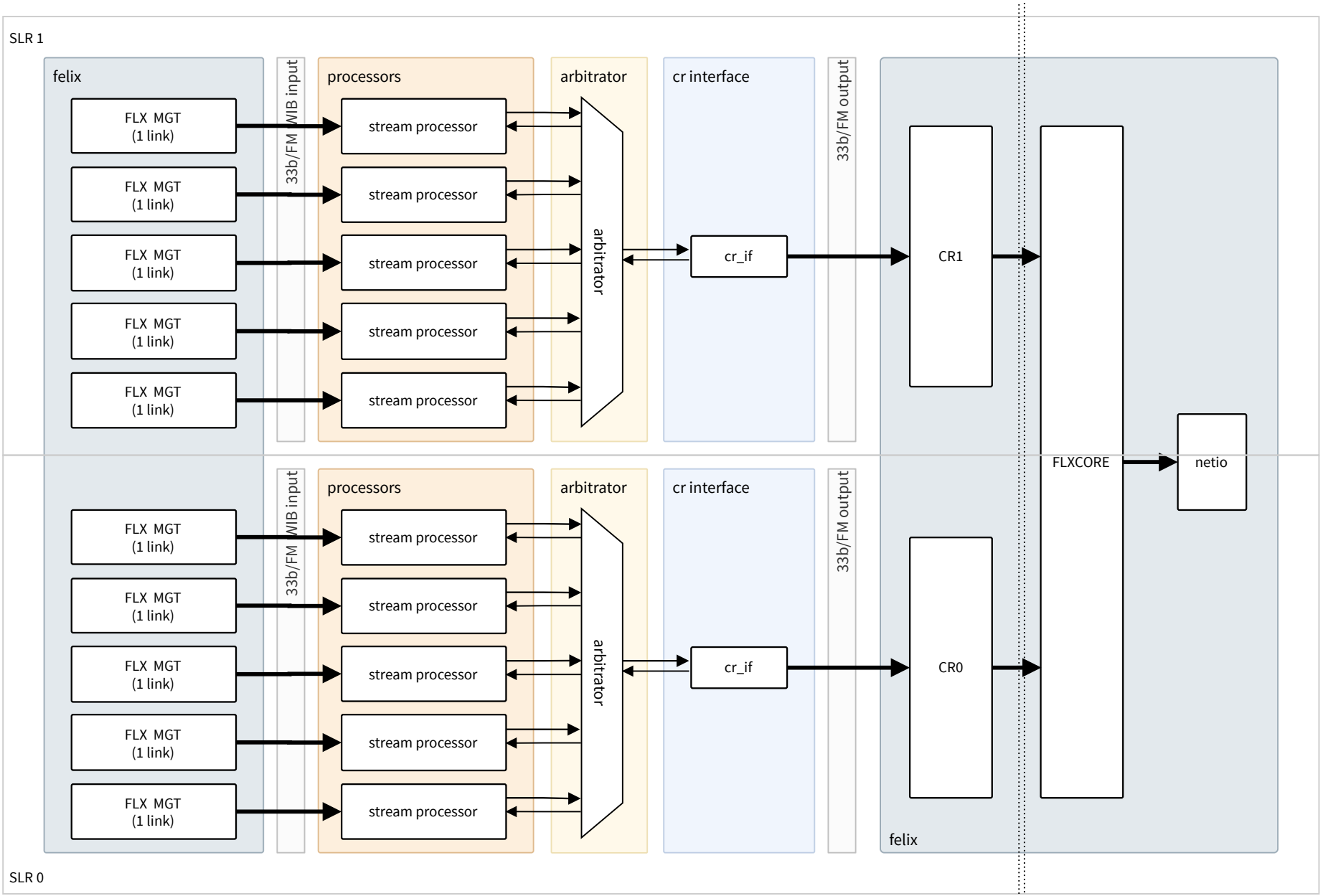
Estimated Resources for DUNE-FLX fw with Ethernet extension

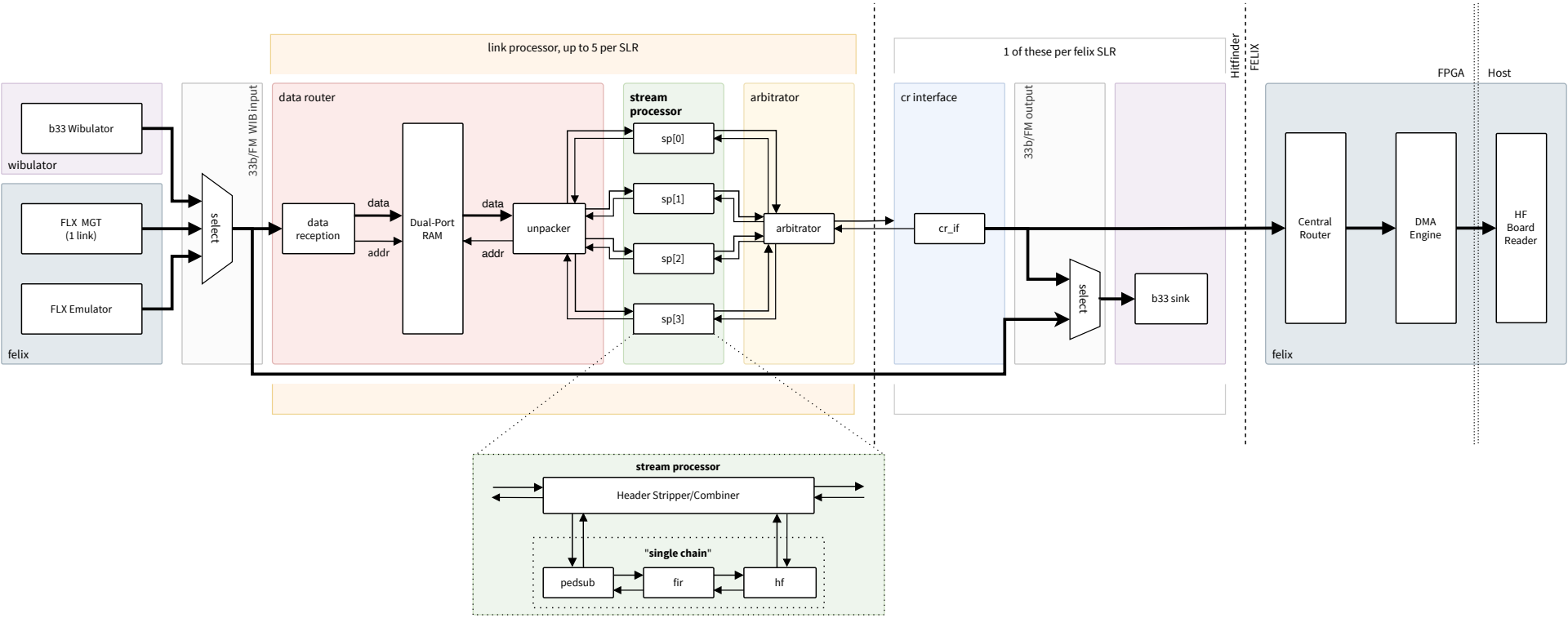
Resource	Utilisation
LUT	130404
LUTRAM	2489
FF	231925
BRAM	808
DSP	720 (max 1280)
PCIe	2

Summary

- Presented the resource requirements for the FELIX fw and the Hit Finding processors
- Options for the VD Ethernet extension with an estimated resource utilization for a 100G solution targeting the VUP family
- DUNE Trigger Primitive Generation is an ongoing effort → required resources will increase slightly in the near future
  - This will mostly affect LUT, LUTRAMs and FFs
- The FPGA choice will also affect both final resources and actual system cost
  - MAC/PHY IP cores are not always free
  - Depending on the final design choice there might not be enough hard cores and using soft cores means extra resources

Backup slides





FELIX firmware