Charge is in DocDB-14259

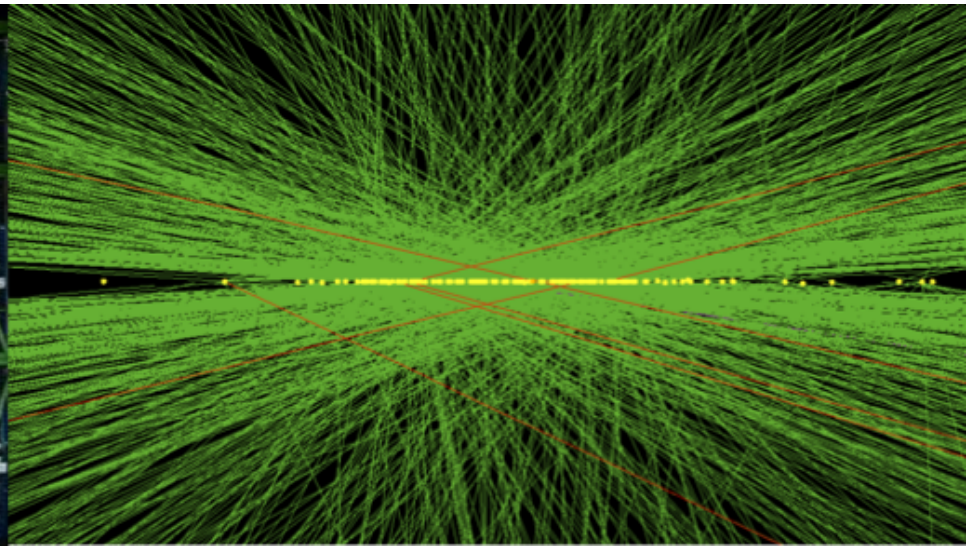
L1 Trigger

Jeff Berryhill, Keith Ulmer

MREFC Annual Review

August 25, 2021

Draft updated Aug. 23, 2021



Outline

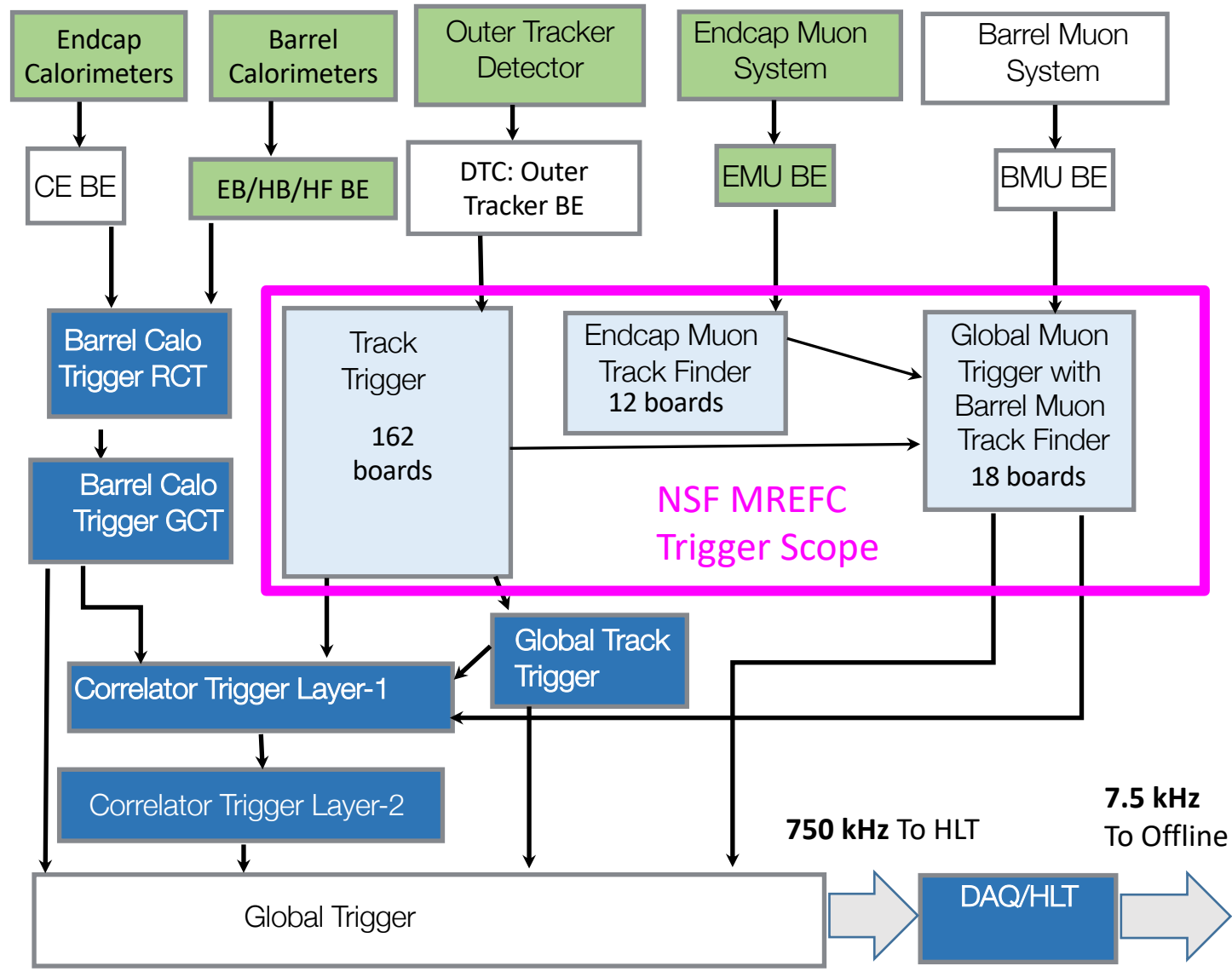
- Overview/Scope
- Completion of R&D
  - FDR Recommendations
- Progress Overview – Technical
  - Trigger
- EVM Status
  - Milestones/Schedule
  - Earned Value Summary
  - Summary of Covid Impacts and Plans
  - Summary of Change Control Actions
- Plans for 2022 and iCMS updates
- QA/QC Implementation
- Risks

Bio Sketch

- L2 Manager: Keith Ulmer, Colorado-Boulder
  - Physics PhD (Colorado 2007)
  - CMS Phase 2 Global Track Trigger System coordinator 2020-
  - USCMS L2 manager for Trigger/DAQ upgrade 2019-
  - CMS Phase 2 Track Trigger to L1 Trigger interface coordinator 2019-
  - CMS Convener: SUSY group 2014-2015
  - Technical Interface Coordinator
- L2 Manager: Jeffrey Berryhill, Fermilab
  - Physics PhD (Chicago 2000)
  - CMS L1 Trigger Upgrade Co-coordinator 2018-2020
  - USCMS L2 manager for Trigger/DAQ upgrade 2015-
  - CMS PM for LS1 upgrade of calorimeter trigger 2014-2015
  - CMS Convener: Standard Model Physics 2012-2013

Trigger Scope

- L1 Trigger system: 40 MHz event data processing
- ATCA PCBs with large FPGAs
  - Track Trigger 162+20 boards
  - Muon Trigger 30+9 boards
- 25 Gbps optical links
- Associated firmware and software to configure and run cards
- Firmware for track and muon reconstruction algorithms



R&D Completion

Charge 1b

- (pre-MREFC) R&D completed March 2020
- Successful prototype ATCA hardware demonstrated for both Track Trigger (Apollo card) and Muon Trigger (APx + Ocean card)
- 25 Gbps optical links demonstrated on both platforms
- Contributions from all MREFC institutions already in the R&D stage

Institution	Spending ($)
Boston	71,890
Colorado	133,264
Cornell	604,181
Florida	360,609
Northwestern	95,755
Notre Dame	217,144
Ohio State	26,133
Rutgers	120,748
TAMU	28,301
UCLA	34,159
Wisconsin	36,472
Total	**1,728,661**

R&D Milestones

Charge 1b

WBS	Milestone	Planned Finish Date	Last Month's Finish Date	Forecast Finish Date
TRIG 402.9.7	µTCA 25 Gbps demonstrator board testing complete	Apr-18	Apr-18	Completed Apr-18
TRIG 402.9.4	Barrel and endcap muon trigger initial algorithm and performance	Mar-18	Mar-18	Completed Mar-18
TRIG 402.9.4	Barrel muon trigger initial algorithm firmware	Jun-18	Jun-18	Completed May-18
TRIG 402.9.4	PTLUT1 memory mezzanine design	Jun-18	Jun-18	Completed May-18
TRIG 402.9.4	PTLUT1 first mezzanines	Sep-18	Sep-18	Completed May-18
TRIG 402.9.4	PTLUT1 card tested	Dec-18	Dec-18	Completed Dec-18
TRIG 402.9.7	Complete track trigger ATCA daughter board design	Dec-18	Feb-19	Completed Feb-19
TRIG 402.9.4	Muon trigger prototype board + memory card tested	Mar-19	May-19	Completed May-19
TRIG 402.9.7	First testing of track trigger ATCA prototype complete	Apr-19	Jun-19	Completed May-19
TRIG 402.9.7	Reference algorithm for track trigger defined	Apr-19	Apr-19	Completed Apr-19
TRIG 402.9.4	Demonstration of muon trigger physics requirements with pro	Dec-19	Dec-19	Completed Dec-19
TRIG 402.9.7	Track trigger preproduction design begins	Jan-20	Jan-20	Completed Feb-20

- All Trigger R&D Milestones completed before start of MREFC
- Used prototype hardware to demonstrate first versions of Track Finding and Muon Track Finding algorithms in firmware

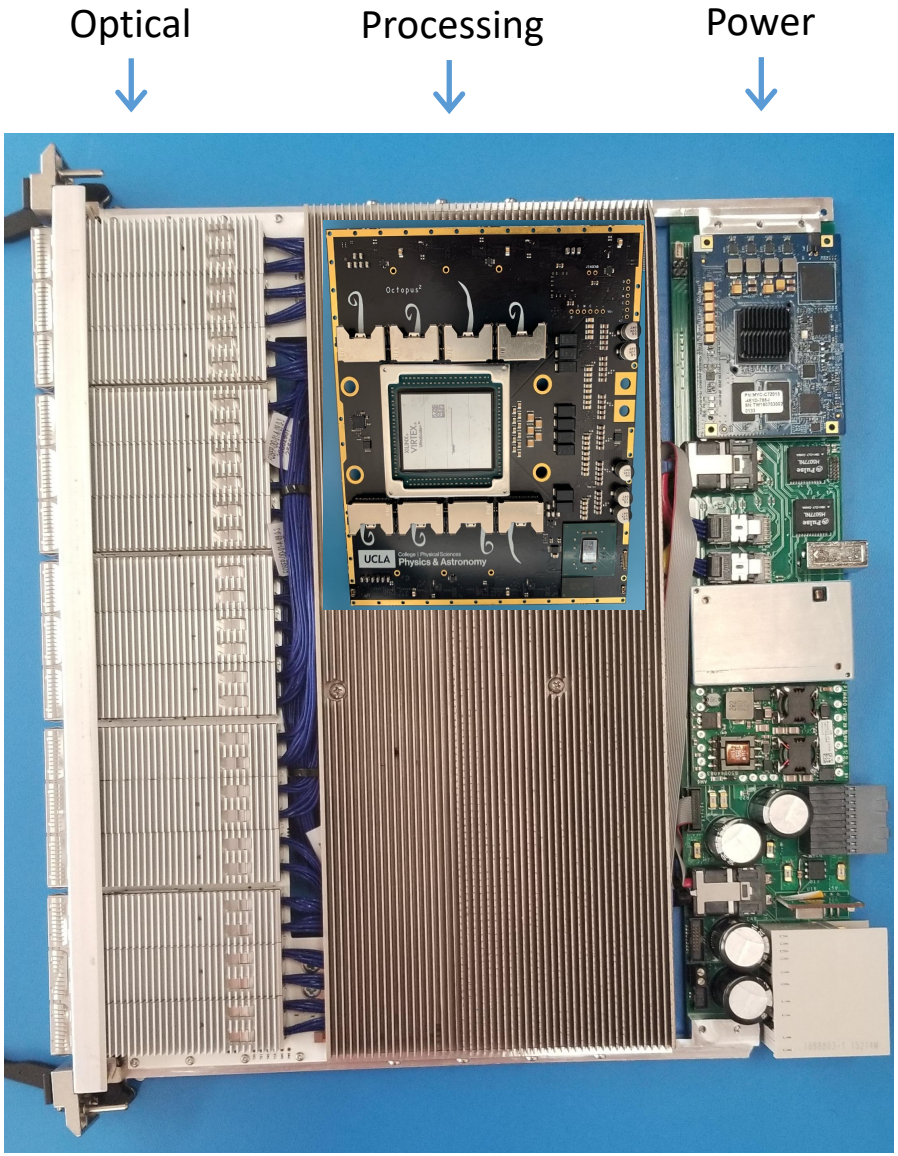
FDR Recommendations

Charge 1a

- No Recommendations for Trigger from the FDR
  - Continue with MREFC plan

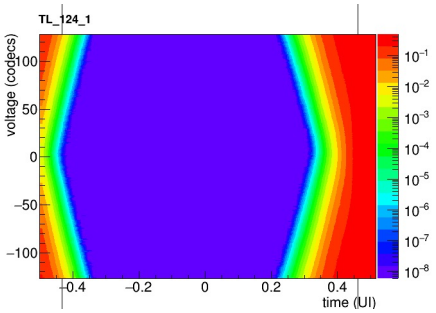
Muon Trigger Progress (402.9.4)

- Preproduction hardware progress
- X2O card from merging of UCLA and Florida design efforts
  - Modular design with optical, FPGA, and power modules
- QSFP-Double Density optical module complete (120 RX + 120 TX links @25Gbps)
- FPGA modules designed and assembled for VU13P and KU15P FPGA options
- Power module: DC-DC converters and Gigabit ethernet successfully tested

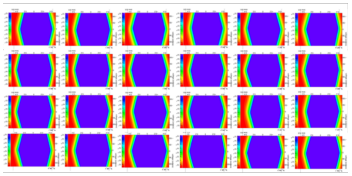


Muon Trigger Progress (402.9.4)

- Preproduction card testing and infrastructure progress
  - Zynq board control firmware migrated to CentOS
  - X2O IPMC board control software completed
  - Integration with CERN DTH (timing and control) card over backplane
  - Successful 25 Gbps link tests on 120 links/board
- Preproduction design milestones met
- Standalone testing milestones met
- Now working on integration testing



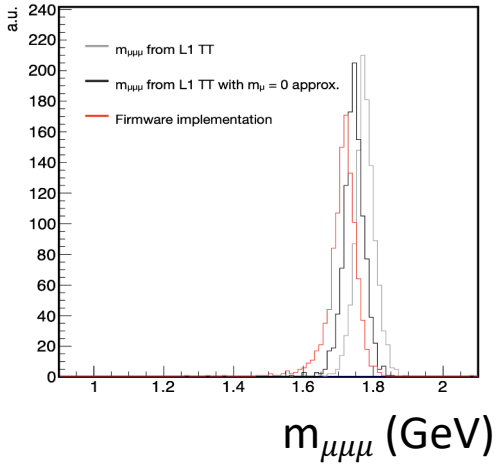
QSFP-DD SR4 optics excellent signal integrity @ 25Gbps



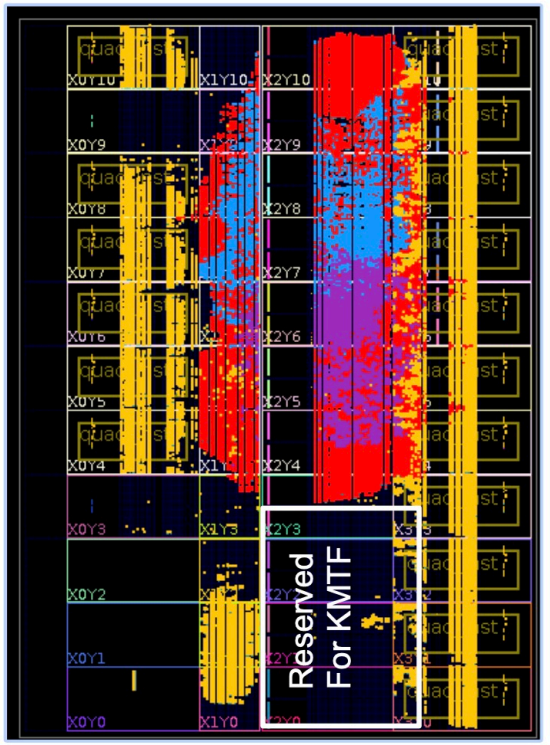
Tier - Milestone	Baseline	Previous Month	Forecast	Delta from baseline
T3 - TD - MTF preproduction design complete	2020-06-30	2020-07-30	2020-07-30A	-30
T3 - TD - BMTF preproduction design complete	2020-06-30	2020-07-30	2020-07-30A	-30
T3 - TD - MTF PreProduction Ready for Integration Testing	2021-03-31	2021-03-31	2021-03-31A	0

Muon Trigger Progress (402.9.4)

- Algorithm firmware progress
  - New Endcap Muon Track Finder algorithm implemented in HLS
    - Includes neural net track pT assignment
  - Global Muon Trigger firmware integrating tracker track streaming, matching, and isolation
  - GMT also includes topological algorithms like $\tau \rightarrow 3\mu$
  - GMT firmware emulation in CMSSW
  - All firmware being migrated to X2O card
- Interfaces
  - Baselined all GMT interface definitions and link data format (EMTF, PFL1, GT)



Ocean



Framework
Tracker Muons
Cleaning and Sorting
Track based isolation

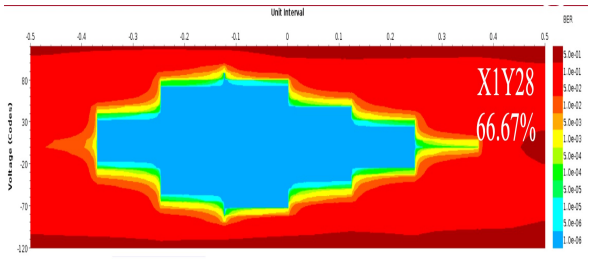
~30% resource usage on smaller Ocean FPGA

Track Trigger Progress (402.9.7)

- Preproduction hardware progress:
- Track Trigger Apollo card split into Service and Command modules
  - Service Module: board configuration and monitoring
    - First SM preproduction design submitted in July 2020. Cards assembled in Nov. 2020.
    - First version needed rework due to evolving timing and control (TCDS) requirements
    - Revised SM design completed June 2021
  - Command Module: hosts dual VU13P FPGAs and 25 Gbps optics
    - Preproduction design completed in June 2021
    - Some delay due to new Samtec Firefly 12 channel transceiver part specs changing

Track Trigger Progress (402.9.7)

- Hardware testing progress
- Started preproduction testing with first version of SM
  - Power up and run the CM
  - Supports Ultrascale+ Zynq
  - Ethernet switch tested

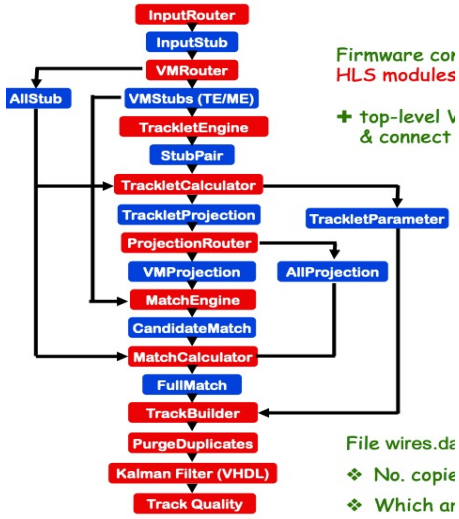


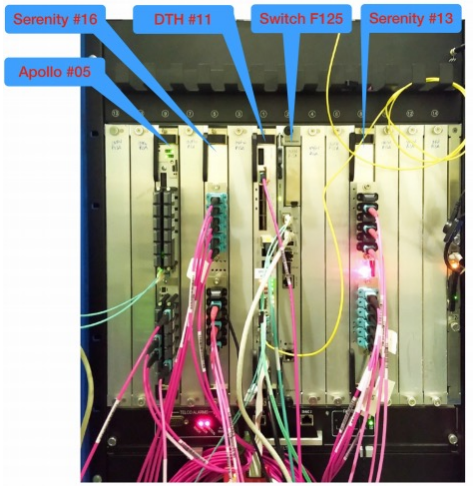
- New 12Tx/12Rx Firefly 25 Gbps optical transceivers validated with good eye diagrams. 2nd generation part also tested, with even better results.
- Command Module power, current, and cooling tests with ATCA card and Ultrascale+ FPGAs
  - >100A per FPGA for >250W total per board successfully validated
- Defined online software (ShepherdsCrook) interface to Apollo board
- Achieved preproduction design milestones for both SM and CM
  - About 6 months behind baseline. Roughly half due to COVID (discussed later).
  - SM testing in parallel with re-design to recover the 3 months delay
  - CM is 3 months behind baseline, largely due to more challenging design than anticipated (ex. changing Firefly specs)

Tier - Milestone	Baseline	Previous Month	Forecast	Delta from baseline	Delta from previous month
T3 - TD - Track Trigger preproduction command board design complete	2020-12-18	2021-06-18	2021-06-15A	-179	3
T3 - TD - Track Trigger preproduction service board design complete	2020-12-18	2021-06-01	2021-06-15A	-179	-14

Track Trigger Progress (402.9.7)

- Algorithm Firmware Progress
  - Since FDR have transitioned all algorithm fw to HLS to improve maintainability and development speed
    - All algorithm blocks now working in HLS (plus Kalman Filter in VHDL)
  - Current effort on end-to-end slice test demonstration for Summer
    - On prototype hardware from R&D period
    - Top-level firmware (HDL) developed to chain modules together. Significant progress to automate the generation of this fw "glue" holding the processing steps together
- Firmware emulation code being rewritten to better match fw implementation on hardware
- Preproduction algorithm firmware v0 design complete milestone met Dec. 2020
  - Around 3 months behind baseline largely due to inefficient working conditions due to COVID (discussed later)
  - This milestone satisfied by having all algorithm firmware blocks written and verified
  - Next algorithm milestone is linking them all together in end-to-end slice test



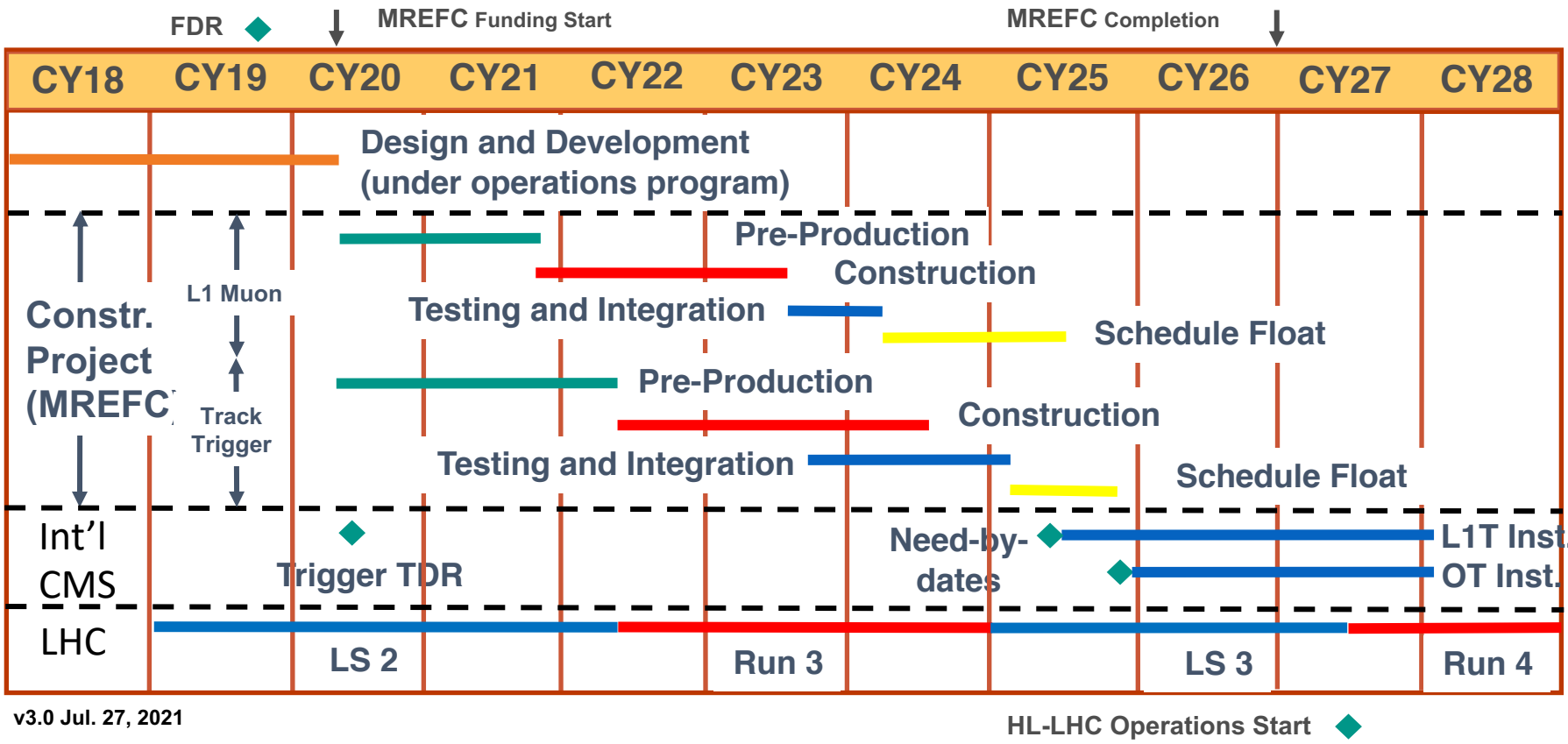


Tier - Milestone	Baseline	Previous Month	Forecast	Delta from baseline	Delta from previous month
T3 - TD - Track Trigger preproduction algorithm firmware design complete - v0	2020-09-22	2020-12-30	2020-12-30A	-99	0

Resource usage (Q from David)

- Pattern Recognition is performed in HLS modules
- Track Fit is performed with Kalman Filter in VHDL
- HLS modules exported as IP cores and combined with VHDL to pull whole project together
- FPGA resources estimated so far extrapolating from individual modules up to full system
  - This simple extrapolation shows the full sector firmware should fit on a VU13P FPGA
  - Overall HDL build not yet to point where it can be tested for resource usage
    - Routing constraints, meeting timing, SLR crossings, etc. still to be dealt with
- HLS modules all included in Continuous Integration
  - VHDL Kalman and module connector fw not yet in CI
- Current end-to-end slice test will link together all pattern recognition and track fit modules in narrow slice, including connector fw
- Major items for algorithm firmware after slice test:
  - Scale out from narrow slice to cover full detector phi-sector
  - Merge some PR modules into single steps to reduce latency

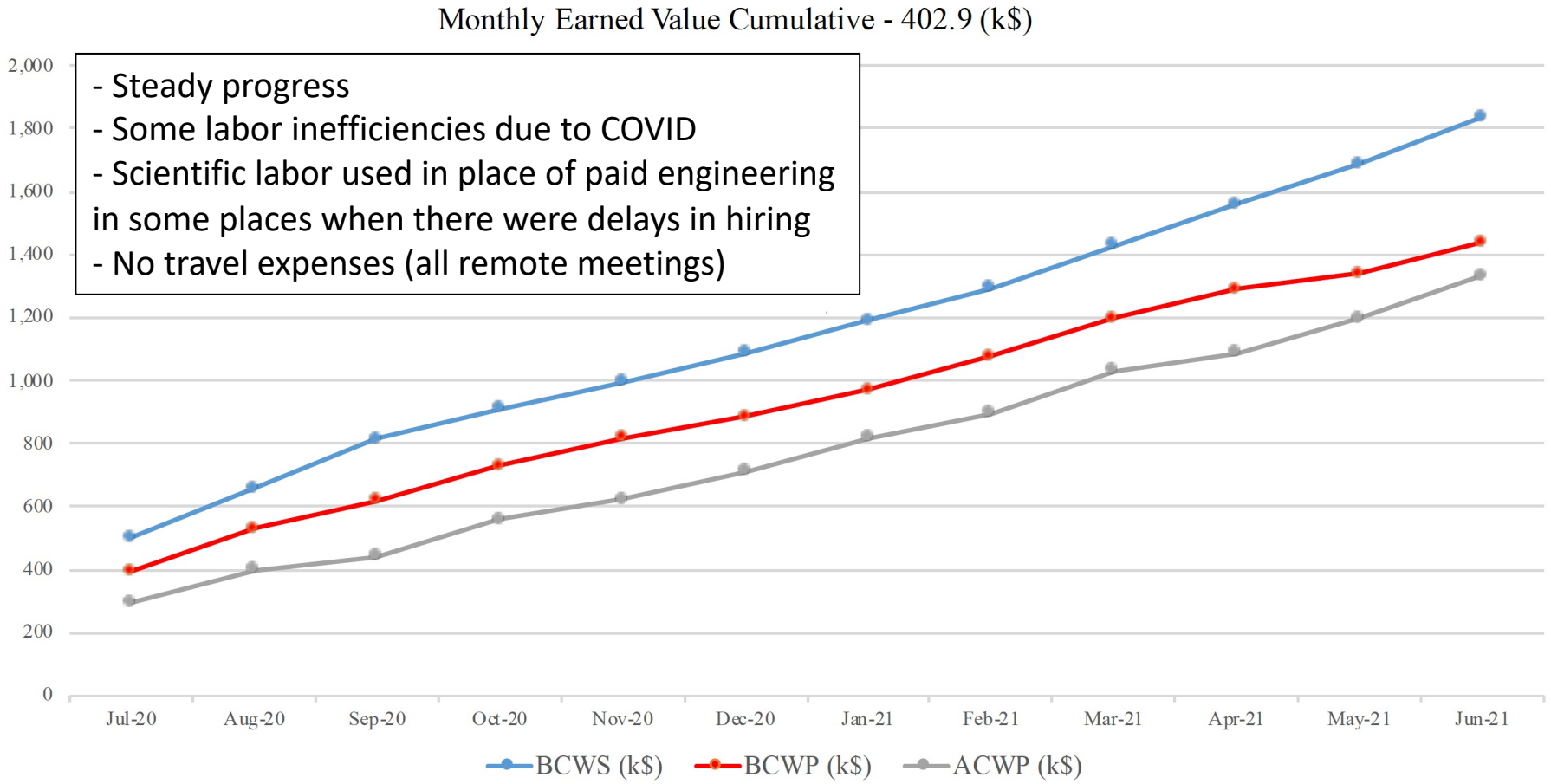
Trigger Schedule Summary



- Muon Trigger Float: 16 months (50% of time to go)
- Track Trigger Float: 9 months (21% of time to go)

EVM Summary

Charge 2a



	Jul-20	Aug-20	Sep-20	Oct-20	Nov-20	Dec-20	Jan-21	Feb-21	Mar-21	Apr-21	May-21	Jun-21
BCWS (k$)	503	659	815	912	996	1,089	1,189	1,295	1,428	1,561	1,688	1,837
BCWP (k$)	396	530	618	729	820	885	972	1,079	1,198	1,289	1,341	1,440
ACWP (k$)	296	398	441	559	623	714	817	897	1,032	1,088	1,199	1,335

EVM Performance by Institution

Institution	Budget ($k)	Earned ($k)	Actual ($k)	CPI	SPI
Boston	120	92	67	1.36	0.76
Colorado	119	90	72	1.26	0.76
Cornell	475	240	230	1.04	0.50
Florida	349	350	295	1.19	1.00
Northeastern	50	38	44	0.87	0.77
Northwestern	204	194	195	0.99	0.95
Notre Dame	148	143	139	1.02	0.97
Ohio State	41	12	14	0.89	0.30
Rutgers	88	44	7	6.18	0.50
TAMU	21	21	24	0.90	1.00
UCLA	222	217	248	0.88	0.98

Covid Impacts

Charge 3b

- Labor inefficiency
  - General working inefficiency with remote operations and new safety protocols
    - Board testing in labs was severely limited, but proceeded with limited lab access and remote hardware access
    - Remote work easier for board designs, firmware, and software, but still at lower-than-normal efficiency
  - Reflected in Monthly Reports generally as 10-20% inefficiency in labor production
- Vendor delays
  - Some vendors for board fabrication and assembly were delayed by 1-2 months longer than normal delivery times
  - Due to both staffing issues and parts availability
- Supply chain issues
  - Some key components face global shortages (ex. FPGA chips)
  - Have received some scary lead-time quotes (ex. 11 months for Xilinx FPGAs, when ~4 weeks was normal previously. Some details in next slide.)
  - Despite this, have been able to negotiate for quicker delivery of small size orders needed for preproduction
  - No impact from supply chain issues yet, but need to remain cognizant going forward, especially for the larger orders needed for production
- Net result is ~3 month delay in the schedule and ~$100k in lost labor productivity

FPGA availability (Q from David)

- With COVID and the global chip shortage, we've seen increased lead times quoted for FPGAs
- So far, we've been able to procure what we need much more quickly than quoted
  - Track Trigger (Xilinx VU13P, 12 pieces)
    - March 2021 quoted 12-14 weeks for delivery
    - April 2021 ordered and told 35 weeks for delivery
    - After discussions with Xilinx able to receive delivery after 5 weeks
  - Muon Trigger (Xilinx VU13P, 6 pieces)
    - Ordered April 2021 and told 35 weeks for delivery
    - Actually delivered after 9 weeks
- Now have all parts needed for pre-production cards
- Production orders will be much larger, so important to monitor this issue
  - Scheduled to procure parts for pilot production in Summer 2022

BCRs and iCMS Updates

- CMS updates
  - CERN extended the Long Shutdown 3 (LS3) schedule to push back the start of the HL-LHC by 1 year
    - We determined that the Trigger schedule can proceed largely as originally planned without significant external dependencies
    - Need by dates for Track Trigger and Muon Trigger moved back to give additional float
    - Assigned new risks that additional firmware features or board revisions could be required in the additional time (ex. due to advancing technology)
  - L1 Trigger Technical Design Report (TDR) was completed in April 2020
    - Muon Trigger architecture revised to combine Barrel Muon Track Finder and Muon Global Sorter layers into new Global Muon Trigger
    - No change in schedule needed
    - Cost increase $94k. BoE has been updated.
- Processed 5 Baseline Change Requests (BCRs)
  - BCR-111 - Update Track Trigger schedule to account for extended LS3. Need by date moved back to Oct. 2025
  - BCR-114 - Update Muon Trigger for TDR architecture. Merge BMTF and Muon Sorter into new Global Muon Trigger. Update board counts. Update cost book estimates for hardware.
  - BCR-118 - Change Muon Trigger need by date (1/2025 → 7/2025) to reflect new international schedule
  - BCR-123 - Move some Florida firmware labor to SHREC student
  - BCR-126 - Trigger schedule ~3 month delay due to COVID

Plans for FY2022

- Muon Trigger plans through 2022
  - Testing of preproduction X2O cards in progress now
  - After successful preproduction integration tests, move to pilot production design
  - Pilot design, procurement, testing, integration cycle expected to conclude Sept. 2022
  - Associated firmware and software development for pilot production follows similar timeline as hardware
- Track Trigger plans through 2022
  - Receive and test preproduction Apollo service and command modules through Feb. 2022
  - Design pilot production SM and CM March– Sept. 2022 followed by procurement and testing
  - Associated firmware and software development for pilot production follows similar timeline as hardware

QA/QC Implementation

Charge 2d

- Have recently reviewed project documentation
  - Technical requirements – verified no changes needed
  - QA/QC and test plans – verified no changes needed
  - Interface documents – small updates to interface partner contacts
  - Scope options – small updates to decision dates to match current CMS schedule
- Following QA/QC plan to verify performance (docDB-13318). Some examples:
  - Demonstration: Use prototype hardware to verify optical link performance and board configuration and monitoring controls
  - Demonstration: Use prototype hardware to demonstrate algorithm latency and resource usage within specifications
  - Simulation: Verify algorithm efficiencies and rates

Risks

- New Risks (402-9-[11-16]) added to cover possible impacts from LS3 delay
- Remaining risks unchanged from FDR

/ Operations Activity: 402.9 TD - Trigger and DAQ (NSF) (11)

RT-402-9-02-N	TD - Board or parts vendor non-performance (NSF)	20 %	42 -- 176 -- 318 k$	1 -- 3 -- 4 months	2 (Medium)
RT-402-9-03-N	TD - I/O performance does not meet scope and/or interface requirements (NSF)	20 %	349 -- 681 -- 1013 k$	3 -- 5 -- 7 months	2 (Medium)
RT-402-9-04-N	TD - Additional board redesign is required (NSF)	20 %	67 -- 176 -- 318 k$	1 -- 3 -- 4 months	2 (Medium)
RT-402-9-05-N	TD - Additional firmware development is required (NSF)	20 %	12 -- 25 -- 50 k$	1 -- 2 -- 3 months	1 (Low)
RT-402-9-06-N	TD - Baseline FPGA does not satisfy requirements (NSF)	20 %	77 -- 261 -- 522 k$	1 -- 3 -- 6 months	2 (Medium)
RT-402-9-11-N	TD - Endcap muon board needs revision due to technology advances (NSF)	10 %	152 -- 247 -- 295 k$	6 -- 12 -- 15 months	2 (Medium)
RT-402-9-12-N	TD - Endcap muon trigger firmware needs additional feature development (NSF)	10 %	78 -- 156 -- 195 k$	6 -- 12 -- 15 months	2 (Medium)
RT-402-9-13-N	TD - Global Muon Trigger board needs revision due to technology advances (NSF)	30 %	182 -- 259 -- 298 k$	6 -- 12 -- 15 months	3 (High)
RT-402-9-14-N	TD - Global muon trigger firmware needs additional feature development (NSF)	30 %	102 -- 205 -- 256 k$	6 -- 12 -- 15 months	3 (High)
RT-402-9-15-N	TD - Track trigger board needs revision due to technology advances (NSF)	30 %	189 -- 252 -- 284 k$	6 -- 12 -- 15 months	3 (High)
RT-402-9-16-N	TD - Track trigger firmware needs additional feature development (NSF)	30 %	268 -- 536 -- 670 k$	6 -- 12 -- 15 months	3 (High)

Summary

- Track Trigger and Muon Trigger have successfully completed preproduction hardware designs
- Procurement and testing now in progress
- Around 3 months delay due to COVID effects
  - Labor inefficiencies
  - Procurement and Vendor delays
- Track Trigger an additional 3 months delayed due to unexpected technical challenges
- No major modifications to the FDR plans, even with delayed LS3
- Earned value and QA/QC procedures are in place and working well

Quality Assurance

From FDR

- All QA aspects of the HL LHC CMS Detector Upgrade Project will be handled in accordance with the Fermilab Integrated Quality Management approach, and the rules and procedures laid out in the project-wide QA plan
  - Project-wide Quality Assurance Program DocDB 13093
- All hardware deliverables, data, and testing results are tracked in a database
- Testing/commissioning/production software and firmware are tracked in github repositories
- Blade hardware:
  - Responsible institute validates HW with tagged FW+SW prior to final shipping
- Optical connections: live continuous non-invasive monitoring (eye-diagrams) with on-board Zync applications for Xilinx.
- Firmware & software: follows Fermilab software quality assurance (SQA) (Quality Assurance Manual 12003, 12090)