PIP-II Low Level RF Beam Pattern Generator

Harsh Maniar

PIP-II LLRF Preliminary Design Review

September 9, 2021

A Partnership of:
US/DOE
India/DAE
Italy/INFN
UK/UKRI-STFC
France/CEA, CNRS/IN2P3
Poland/WUST
Outline

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• Documentation Details
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  – Physics Requirements
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• Preliminary Design
  – System Diagram
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• Final Design
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Introduction

• Harsh Maniar, Staff Electrical Engineer L4, Fermilab
  – Education: MSEE (VLSI and Microelectronics), Illinois Institute of Technology, Chicago
  – Experience: 5+ years of Circuit design/ FPGA design experience
  – Fermilab Experience: ~1 year

• Project Responsibilities
  – BPG circuit design and verification
  – FPGA firmware development for arbitrary waveform pattern generation
  – IOC Communication and EPICS user interface development
  – BPG system bench test
  – PIP-II BPG installation
  – Interface with controls system, timing system, MEBT kicker electronics, Booster LLRF system
  – BPG system test at PIP-II
  – System maintenance and technical support
## Documentation Details

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Physics Requirements

- In the PIP-II configuration, the beam will be injected into the Booster from the PIP-II SRF Linac.
- To reduce the impact of the space-charge
  - the PIP-II beam energy was increased to 800 MeV
  - injection will utilize a micro bunch-to-bucket, multi-turn, charge-exchange injection into the Booster utilizing both transverse and longitudinal phase space painting procedures
- To achieve and maintain the Linac beam quality required for the painting
  - the PIP-II beam current was reduced to 2 mA
  - the pulse length was increased to roughly 550 μs
- Values suitable for injection shall be programmable and adjustable by an operator to optimize the final injected distribution.

<table>
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<tr>
<th>Req. #</th>
<th>Description</th>
<th>Value</th>
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<tr>
<td>B8</td>
<td>Booster RF Frequency (injection – extraction)</td>
<td>44.7-52.8 MHz</td>
</tr>
<tr>
<td>L5</td>
<td>Pulse repetition Rate</td>
<td>20 Hz</td>
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<tr>
<td>L6</td>
<td>Average Beam Current during Pulse</td>
<td>2 mA</td>
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<tr>
<td>L8</td>
<td>Max Bunch Repetition Rate</td>
<td>162.5 MHz</td>
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<tr>
<td>L9</td>
<td>Bunch Pattern</td>
<td>Programmable and arbitrary</td>
</tr>
<tr>
<td>L10</td>
<td>RF Frequency</td>
<td>162.5 MHz and harmonics</td>
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From PIP-II GRD: ED0001222
# Key Technical Requirements

<table>
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<th>Interface</th>
<th>Requirement</th>
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<td>Kicker, Booster</td>
<td>The BPG system should generate the stable waveforms for all four output channels with peak-to-peak jitter being sub 100 pico-seconds.</td>
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<tr>
<td>Kicker, Booster</td>
<td>The BPG system generated arbitrary pattern shall maintain extremely flat phase and amplitude response as needed to achieve the jitter requirement across random patterns, over the frequency span from DC to 300 MHz range.</td>
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<td>Kicker</td>
<td>The BPG system shall have a very high timing resolution requirement (~38ps), needed to precisely align the kick waveform with the beam.</td>
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<td>Kicker</td>
<td>The BPG system shall provide an output trigger, precisely aligned with the 162.5 MHz and 1300 MHz RF.</td>
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<td>Booster</td>
<td>The BPG system shall provide a revolution marker for the Booster to identify the position of the gap buckets.</td>
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<td>IOC Controls</td>
<td>The BPG software application shall have an EPICS interface and communication link with IOC.</td>
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<td>MPS</td>
<td>The BPG system must raise a flag for Machine Protection System (MPS) when (1) BPG chassis is not detected by the application (2)if the BPG is not ready to deliver the proper pattern (3)if there is any system failure.</td>
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From BPG TRS: ED0013972
During PIP2IT operation, Beam Pattern Generator **successfully drove the MEBT Kickers** providing many beam patterns including a prototype 550 usec Booster injection pattern.

- Synchronize beam injection and the RF systems between PIP-II Linac and the Booster.
- Synchronization is accomplished by controlling two MEBT beam choppers, which select 162.5MHz beam bunches from the LEBT and RFQ to produce an appropriate reduced beam bunch pattern that enables bucket-to-bucket transfer to the Booster RF at 46.46MHz (84th Revolution Harmonic).
- Reduces the beam current to an average of 2mA over the Booster injection, matching the Linac nominal beam current.
- The Beam Pattern Generator (BPG) is the system that determines the bunch pattern as requested by experiment or by the Booster injection, and provides:
  - drive to the MEBT Fast Kickers
  - the capability to drive the LEBT Chopper
  - the injection RF frequency/phase reference which the Booster will phase lock to during injection signal
  - a sync pulse for the Booster to generate the Booster revolution marker.

Note: Booster injection locking was not implemented.
Preliminary Design: Hardware

- **Arbitrary Waveform Generator (AWG)**
  - Wavepond DAx22000
  - (2) Channel, 2.5 GSPS/ channel, 12-bit D/A resolution
  - DC coupled into 50 ohms; 2, 8 Msamples/ channel
  - 1ppm internal clock stability, <5psec jitter
  - (2) TTL marker outputs
  - Programmable segmentation size, trig, looping etc.
  - Full scale Trise/ Tfall = 180 picoseconds

- **Drive Amplifier Board**
  - Translates 750 mVp-p AWG output into 0-1.3V signal for kicker drive electronics
  - Single ended output into 50 ohms

- **Trigger synchronization board**
  - Receives trigger from timing system, samples to the 162.5 MHz RF clock
  - Contains adjustable delay line to ensure timing meets setup and hold times

- **Power distribution board**
  - Power supply for AWG board, drive amplifier board and trigger synchronization board
External trigger as input in synchronizing circuit, will create an output trigger precisely aligned with the 162.5 MHz and the 1300 MHz RF
Sub 1300 MHz period alignment is done so that the trigger maintains the setup and hold time requirements of the AWG input circuit
Stable AWG output to the order of picoseconds
Fine tuning resolution and precision requirements can be met with the 1.3 GSPS clock rate
This sample rate allows the generation of a 650 MHz bandwidth signal with exact timing and amplitude
Timing resolution ~38 ps, Virtual sampling rate 26 GSPS
Final signals are digitally filtered to below the 650 MHz Nyquist frequency, then downsampled to 1.3 GSPS
Analog reconstruction filter for DAC outputs
Preliminary Design: LabVIEW application

- CSV pattern file, 0: Beam bunch allowed to pass, 1: Beam bunch to be kicked out
- Each element: 6.15 ns, Sampling clock rate: 1300 MHz
- Key features: rising edge delay, falling edge advance, channel delay, phase flip
Kicker drive channel 2 delayed by 1 µs with 10 µs pattern, compared to channel 1
- Pattern contains different combinations of 0s (Beam pass) and 1s (Beam kick)
- Pulse width: 6.15 ns (1/162.5 MHz), can be adjusted using rising edge delay/ falling edge advance
Preliminary Design: Results (Jitter measurement)

- BPG Output channel measured over few minutes span with infinite persistence, triggered on 1.3 GHz sample clock
- Complex pattern with beam kick and pass combinations
- Peak to peak electronic jitter and system dispersion: $\sim 85$ps (p-p), measured at falling and rising edge crossover
Final Design: Features

FPGA board
- 4 output channels and IOC communication
- Generates waveforms for fast kickers, synchronized to 1.3 GHz sample clock
- Supports 75ms of beam chopping waveforms
- (4) channel, > 1.3 GSPS/channel, min. 12-Bit D/A resolution
- (6) channel, > 1.3 GSPS/channel, 14-bit A/D resolution
  - 4 ADC channels for kickers, 1 for each coil
  - 1 ADC channels for Wall current monitor
  - 1 spare ADC channel
- DC Coupled into 50 ohms
- (4) TTL marker outputs

IOC Communication
- All GUI features will be integrated into an EPICS application in the Input-Output Controller (IOC)
- The software shall provide status indicators for communication link between BPG hardware and BPG application on EPICS main page

MPS Communication
- The BPG system must raise a flag for Machine Protection System (MPS) when the BPG chassis is not detected by the application or if the BPG is not ready to deliver the proper pattern or if there is any system failure
Wavepond DAx22000
• Chase Scientific, Used in BPG preliminary design
• 2 channel, 2.5 GSPS/channel, 12-bit D/A
• DC coupled into 50 ohms
• 2 TTL marker output
• Programmable segmentation size, trig, looping etc
• LabVIEW support
• End of life product; Less flexibility for firmware development, IOC/EPICS communication

Arb Rider AWG-5000 series
• Active technologies AWG
• 4 channel, 6 GSPS
• 16-bits resolution, Fmax= 2 GHz
• Less flexibility for firmware modification
• Difficult to integrate with PIP-II control system

Custom Baseboard with FPGA SoM
• Baseboard contains data converters, clocking, power, I/O, but simplified
• ReflexCES Arria10 FPGA SoM board
• DACs: (4) channels, 2.8GSa/s, 16-bit (AD9144 or similar)
• ADCs: (4) channels, 3.0GSa/s, 14-bit (AD9208 or similar)
• Analog Front/Back Ends can be configurable

Xilinx ZCU RFSoC
• ZCU208 Gen 3, 6 GHz Zync Ultrascale+ RFSoC FPGA
• 12-bit ADCs, 5 GSPS, 14-bit DACs, 10 GSPS
• RJ45 communication for IOC/EPICS
• 4 GB DDR4
• XM500 RFMC plug-in card with baluns, pad attenuators and SMA connectors
• Less hardware development efforts required, more focus on firmware, signal processing and user interface

Intel RFSoC
• Up to 64 GSPS, integrated ADC/DACs
• Eliminates the JESD204 interface, reduce system power
• Smaller footprint and reduced complexity
• Product announced but not in market yet
• Benefits: Most LLRF FPGAs use Intel technology and Quartus IP cores, Can be re-used for BPG firmware development
Final Design: Next Steps

- FPGA firmware development
  - Pattern generation
  - Digital signal processing
  - Memory storage, link multiple patterns
- IOC communication
  - FPGA network communication
  - EPICS user interface
- MPS communication

- Hardware changes: Update to the latest ICs, devices etc.
  - Driver amplifier board
  - Trigger synchronization board
  - Power distribution board

- Chassis assembly
- Bench testing
  - Pattern generation
  - Channel delay, rising/ falling edge adjustments: resolution
  - Electronic system jitter
- PIP-II installation
- System testing
  - Test MEBT Kickers interface
  - Test Booster interface
  - Test IOC interface
Bench Test/ QA

• Bench Test Procedure
  – Visual inspection of hardware parts
  – Verify pattern generation:
    • Input parameters on EPICS user interface
    • Pattern generation logic in FPGA firmware
    • Pattern play out on four output channels: Default pulse width 6.15ns
    • Beam pass: 0-0.5 volts, Beam kick: 1.2-1.5 volts
    • Electronic system jitter: <100ps
  – Adjust channel delay, rising/ falling edges
    • Timing resolution: ~38ps
  – Verify marker outputs
  – Verify output trigger precisely aligned with 162.5 MHz clock
  – Verify network communication and EPICS user interface features on development IOC
  – Verify MPS communication PV functionality

• Quality Assurance
  – PIP-II LLRF systems quality control plan (Document #5496-v1)
Summary

- Prototype BPG, Successful operation at PIP2IT
  - Performance met all the requirements for arbitrary waveform generation
  - Wavepond DAx22000 used as AWG
  - Python script, LabVIEW application: was able to make changes as per operational needs during PIP2IT run
  - Achieved 38.46ps resolution and ~85ps electronic system jitter
  - AWG board: end of life product, will be replaced with FPGA board and firmware
  - Driver amplifier board, trigger sync board and power distribution board can be reused
- Final design
  - Develop FPGA firmware solution for arbitrary waveform pattern generation
  - Reuse other hardware with latest components, minimal changes to circuit
  - IOC/ EPICS interface for PIP-II controls
  - MPS communication
  - Less hardware design challenges, focus will be on firmware changes, signal processing algorithms and user interface

Thank you!
Backup Slides
Final Design: PIP-II Linac & Booster Interface

BOOSTER INTERFACE TO PIP-II LINAC AND TIMING

V9 7/26/21

Brian Cheater, Ed Cullen, Bill Peluso, Brian Shafiekhah, Hyomin Yoon, Chungyang Tan

Timing System

Booster Interface to PIP-II Linac and Timing

9 MHz

10 MHz

10 MHz

Booster RF signal

Located in the BMA Room

Booster kicker/pitchers/extraction

Measurement sensor? operation?

Beam Pattern Generator (BPG)

Booster LLRF

56 MHz

106 MHz

106 MHz

44 MHz

9 MHz

Injection sequence

PIP-II LLRF Beam Pattern Generator

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Final Design: Booster Interface

- Linac provides
  - 44.46 MHz RF to Booster (adjustable)
  - Revolution marker reset at the start of injection
  - Beam selected to hit proper phase of the Booster RF buckets

Reference: Booster interface to PIP-II Linac and Timing drawing v8, B.Chase, Ed Cullerton
BPG Function – LINAC Bunch Selection

Trigger From Timing System

Trigger is synchronized, but absolute timing can walk over clock edges due to systematic conditions

Therefore, the BPG resynchronizes the trigger to the 162.5 MHz accelerator RF

Synchronized Trigger Pulse

Time Resolution <50 ps

162.5 MHz Beam Bunch

BPG Pattern (ideal) Selecting every other bunch here (black signal)

BPG Pattern (ideal) Selecting every other bunch here (black signal)

Beam Bunch (6.154 ns spacing)

Common Delay

Delay between Helix

Rising Edge Adjustment

Falling Edge Adjustment

The BPG provides an adjustable master delay between the trigger and start of the bunch pattern

BPG Pattern (actual) Showing ability to adjust rising and falling edges (same for all bunches) / (blue signal) / this allows us to select where in the bucket the bunch is placed