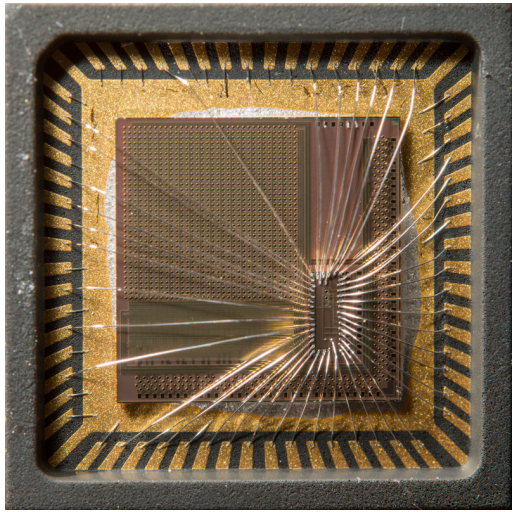
Fermilab Microelectronics Initiative
ASIC Research & Development Department

Farah Fahim & Jim Hirschauer

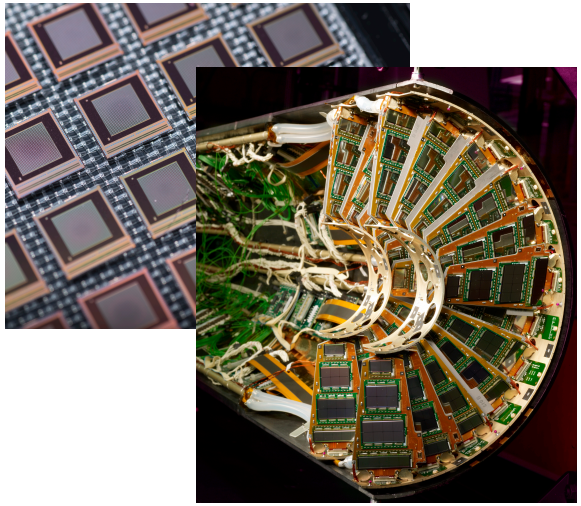
ASIC Design mission at Fermilab

ACADEMIC RESEARCH



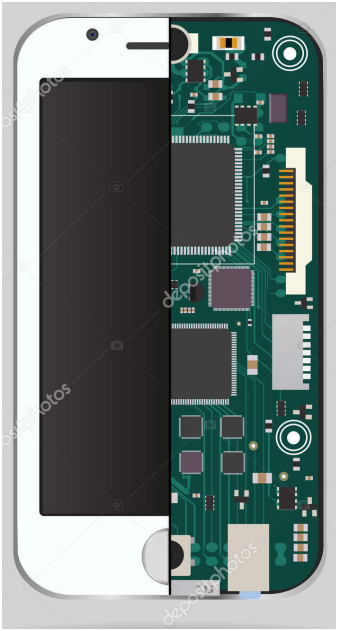
- Support interdisciplinary research
- Enables new scientific discovery and foundational engineering
- Novel solutions
- Mission: new knowledge and education of students

NATIONAL LABS: ADVANCED SCIENTIFIC INSTRUMENTATION



- Support scientific experiments operating in extreme environments
- Mid-size scaling for large experiments
- Mission: robust performance over several decades

INDUSTRY – PRODUCT DRIVEN



- Support consumer electronics
- Mature designs
- Mission: incremental product driven design

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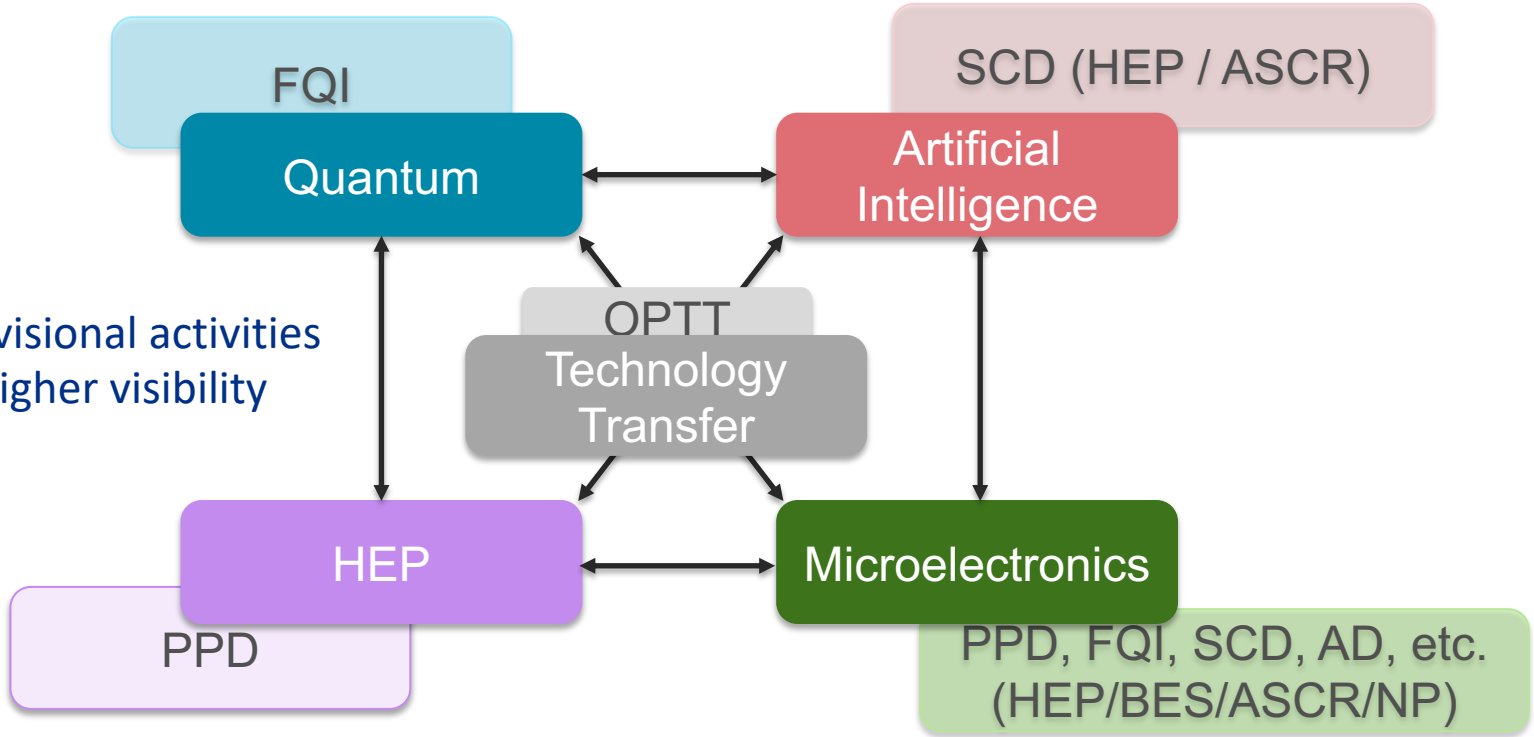
Fermilab ASIC Design Future

- Cross divisional activities
- Needs higher visibility



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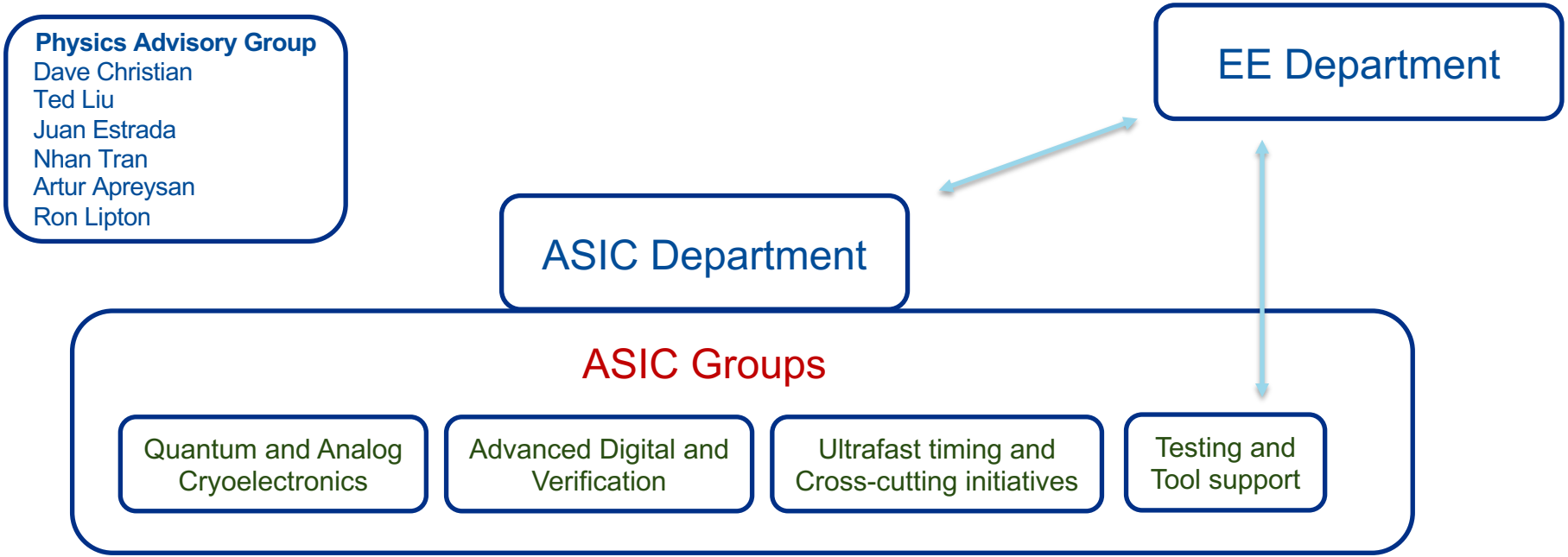
Strategic Structure



- 16 ASIC designers
- 1 scientist
- 1 Application Physicist
- 1 test engineer, 1 engineering associate

Currently recruiting for 3 more positions:
2 ASIC designers + 1 Application Physicists

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HEP – CMS & DUNE

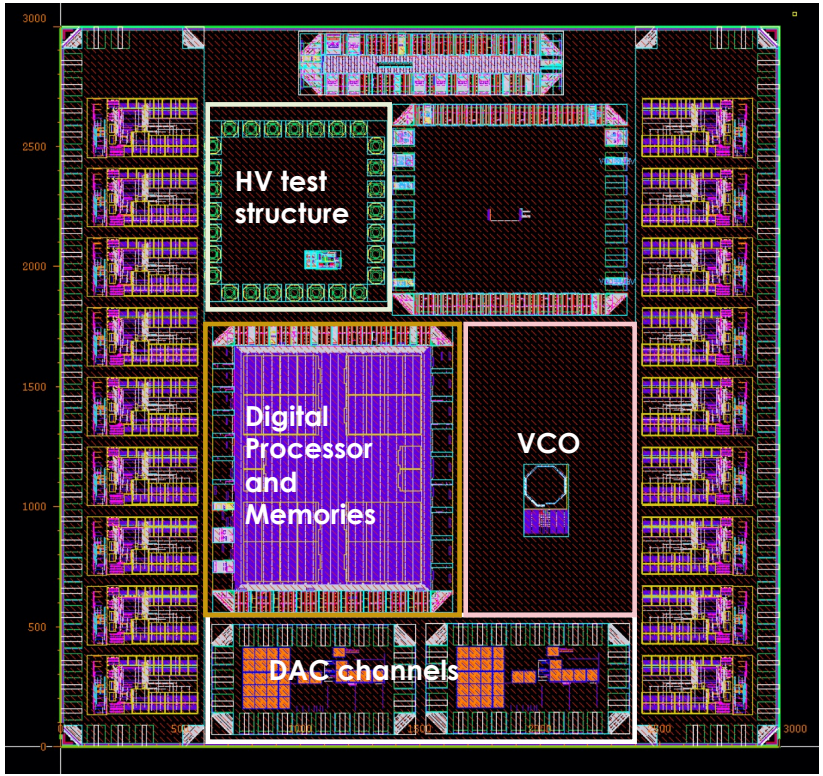
Operation in extreme conditions – high ionizing radiation, cryogenic operation with long lifetime requirements

- ETROC: Timing layer ASIC for CMS LGAD detectors (picosecond timing chip in collaboration with SMU)
- ECON (T&D) – High Granularity Calorimeter Concentrator chip
- COLDATA/ COLDADC –DUNE data concentrator and ADC chip (completed in FY 21)

Quantum

Deep cryogenic electronics on advanced technology nodes

- Cryogenic modelling for development of 4K process design kit for GF 22 FDX
- QSC: Quantum Science center (National Quantum Initiative center)
  - Ion trap based Quantum Simulator: Cryoelectronics Controller – Low noise, high speed DACs
- QuantiSed
  - Control electronics for Compact Optical Atomic Clocks with MIT LL
  - SNSPD readout with JPL, GT and Caltech (Quantum Communication). Demonstrated cryo LNA performance.



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Artificial Intelligence/ Machine Learning

Hardware - software codesign, driven by edge compute: Processing data at source, real-time feedback and control. Neuromorphic low power architectures with integrated memory

- Low-power, Low-latency Autoencoder
  - ECON (65 nm, test vehicle for implementation: with NU & U.Columbia)
  - Working with Mentor Graphics (hls4ml) to integrate TMR in HLS tool
- Cryo AI: Quantum ML for controls and readout
  - Ultra low power implementation in GF 22 nm
  - RISC V processor and Network on chip (Next gen R&D for both HEP and Quantum applications)
- Radhard/ cryogenic eFPGA on-chip (backend of ASIC) – working with industry to develop IP

Pixel Detectors

Gigapixel/ Megapixel camera systems – high resolution, low power, operating in extreme conditions

- Device Physics – New detector technology: Detector R&D funds
  - Skipper CCD in CMOS – collaboration with SLAC and Tower Semiconductor
  - Ultrafast skipper CCD (SiSeRo) – collaboration with MIT LL (high gain, high speed, non-destructive readout)

- Readout of CCD (Dark matter detection OSCURO)
  - MIDNA: Low Noise readout of CCDs (Corelated multi sampling amplifier with analog averaging). Recently demonstrated single photon counting

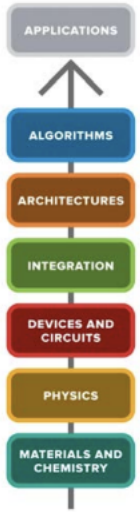
- AI_pixel_detector: 1Mfps megapixel detector
  - SLAC (BES) – seeding activity
- Qpix: R&D for DUNE far detector with U.Hawaii, U. Penn & UTA

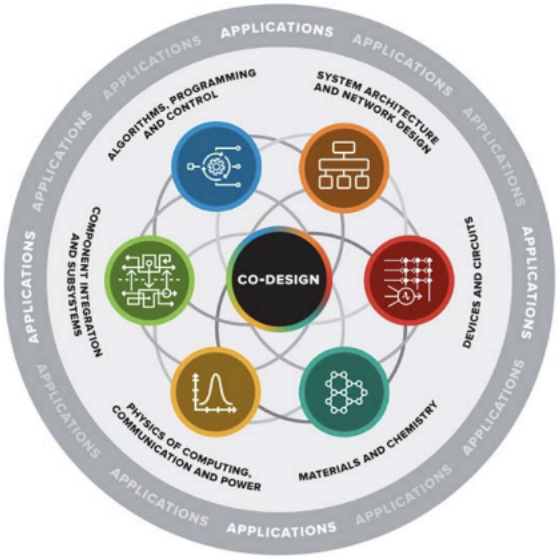
New Microelectronics Initiative

Fermilab led co-design team: PI – Davide Braga

Hybrid cryogenic detectors enabled by new materials and fabrication processes

- FNAL : DM application, skipper-in-CMOS, cryo CMOS, system integration
- Labs : **ANL/JPL/NIST (SNSPDs)**, SLAC (skipper readout)
- Academia: MIT/Caltech (SNSPDs)
- Industry: GF (cryo CMOS), Tower Semiconductor (skipper-in-CMOS), Synopsys (cryo modelling)
- HEP, BES, FES, ASCR





Microelectronics ECA (1st in HEP)

- Radhard neural networks for frontend data processing
- Beyond CMOS processing – Blue sky R&D
- Phase III pixel detector R&D
- Working in conjunction with ORNL led co-design team

DOE Microelectronics centers likely to be announced in FY 22

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Focus on both: Engineering Projects and R&D

- **Strong focus on getting a process in place for projects**
  - Specifications
  - Design reviews
  - Documentation
  - COMMUNICATION

- **Flexibility for R&D**
  - Continuous R&D effort
  - Funding for development
  - Collaboration with universities
  - Demonstrators for next generation of projects

Collaboration with Universities

- Create a model comparable to CERN [20 staff + 20 students]
  - Enables knowledge transfer
  - Creates a culture of teaching and learning
  - Research aspect of the development
  - Workforce development

- Strong collaboration with NU – EE department (PhD students based at Fermilab)
- Started ASIC Design Associate position – 5 summer interns last year
- Started collaborations with Columbia U., EPFL, Georgia Tech, UCSB, Stonybrook U.,

Collaboration with industry

- Started joint development with x on cryoelectronics for Quantum Systems
- In discussion with several other companies including NVIDIA, Honeywell
- Supporting several DOE SBIR companies

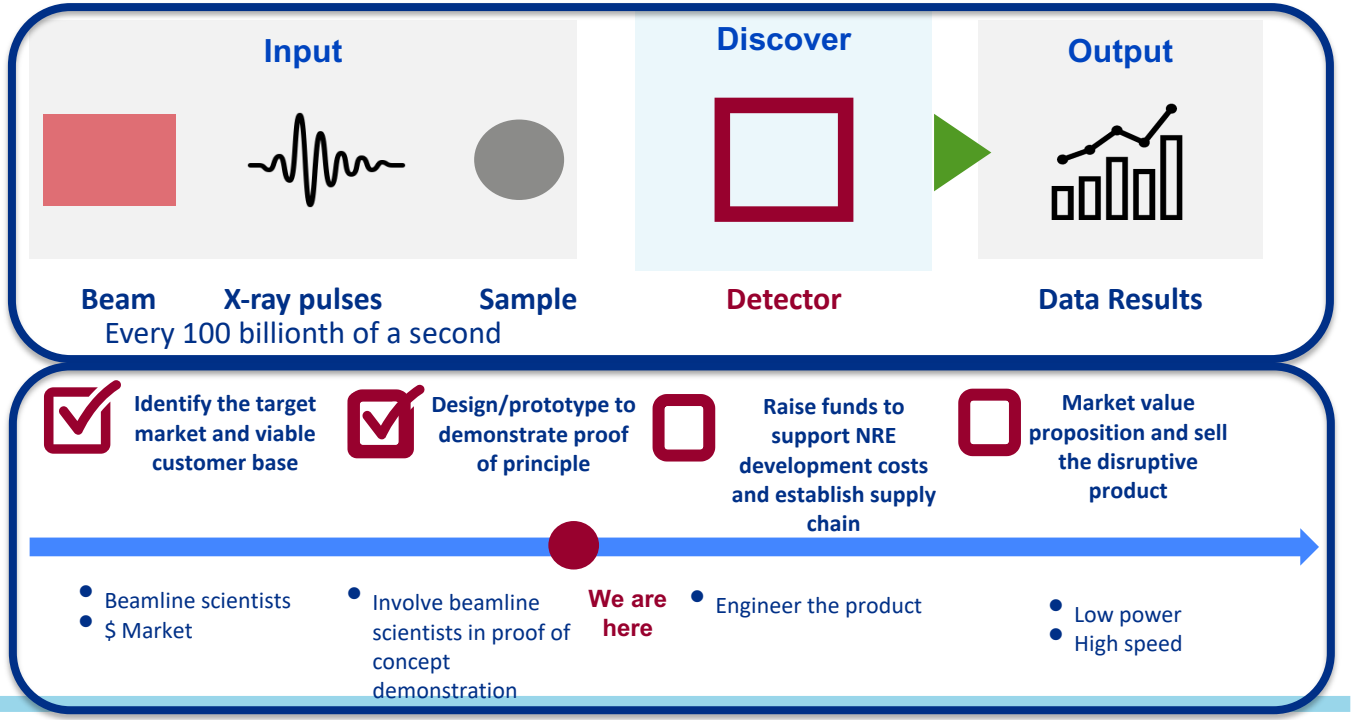
- Involved in Snowmass process (co-lead of Application and Industry)
  - DOE CAD-EDA tool initiative for low cost, higher volume tools for scientific research
  - Engaging CAD vendors to support microelectronics for DOE

Technology Transfer

Commercializing - Participated in the Innovation Discovery Event

Innovation fund and other Polsky programs

Lab innovation fellow (Shaorui Li)



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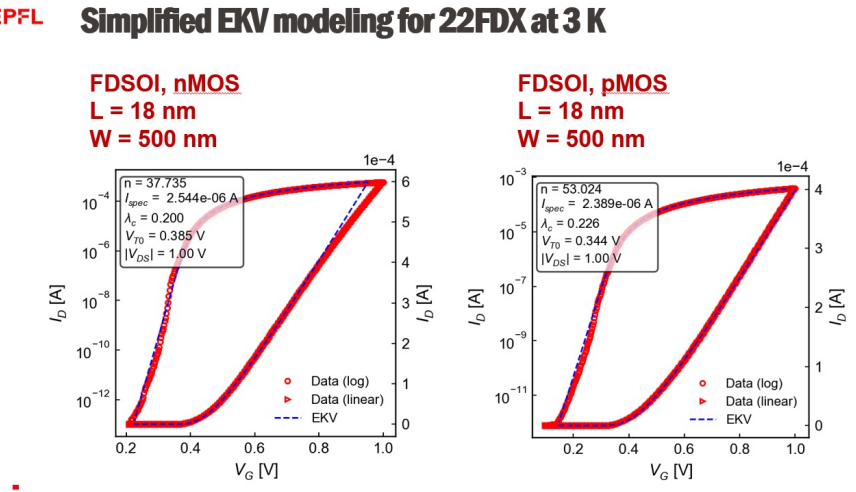
Backup

22FDX cryo testing and characterization

- Collaboration/subcontract with EPFL progressing well

1. Development of test structure for RF/low-freq noise characterization of transistor:
   - Design on schedule for Nov tapeout
2. Test plan for device measurement and model extraction late 2021/early 2022
   - Some delay due to availability of cryo probe station
   - Test plan agreed

- Good working relation with GlobalFoundries
- Initial simplified models

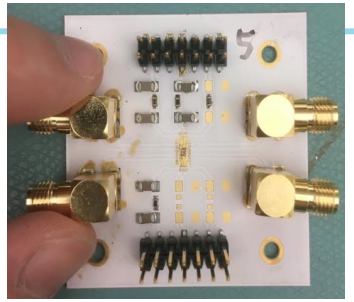


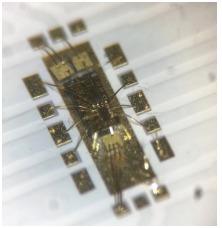
NECQST: Novel Electronics for Cryogenic Quantum Sensors Technology

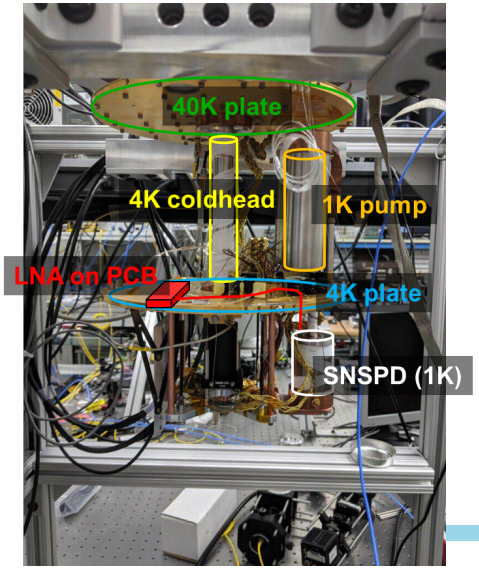
D. Braga (FNAL), J. Cressler (Georgia Tech), M. Shaw (JPL), M. Spiropulu (Caltech)

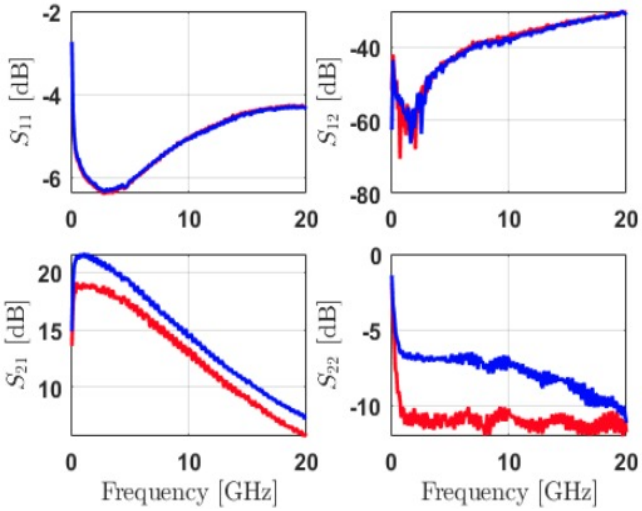
- Cryogenic (4K) SiGe HBT Low-Noise Amplifier (LNA), optimized for low-jitter low-power readout of Superconducting Nanowire Single Photon Detectors (**SNSPD**s).

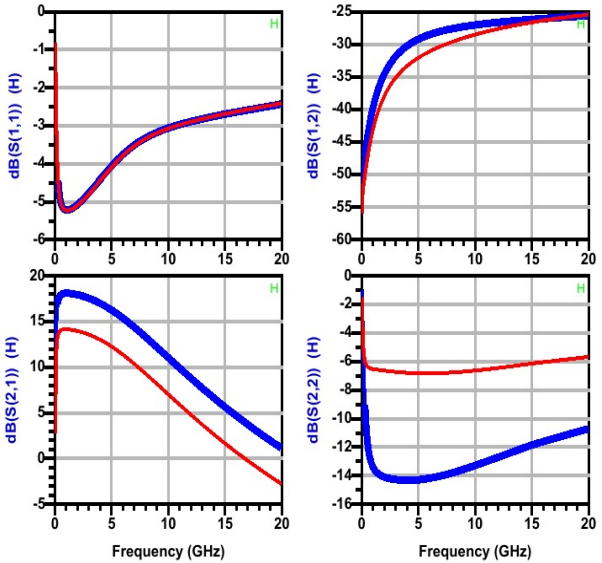
- Chip results without SNSPD are promising (been measured in both cold and warm)
- Currently the PCB for SNSPD connected to LNA is not working, which needs to be fixed and retested











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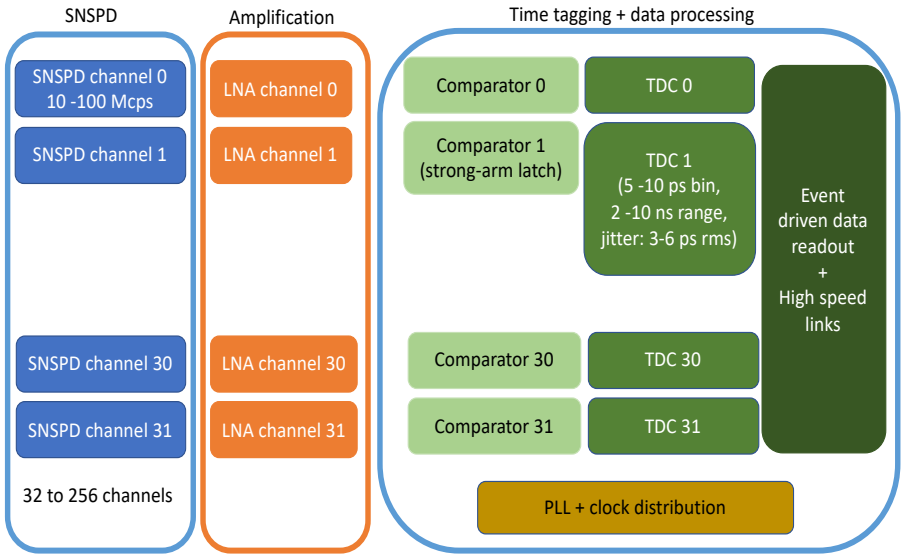
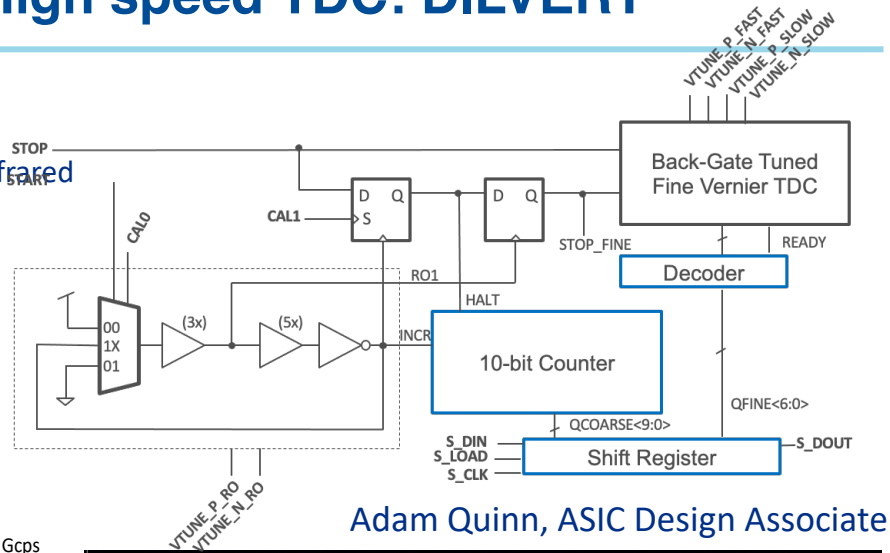
Projects	Designers and Circuit Blocks	Current status (Sept. 10)	Action Items
ACC1 (3x0.5x2 mm^2)	Hongzhi: DAC w/ auto-correction [Optional: DAC LSB mismatch test structure]	-Analog schematics updated w/ new pdk models). -Analog layout ~40% ready?	-Complete analog layout. --Complete I/O ring.
	Chinar: Encoder	-Architecture ready. -Refine RTL code.	-Complete RTL. -Digital PnR
DILVERT (1x0.3 mm^2, 22 pads)	Adam: 16b TDC	-Analog schematics ready. -Analog layout 90% ready. -Complete Analog I/O pads. -Digital RTL ready.	-Digital PnR
LDRD: Characterization & Modeling (1x1 mm^2)	Antonio (EPFL): noise test structures	-Schematics ready. -Layout ~80% ready?	-Complete top-level layout. -Complete digital selector
	Hungchi (EPFL): EKV modeling	-Testing time reserved.	-Cryo characterization of GF test devices. -Extract simple EKV models.
CryoAI (1.2x1.2 mm^2?)	Manu/Chinar/Farah: memory & processor	-DCO done -RTL ready. ML algorithm ready. -Digital flow for PnR ready	-Digital PnR will start upon clean flow. -Recompiling memory -Voltus flow
CITC1 (DAC: 1.8x1 mm^2 & VCO: 1x1.2 mm^2)	Zexi/Sharoui: Cryo HV DAC [Optional: DAC LSB mismatch test structure]	-Schematics updated w/ new pdk models). -Layout ~20% ready?	-Complete analog layout. -Complete I/O ring.
	Xiaoran: low phase-noise LC-VCO	-Schematics ready. -VCO core layout ~80% ready?	-Complete analog layout. -Complete I/O ring.
ADC (1x1 mm^2-> 1x0.7 mm^2?)	Troy: 12b capacitive DAC for SAR ADC	-Schematics ready. -Layout ~50% ready?	-Complete analog and top-level layout. -Complete I/O ring.

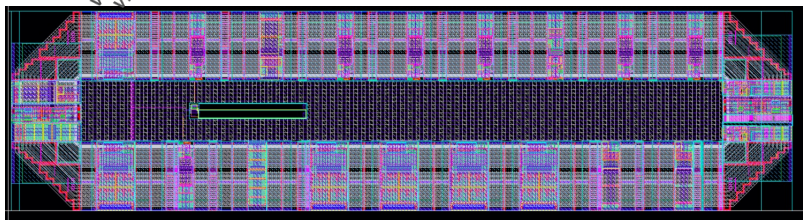
Quantum communication: SNSPD – High speed TDC: DILVERT

SNSPD best performance – (operating at 1 - 4K)
Time-correlated single photon counting from the deep UV to the mid-infrared
Extremely low dark counts and very high precision
QUANTUM INTERNET - High bandwidth communication





Adam Quinn, ASIC Design Associate



Two step TDC:16b; 2.2 ps resolution; 10 ns range

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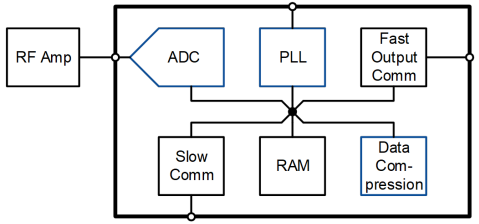
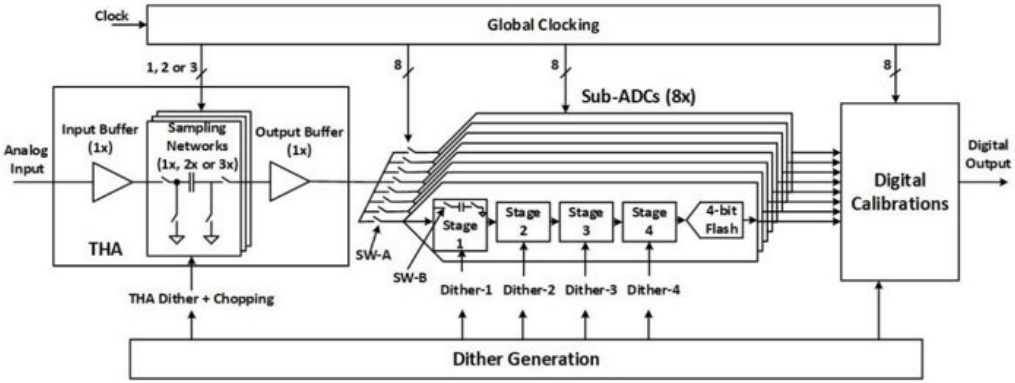
10 GSPS ADC operating at 4K with Microsoft

Troy England

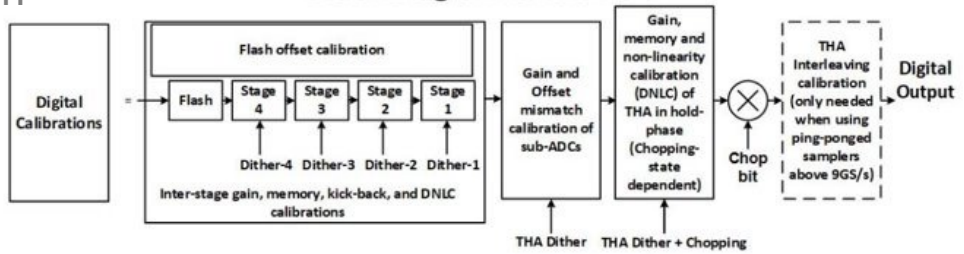
- Time interleaved 1GSPS SAR sub-ADCs

- Progress:
  - Further iterating architecture
  - CDAC schematic and layout iteration
  - CDAC tapeout in Nov to study mismatch effect on resolution o ADC





Block Diagram of the ADC



Block Diagram of the Digital Calibrations

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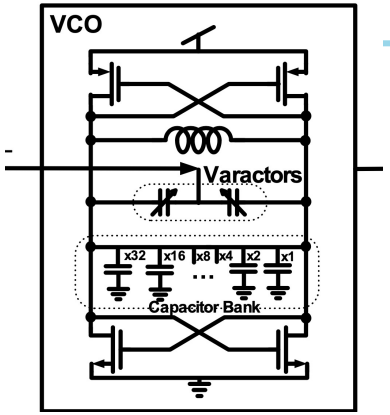
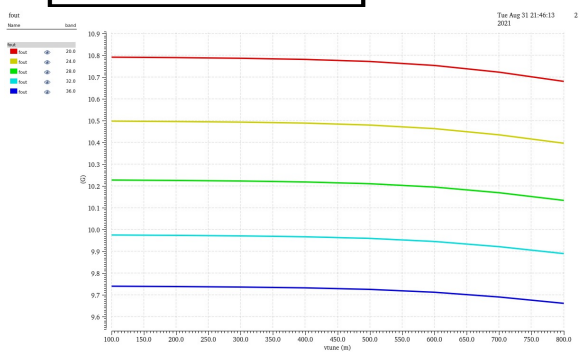
LC-VCO Test Structure

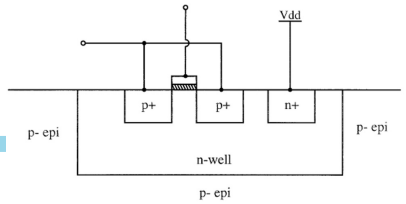
Xiaoran Wang

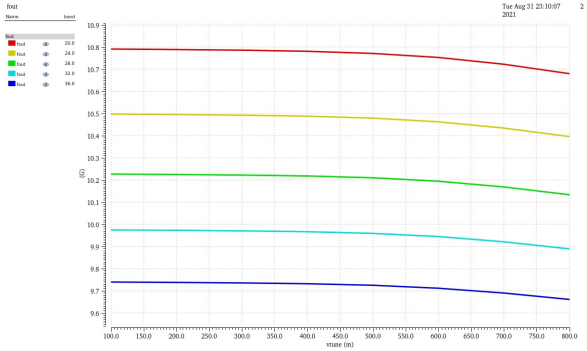


- High-Speed (**10GHz**) low jitter LC VCO
- Working at **cryogenic temperature**.
- **Double biasing** (Top PMOS and Bottom NMOS) for better phase noise performance
- **Coarse tuning: MOM Cap** bank with 32/64 band for high precision and high resolution.
- **Fine tuning:** Test structure for varactors: MOS D=S=B/MOS Inversion mode/MOS accumulation mode
- **Large signal effects** (voltage amplitude varies) on tuning range (Kvco) and linearity

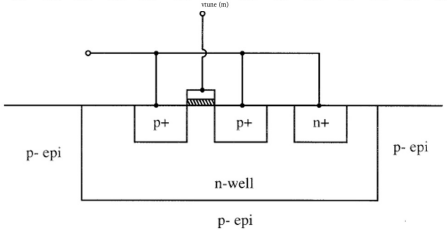


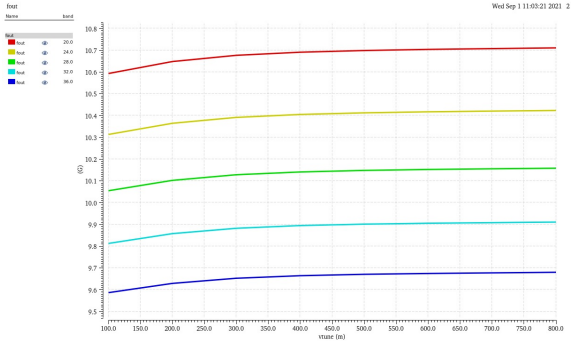
PMOS Inversion-mode Varactor



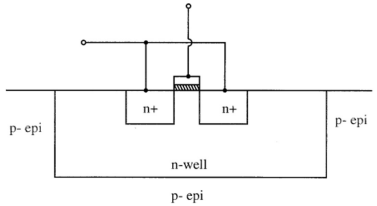


PMOS D=S=B Varactor





NCAP in N-well Accumulation-mode Varactor



Cryogenic Electronics at 4K for Ion Traps

- **Joint Team**: Shaorui Li, Zexi Liu, Xiaoran Wang, Farah Fahim (**FNAL**); Chris Seck, Raphael Pooser (**ORNL**)
- S. Li, "Challenges in developing cryoelectronics for ion-trap-based quantum computing", in *Cryoelectronics Workshop, Tuesday 10/19, 3:15 - 4 pm (MT)*

Specifications	Target for 1st Prototype	Long-Term goal
Output Voltage Range	+/- 6 V (limited by process device maturity)	+/- 10 V
Voltage resolution	1 mV (12 V/ 1 mV -> 14 bit)	1 mV (20 V / 1 mV -> 15 bit)
Output Noise	< 100 nV/srqt(Hz) @ 0.5-5MHz	~1 nV/sqrt(Hz) @ 0.5-5MHz
Updating Rate	1-10 MS/s	100 MS/s
Total average power	< 5 mW/DAC	~500 mW for 100 Ch.

Design Challenges:

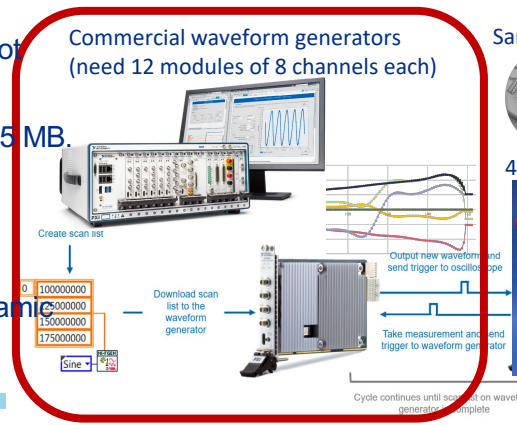
- Low output noise: < 100nV/sqrt(Hz) around a wide frequency range (0.5 – 5 MHz) and at low frequency.
- Low power: < 5 mW/DAC (limited by the cooling power of the cryostat) while driving a wide rage of load capacitance (70 – 1800 pF) of +/- 10 V full scale at 10-100 MHz waveform updating rate.
- High resolution: 14-16 bit for precise control and not disturbing RF electrodes.
- Memory: 100 electrodes * 14 bit * 5000 points ~ 2.5 MB.

Our Unique Solutions:

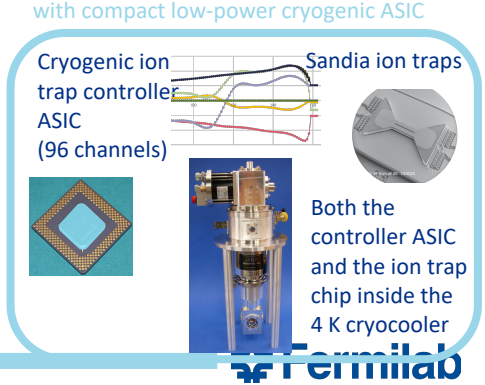
- Low-noise charge-mode DAC with calibration
- High-voltage devices (LDMOS/BOXFET) with dynamic supply.
- High-density memory (eMRAM).

Ion Traps Controller: Room vs. Cryogenic Electronics

with expensive and bulky room-operation electronics



with compact low-power cryogenic ASIC



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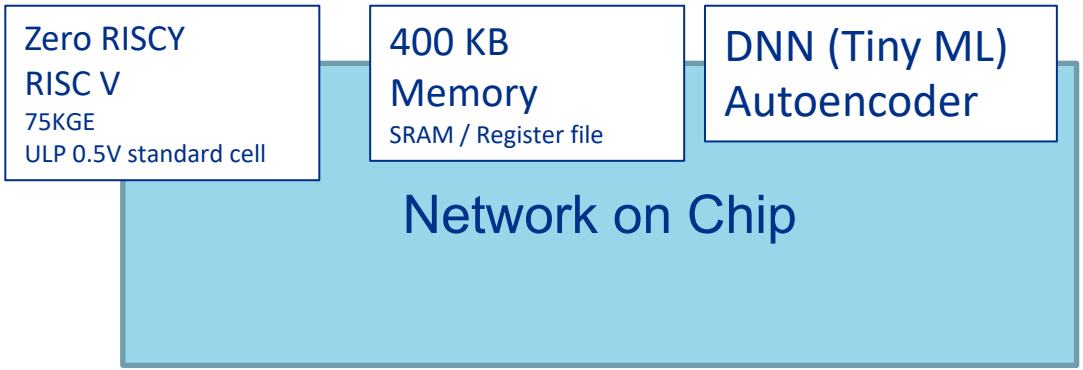
Cryo AI digital test ASIC

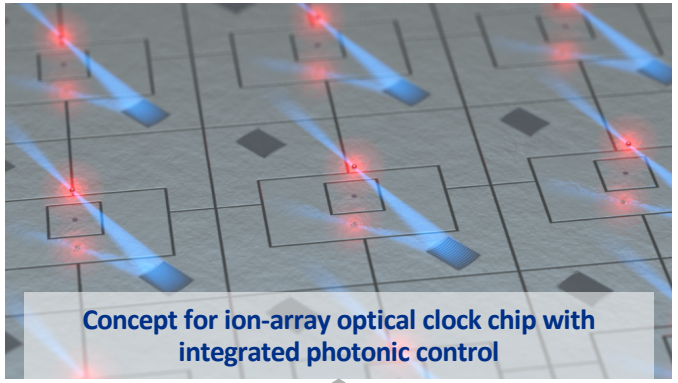
Columbia U., Manu Valentin, Chinar Syal

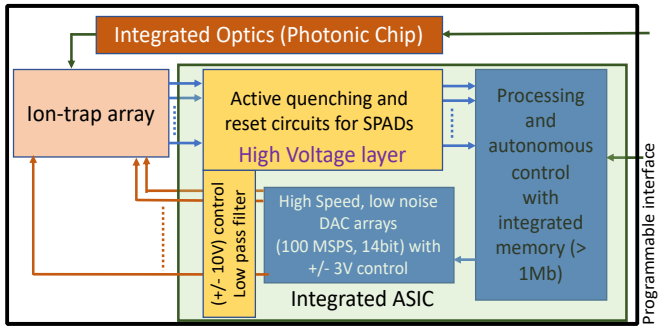
- RISC V processor to control the DNN accelerator
- Manages data and maintains input/output average to flag an anomaly
- Anomaly detector
- Accelerator is reconfigurable and weights can be reprogrammed
- Utilizes SLVT and LVT library for low power performance



Integrated Electronics/Photonics to Enable Portable Trapped-Ion Optical Clocks

- Motivation: high-precision, fieldable clocks for ultra-light dark matter search
- Developing technology for portable optical clocks based on trapped Sr^+ ions
  - Ion array with trap-chip integrated electronic and photonic control elements
  - In-chip optics for individual ion-site addressing
  - Integrated SPADs for ion-state readout
  - Electronics to update trapping potentials to reduce systematic uncertainties; also for biasing and readout of SPADs
  - 3D integration of all control elements
  - In-loop, on-chip processing based on measurements: reduced external-control overhead





Collaboration partners:

MIT LINCOLN LABORATORY

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Funded by HEP-QIS QuantISED

John Chiaverini, Robert McConnell

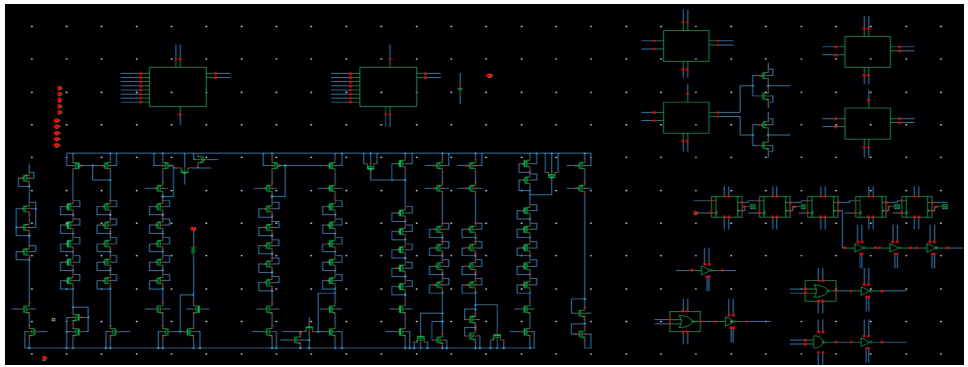
Farah Fahim, Shaorui Li, Hongzhi Sun

Compact Optical Atomic Clocks

Hongzhi Sun, Chinar Syal

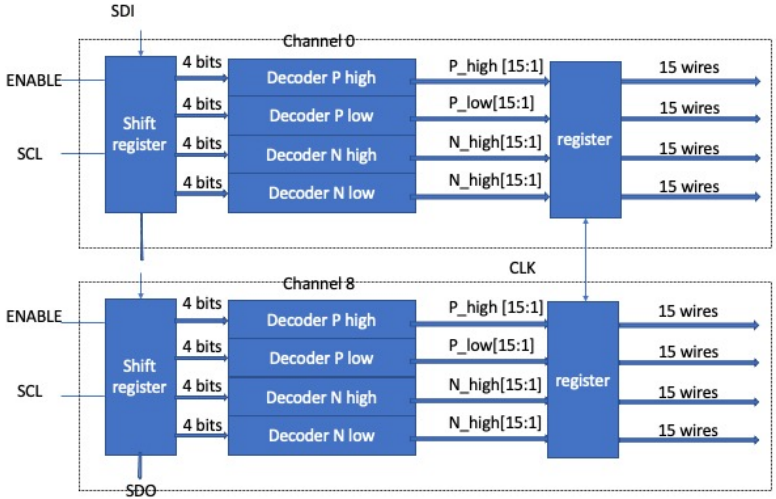
Analog part:

- Updated the schematics based on the latest design kit from the foundry
- Circuits re-simulated and modified based on latest model
- Block-level layout on going
- Targeting taping out in November



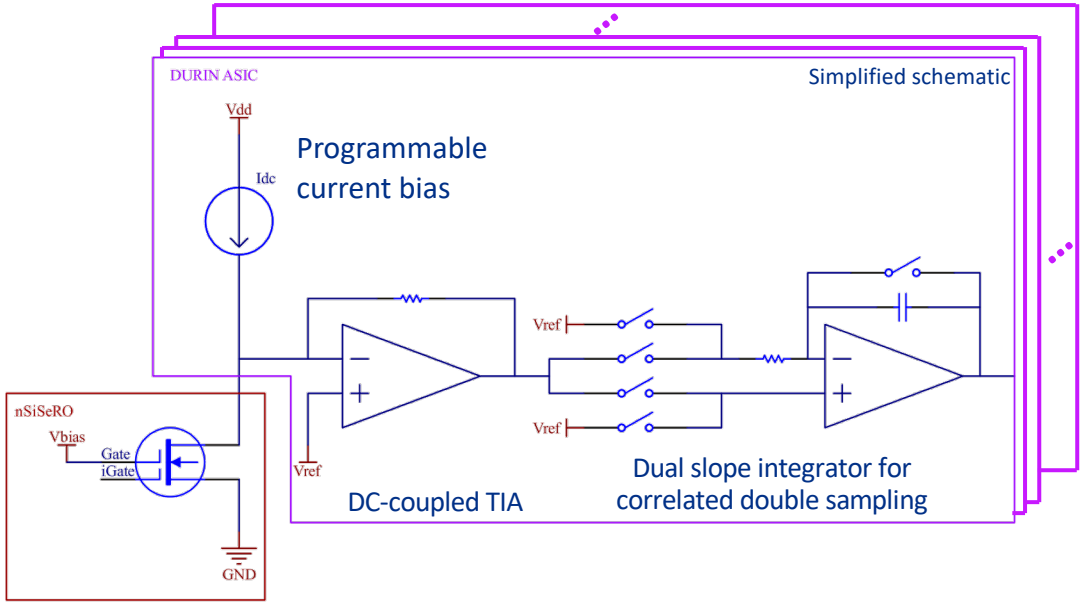
Digital part:

- Initial draft of the architecture with Verilog code
- Working with Chinar for digital implementation.



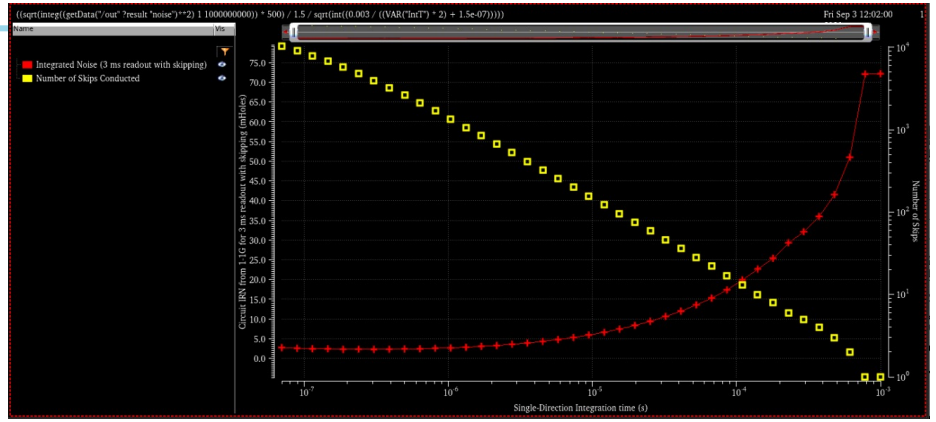
DURIN ASIC (Dark-matter Use-case Readout ASIC Integrating N-SiSeRo's)

- 65nm CMOS, multichannel ASIC
- SiSeRO operating voltage allows for DC coupled readout
- Baseline of 2MHz/500ns single read (incl. CDS), up to 5MHz/100ns
- Drain readout for improved speed
- DC-coupled OTA (new) + dual slope integrator readout for CDS (from MIDNA)
- Programmable current bias to remove offset
- Cascode transistor



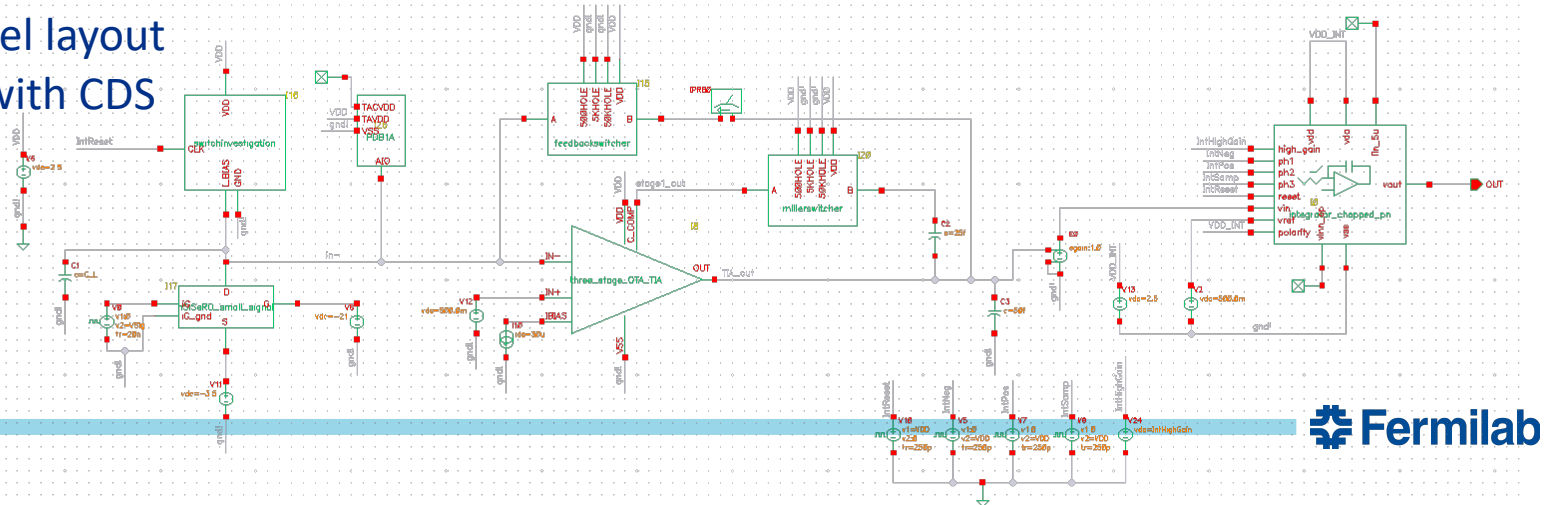
Status:

- Schematic completed for active cascode, preamplifier, low-noise biasing mirror
- 3 programmable gain ranges (500, 5000, 50000 h+)
- Sub-h+ single-shot noise
- Integrator currently off-chip



Next:

- Multichannel layout
- Integrator with CDS



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Skipper CMOS

Ben Parpillon, SLAC, Miguel Sofo Haro, Fabricio Alcalde

Motivation

- **CCDs have been critical to a broad range of science over the last half century – recognized by 2009 Nobel Prize**
  - CCD foundries have been decreasing in number due to declining commercial interest
  - CCDs have no on-chip processing ability
  - CCDs are slow
  - Skipper CCDs have demonstrated remarkable noise levels through repeated non-destructive readout
- **This project combines the intelligence of CMOS and the low noise from a Skipper non-destructive readout fabricated in a high-volume foundry**

- **Physics Applications**
  - **Low mass dark matter searches**
  - **Astrophysics: deep measurements of dark energy and dark matter signatures**
  - **Single-photon quantum sensing**

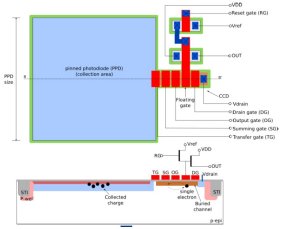
Project Overview

1. Design and Fabricate a CIS test chip.
   → **Tapeout target: 11/15/21**
2. Demonstrate low noise capabilities for a single measurement (target < 2e- RMS)
3. Demonstrate photon counting with micro-second scale readout time capabilities
4. Fabricate and characterize pixel variations and process splitting for the pixel structure.
   → **Optimize Quantum Efficiency of the pixel**
   → **Identify best pixel structure**
   → **improve modeling**

Innovation

- **CCNDR**: skipper CCD in CMOS with Non-Destructive Readout

- **Pixel Technology**: Combining Pinned Photodiode (low noise, hgih gain sensor, demonstrated 0.7e- noise) with CCD-like gate structure for non-destructive read



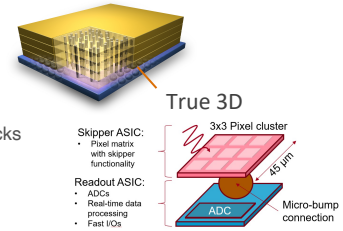
- **180nm CIS process**
  - ✓ High-throughput, commercial foundry
  - ✓ High readout parallelization capabilities
  - ✓ Low noise/ high SNR for fewer averages
  - ✓ **> 3 order of magnitude faster readout time than CCD***
  - ✓ Finer feature size

- **Fabrication**: Back side Illuminated for high quantum efficiency

Ultimate Goal

<u>If our test chip is successful :</u>

- Upgrade the design and build a Single Photon CIS circuit:
  1. Leveraging accurate models and best pixel variation
  2. Leveraging best analog front-end architecture and IP blocks
  3. Implement new features (e.g: on the fly gain selection)



- Hybridize the fabrication (3D or bump bonding)
  1. Pixel on its own tier : Improved detection area
  2. Highly parallel architecture -> implementing amplification and ADC every 3x3 pixels could enable 1Kfps readout speed capabilities
  3. Possibility to design the ROIC in a finer process node (e.g.: 65nm or lower)

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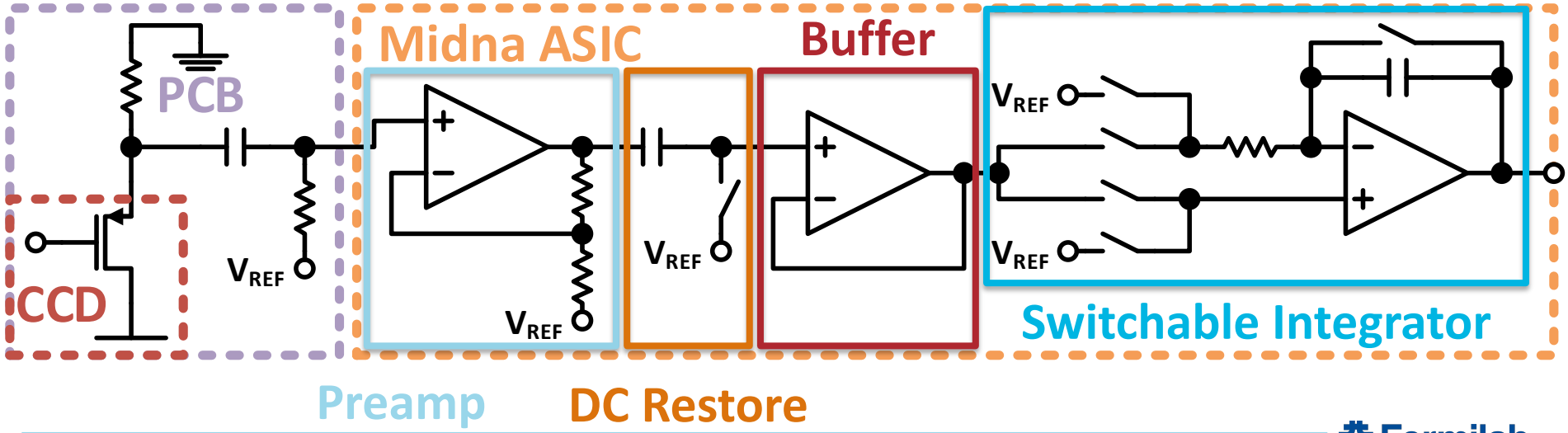
MIDNA

- Preamplifier largely responsible for noise performance drives power consumption
- DC Restore prevents the saturation of the integrator sticking baseline to V_{REF}
- Buffer to provide the current necessary for the Integrator
- Switchable Integrator to implement CDS on chip with efficient bandwidth



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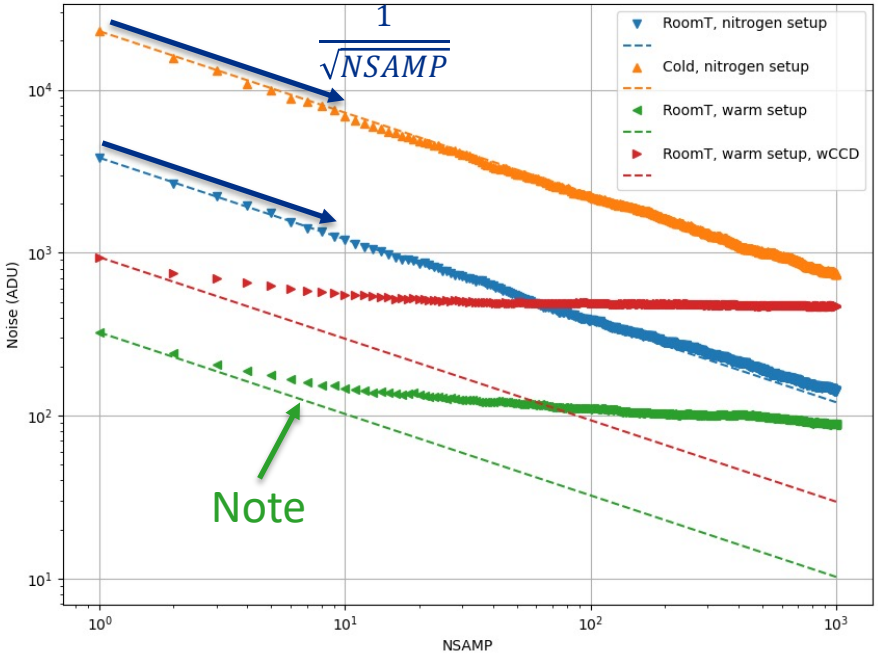
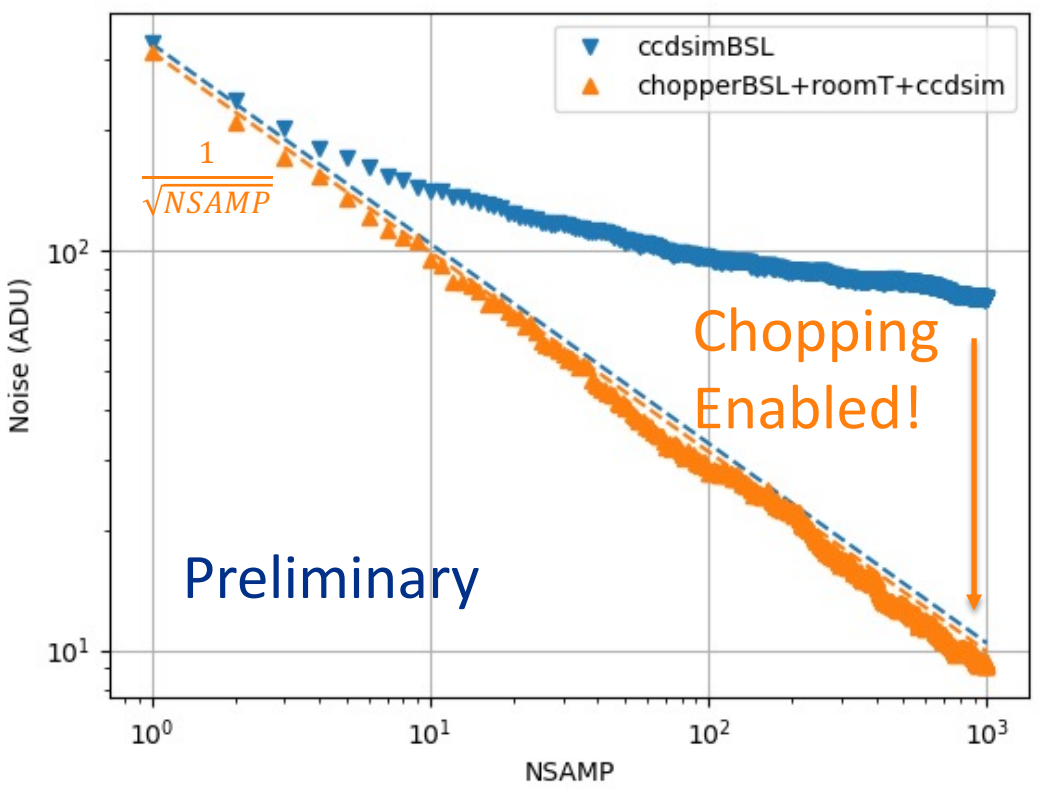
Noise Measurements at Room Temperature and Liquid Nitrogen

- At room temperature, single integration noise with MIDNA alone is successfully 1/3 of noise with CCD included!
- Averaging was saturated out due to 1/f noise being injected after CDS
- Removed with updated clocking!
- Liquid nitrogen setup requires long ribbon cabling that is coupling in noise even without dunking
- Dunking continues to make it worse
- Follows $\frac{1}{\sqrt{NSAMP}}$ much better
- Note bottom trace before next slide



Preliminary Results, $\frac{1}{\sqrt{NSAMP}}$ Scaling Restored!

- The averaging method assumes no 1/f added after CDS
- The integrator adds some small amount of 1/f noise
- Chopping in the integrator used to eliminate 1/f noise contribution
- Restored the $\frac{1}{\sqrt{NSAMP}}$ scaling!
- Room temperature
- AC grounded input



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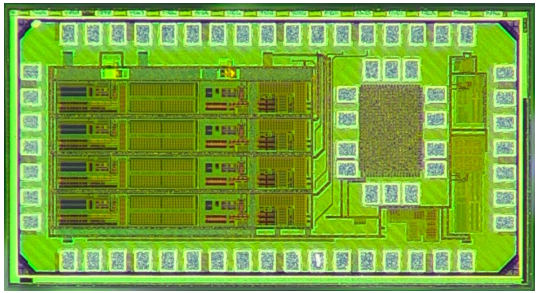
Results and Future Work for MIDNA

- Successfully less than 1/3 of CCD noise even at room temperature!
- Cryogenic functionality down at 77 Kelvin!
- Controlled temperature testing with CCD in progress

MIDNA Chip Image



- Starting design work for next version of chip
- Grow to many more channels to follow the CCD, up to 64
  - Project scaling is currently limited by cost of readout
- Integrate reference generator and analog-to-digital converter
  - Greatly reduce the sensitive analog signals going off chip
- Enable digital processing of data on chip
  - The ADC combined with on-chip memory enables many averaged reads internally
  - Improves noise, power, and complexity compared to analog solutions, especially off chip