Vertical Drift Update

- wirecell 0.17.0 available with gojsonnet
 - Many thanks to Kyle Knoepfel and Lynn Garren
 - <u>https://cdcvs.fnal.gov/redmine/issues/26157#change-85710</u>
 - Brett's blog summarizing wirecell updates in 0.15.0, 0.16.0, 0.17.0
 - https://wirecell.github.io/news/posts/releases-15-16-and-17/
- one file pgrapher/common/tools.jsonnet in dune_pardata needs to be updated for the 3view-30 FR to work

Configuration update for Vertical Drift in dunetpc:

- <u>Nitish's update</u> for configurable plane labeling + many infrastructure updates
- Use PDSP ColdElecResponse for Vertical Drift to remove the pepper noise found by Slavic
- Switch to use jsonnet for VD Sim much easier to change parameters
- Sim-SigProc combined workflow to reduce mem, disk usage
- Better interface with fcl configuration
 - default units consistent with DUNE services
- PR: <u>https://github.com/absolution1/dunetpc/pull/4</u>

Update for Horizontal Drift undergoing

gojsonnet is much faster!

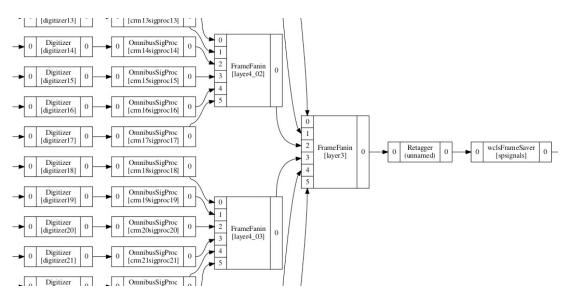
compiling the config. for VD Sim

real	3m3.728s	jsonnet
sys	3m1.922s 0m1.540s	
		-
		-
\$time	./js.sh wcls-sim	-drift-simchannel
	./js.sh wcls-sim	-drift-simchannel gojsonnet
\$time real user		

VD Sim/SigProc is roughly 2-3 min/event

Some Tests for Vertical Drift

Work	outputCommands	Memory summary	disk
detsim+SigProc (dense)	keep*	VmPeak = 5257.82 VmHWM = 3979.98	9.1M
detsim+SigProc (sparse)	keep*	VmPeak = 2856.98 VmHWM = 1586.26	9.1 M
detsim	keep*	VmPeak = 5688.31 VmHWM = 4423.21	125 M



- Current WC graph keeps all last output edges and write out once, maybe write out for each edge may help
- Noise is hard to compress losslessly.
- Matthew Man and Nikolina Ilic from U. Toronto are investigating 2D ROI to mask signal regions.

