IF03 3D integration

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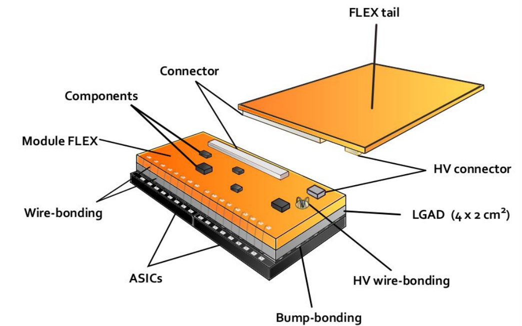
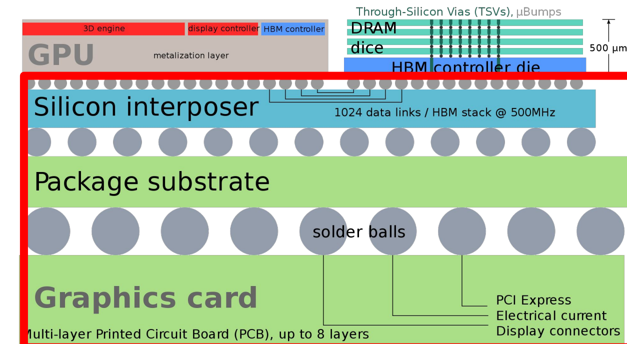
R. Lipton: https://www.snowmass21.org/docs/files/summaries/IF/SNOWMASS21-IF3_IF0_Ronald_Lipton-080.pdf
S. Mazza: https://www.snowmass21.org/docs/files/summaries/IF/SNOWMASS21-IF3_IF5_Simone_Mazza-175.pdf
R. Patti: https://indico.fnal.gov/event/45749/contributions/198237/attachments/135412/167907/NHanced_Snowmass_10012020.pdf

Current packaging

- As of now sensor to chip connections in HEP have been mostly relying on bump bonding
- Bump bonding technology is reliable but has its limitations
  - Only works down to 20-50 um of pitch and has issues of yield for fine connections
  - Solder balls increase the input capacitance to the amplifier and hence the noise
  - Connection is subject to heat stress since it involves different materials
  - Needs silicon interposer for planar connections or side extension of chip for external connections
  - Limits minimum thickness since both chip and sensor need thick enough support wafer
- Advanced packaging may solve part of these issue
  - Improving both performance, yield and processing

HGTD module (https://cds.cern.ch/record/2719855)

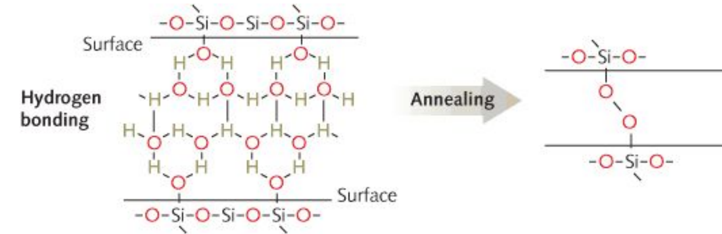


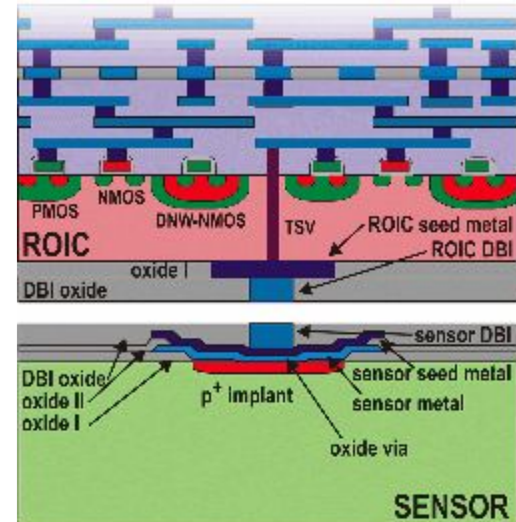


3D technologies

- 3D integration now allows tight packaging of sensor and chip
  - Or stacks of multiple chips
- Many technologies available
  - Direct Bonding Interconnect (DBI) most widely accepted: silicon covalent oxide bonding, copper diffusion bonding
- Can be done for wafer to wafer (w2w) or die to wafer (d2w) assembly
- Through Silicon Via (TSV) connections allows to have multiple planes stacked and connected
  - With external connections not needing extensions or interposers

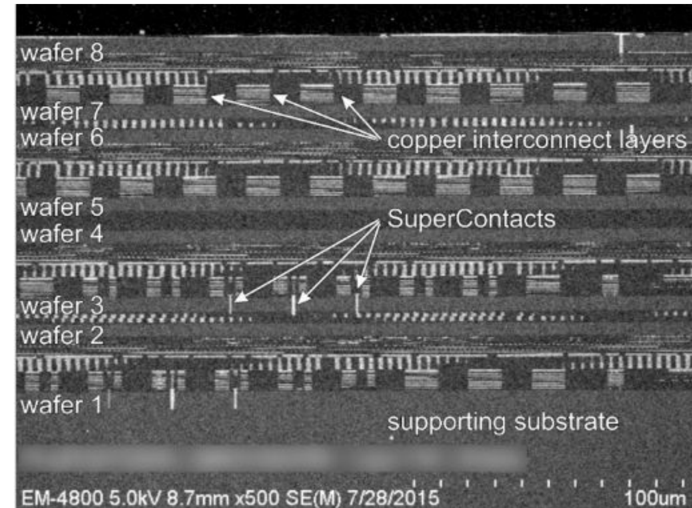
Si covalent oxide bonding





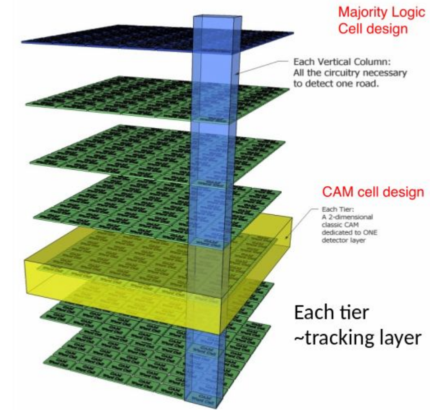
Advantages of 3D integration

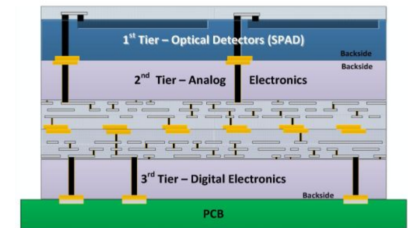
- **Less space**: 3D chips can be multilayer and do not need extension or interposers for external connections
- Very **fine pitch** bonding (~3 micron)
- **Better connections**: faster and shorter than in circuit boards, with reduced dissipated power
- **Better performance**: reduced input capacitance and lower noise
- **Layered design**: e.g. sensor + analog electronics + digital electronics, each layer can be manufactured by different producers
- **Reduced thermal stress** and increased heat dissipation since material is homogeneous, also **increased robustness**
- **Reduction** of single layer **thickness**, after integration all supports can be removed



Possible applications (mostly R. Lipton LOI)

- **3D integrated SiPM** with advanced signal processing
- **Tile assembly**: chip tile array assembled at wafer level with no edges
- **Small pixels** (10 um or less) that reduces the input capacitance of thin sensors (e.g. thin LGADs) increasing both space and time precision
- **Double sided connection** for LGADs to have readout connections on both sides
- **Stacked 3D integrated chip**, creating a 3D network of algorithm cells for advanced pattern recognition
- **Zero mass trackers** with very thin and highly populated layers of 3D integrated sensor+chip for tracking close to interaction point
- **Sensor stacks** for high energy X-ray detection
- **Substrate engineering**, like buried layers for LGAD fabrication (e.g. DJ-LGAD, buried LGAD)
- Many others!

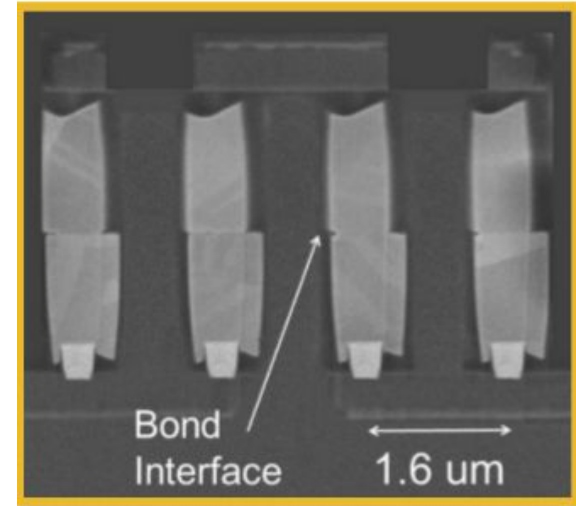


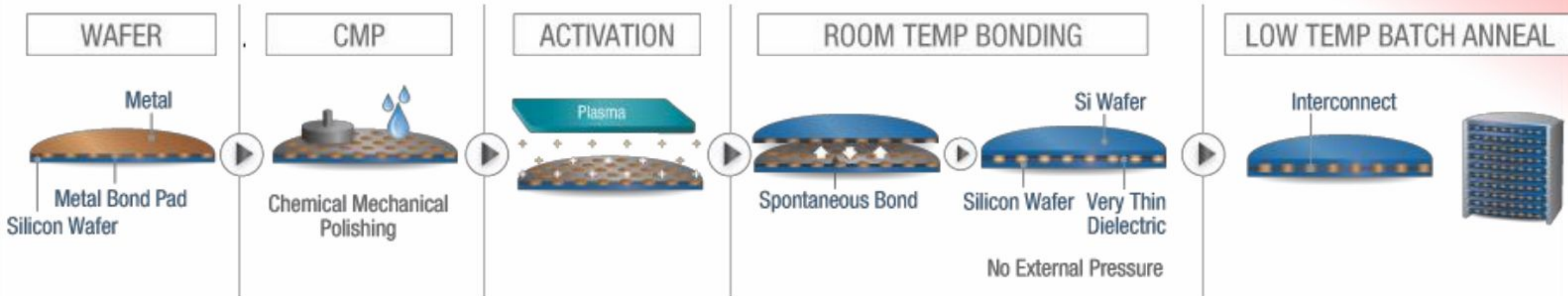


(J.F Pratte Sherbrooke)

NHanced capabilities (R. Patty)

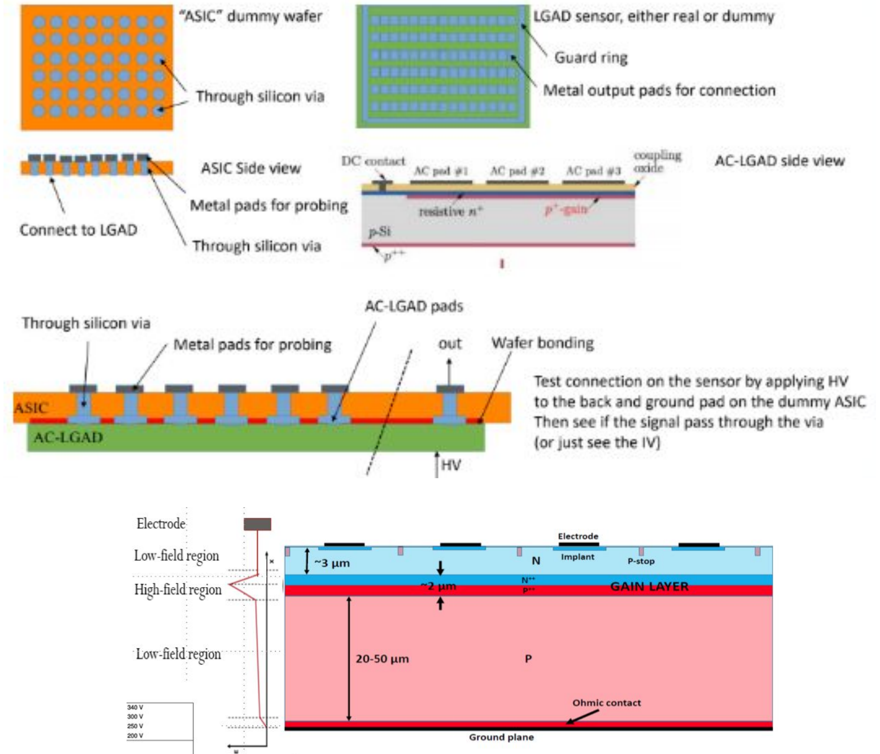
- NHanched have been in the 3D integration business for over a decade
  - Hybrid bonding, Oxide bonding, Si Interposers
- Lower temperature (down to 150 C) bonding
- Bonding yield around 70-80 % with very fine pitch





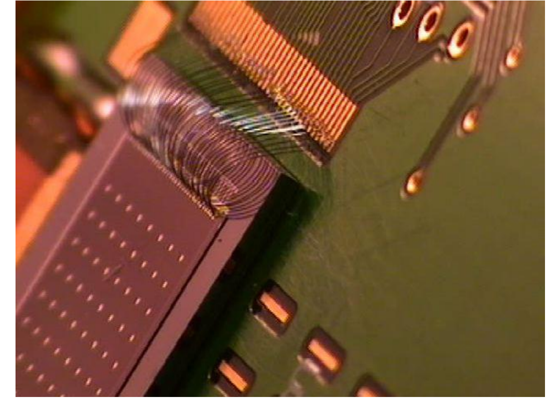
CACTUS material capabilities (R. Islam)

- Low temperature wafer to wafer and chip to wafer bonding capabilities
- Currently working with UCSC to demonstrate successful 3D integration of high density LGADs to readout using TSVs
- Wafer2wafer bonding for deep substrate engineering (DJ-LGAD, Buried LGAD)
  - https://arxiv.org/abs/2101.00511
- Effort funded by awarded SBIRs



Status

- 3D integration still lacks a large scale research application
  - But recent efforts produced or will produce working prototypes of 3D integrated modules
- Pursued by FNAL since some time
  - E.g. “3D integration of sensors and electronics” https://doi.org/10.22323/1.309.0025
  - Comparison of performance of 3D integrated sensor vs bump bonded
- UCSC (new in the game) working with cactus material to test 3D integration and substrate engineering of LGADs
  - Funded through SBIR, expected results early next year



White paper structure

Proposed title: **Integration and packaging**

- Introduction to technology
  - Review of companies available with respective capabilities
- Advantages in respect to current available packaging
- Foreseen applications for 3D integration
  - Possible use in oncoming experiments (EIC, X-rays ...)
- Preliminary results (FNAL past results, possible UCSC near future results)
- Path for future development
- Conclusions

Conclusions

- Time has come for detector packaging to ramp up for the next generation of experiments.
  - New challenges on many fronts: need for finer pitch, lower noise, higher density...
- There are many promising technologies for 3D integration becoming available that have the potential to revolutionize the next generations of experiments
  - Current “blue sky” development will pay off in the long run
- We need to think about what technologies will be available 10 years from now and start developing the tools to use them