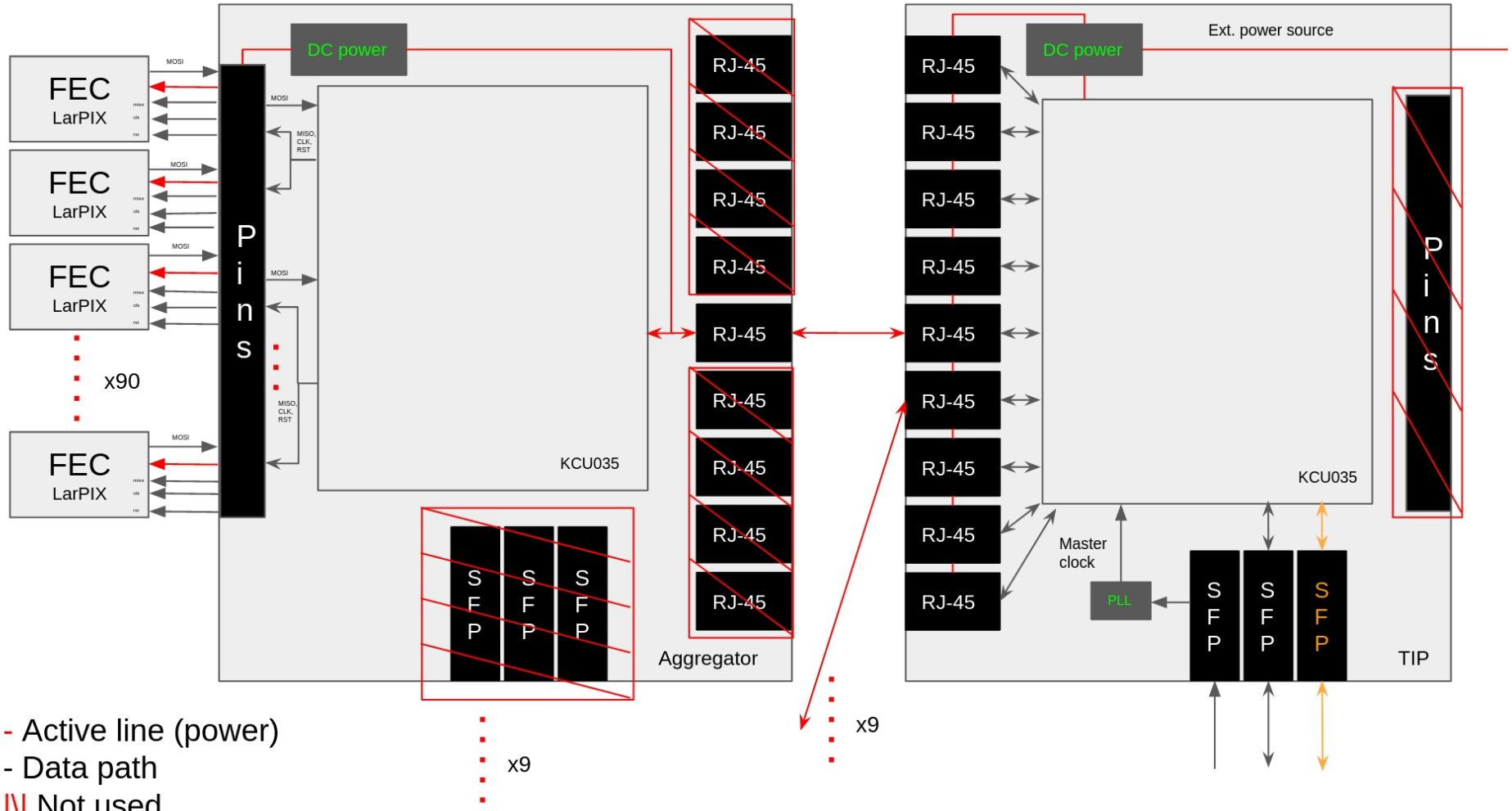
Test procedures

- I. Xiotidis

- HPgTPC Electronics meeting
- Date: 2/11/21

Board layout

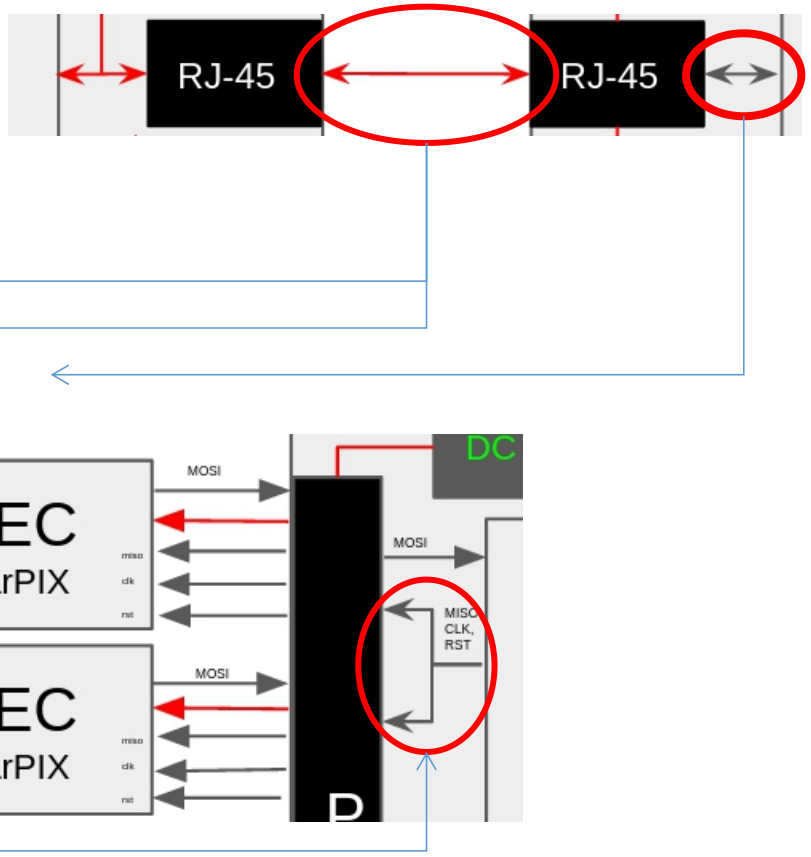


- Active line (power)
- Data path
|\| Not used
- Control port (might become redundant)

- Two type of tests available:
  - Hardware component tests (serial links, power distribution, etc.)
  - Firmware component tests

Hardware tests overview

- We can test various hardware compoents with the two available test boards in the lab
  - Power board (made by Duncan): Allows to power 4 RX/TX lines with DC voltage over RJ45
  - Xilinx evaluation card (Commercial): Hosts same FPGA family and transceiver type as the final boards
    - Any objection to move test set-up from FC7 to the eval. card?
- Proposed hw tests:
  - The TIP <-> AGGR link contains a number of components:
    - GTH transceivers from Xilinx
    - Ethernet cable (long distance) + DC signal
    - Vessel feedthrough
    - Custom serial transceiver circuit (e.g. bias network, ESD diodes, etc.)
  - AGGR<-> FEC links from FPGA fabric (HP/HR banks)
    - Paired in groups of two for configuration and reset
    - Rate much smaller than serial links
    - Do we want to test the FEC communication links?
      - We cannot use Eval card out of the box
      - Extra adapter is required
    - Eye scans with oscilloscope (performed from Johan in the past)
  - Any other component we can test?



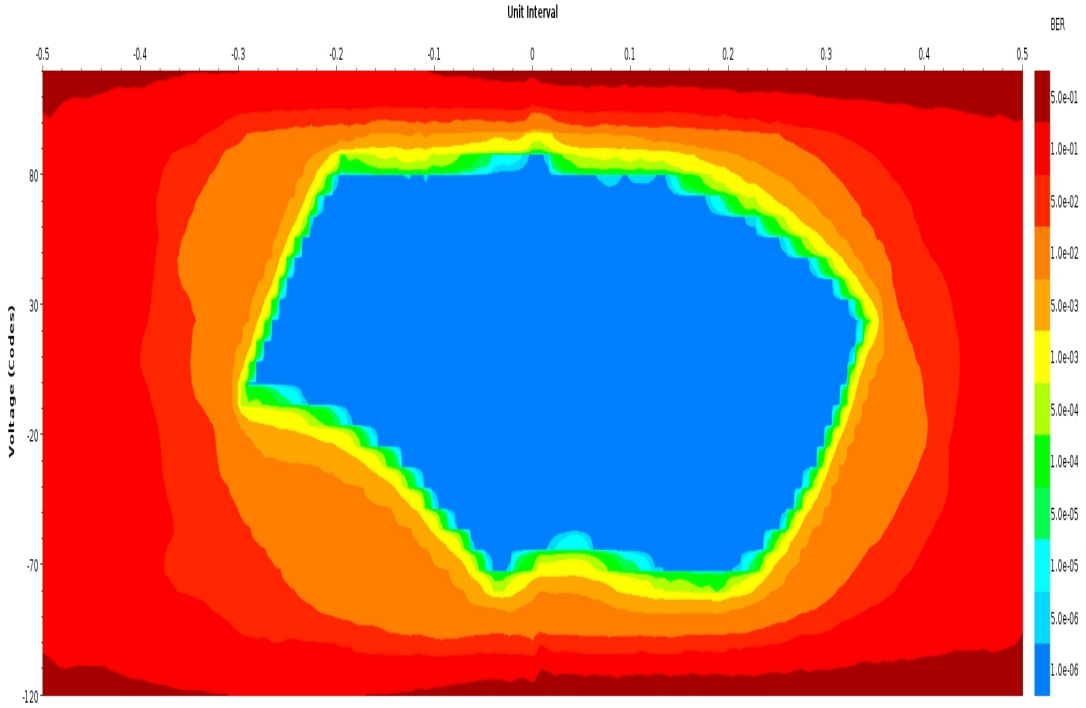
Testing signal integrity on serial transceivers

- Current hardware allows 4xGTH transceiver tests via the FMC connector
  - Power can be provided externally with DC power supply
  - FMC extender card allows setup to be tested in the magnetic field (what is the status for that?)
  - 4-5x ethernet cables available to be tested
  - 1x feedthrough for high pressure
- What tests are available (@1Gbps):
  - Tune the GTH transceivers with sweap scans to derive base configuration
    - 4x parameters with all combinations can be changed (Swing, Pre/Post cursor, RX termination)
    - Equalization network (LPM-short distance vs DFE-long distance)
  - Cable standard (CAT5/6) and length + feedthrough
  - Cable + DC power
  - Test impedance elements (currently air-cored inductors)
  - Anything else?

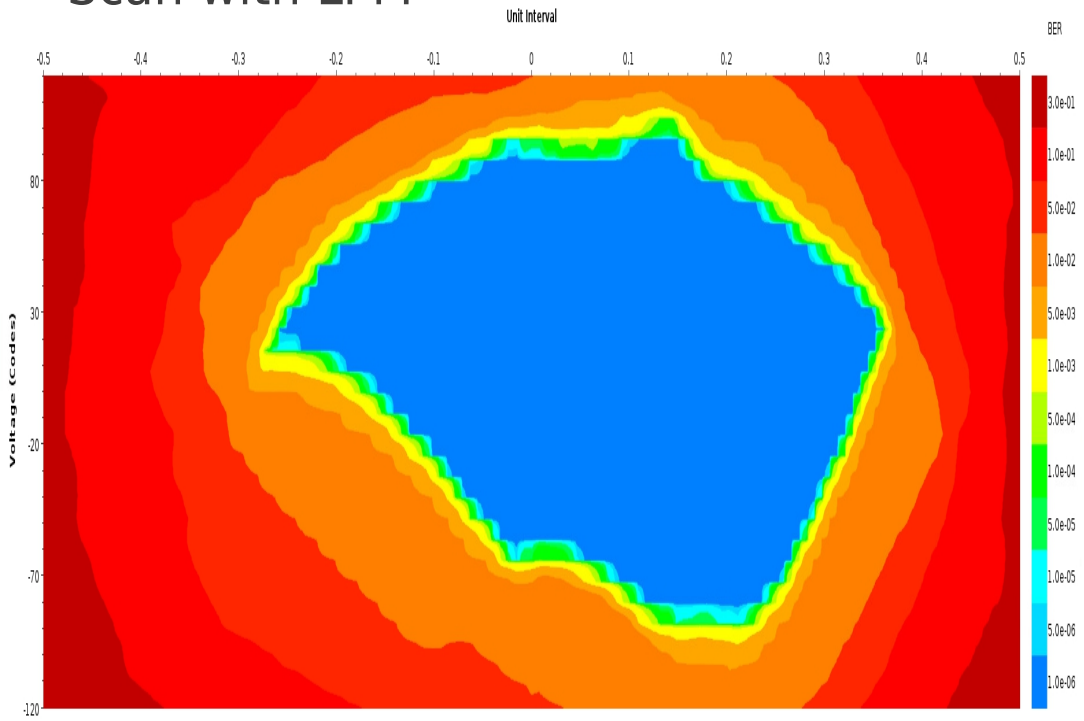
Current scan status

Transceiver parameters:
* Line rate: 1Gbps
* Pre/Post cursor: 0dB
* TX Swing: 0.995 V
* RX Term: ?

- Scan with DFE



- Scan with LPM



Wrote ROOT based macro to automated scan procedure to avoid Vivado

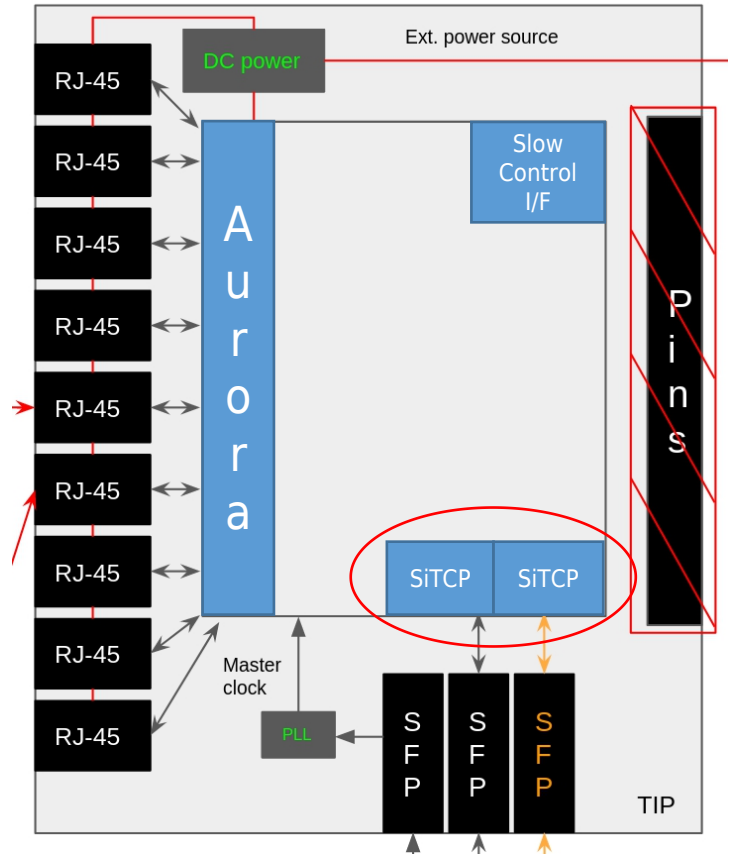
Firmware tests

- Current focus on TIP firmware implementation in kcu105 card
  - In case FPGA parts are late can we use this as back-up TIP?
    - What about aggregators?
- Firmware can be separated in three high level blocks:

- Each component can be tested with evaluation card initially
  - Almost same boxes for Aggregator (what about the LArPIX?)

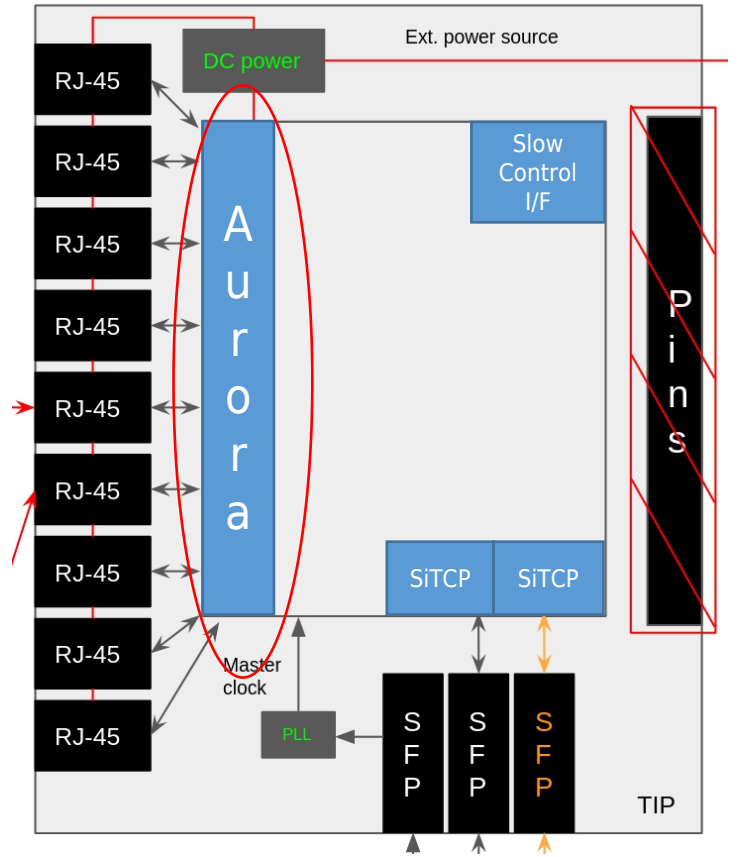
Interfacing block

- Contains all required I/Fs decoders for data processing
- Block break down:
  - SiTCP: TCP core from beebeans
    - Interfaces network with processing logic
    - Current status: Implementation to kcu105 completed -> ping operation works but ~20% of packages are lost (under investigation)
    - Testing:
      - Send data to fifo and read back
      - Saturate link to measure throughput (p2p connection)
      - Anything else?



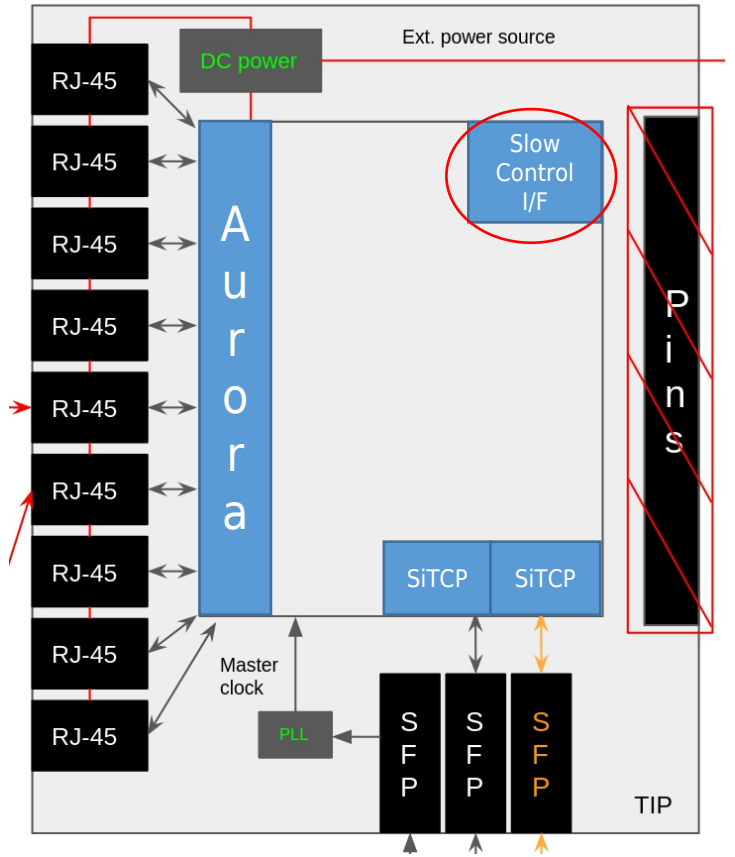
Interfacing block

- Contains all required I/Fs decoders for data processing
- Block break down:
  - Aurora 8b/10b core: Standard IP-block from Xilinx (well documented)
    - Interfaces Aggregators with processing logic
    - Current status: Configured via Vivado GUI, include In-System IBERT core
      - IBERT core (resources permitted) will remain also in final design to allow online integrity tests for link quality
    - Testing:
      - After transceiver configuration derived from hardware tests repeat same eye scans with data from FIFOs
      - Not much internal stuff to be checked



Interfacing block

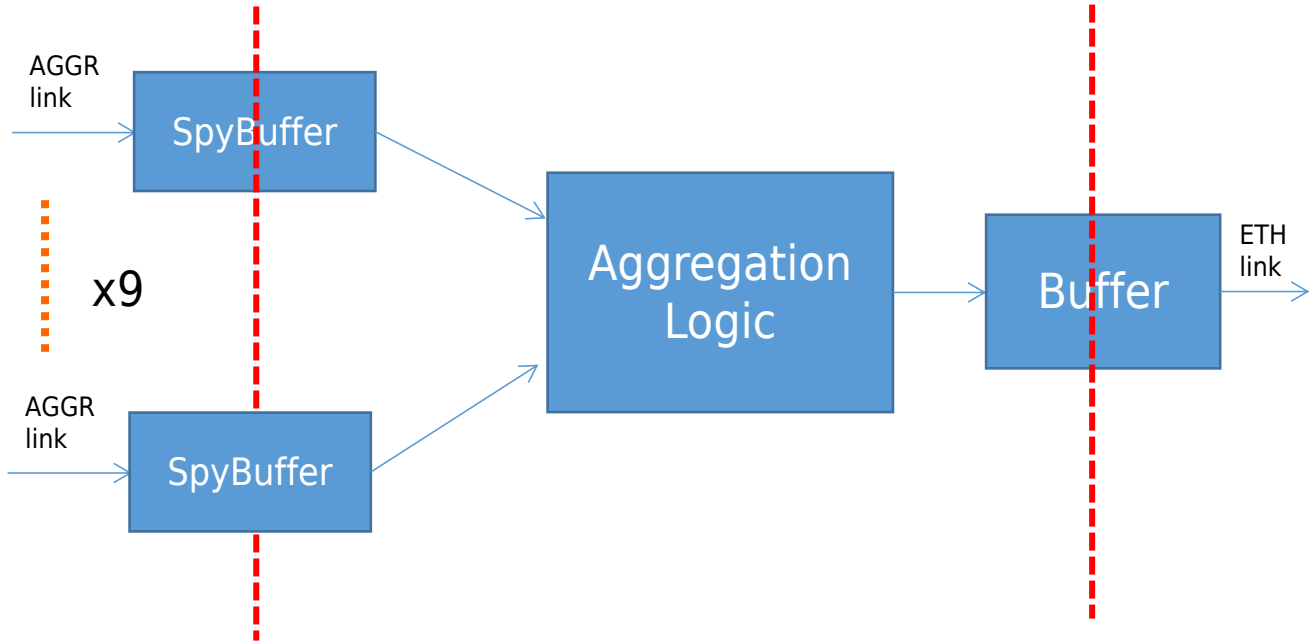
- Contains all required I/Fs decoders for data processing
- Block break down:
  - Slow control I/F: Masters for board configuration interfaces (SPI,I2C,etc.)
  - Interfaces with control/monitoring logic
    - Current status: Not much developed, implementations of I2C/SPI/PMbus masters are available and will be used
    - Testing:
      - Once hardware components available tests master behaviour with data from the con/mon path
      - Anything else?



Aggregation logic

- Main data path block:
  - Retrieves data from 9x Aurora links
    - 8-bit@62.5MHz
  - Buffering with spy buffers:
    - RAM+FIFO (possibly): FiFo will buffer the data to enter the aggregation logic block, RAM will keep copy to be accesed from control/monitoring interface
  - Aggregation logic: TBD
    - Higher clock frequency
  - Buffering with normal buffer (don't think we need data copy)
  - Transmitts to 1x ETH link
    - 8-bit@125MHz

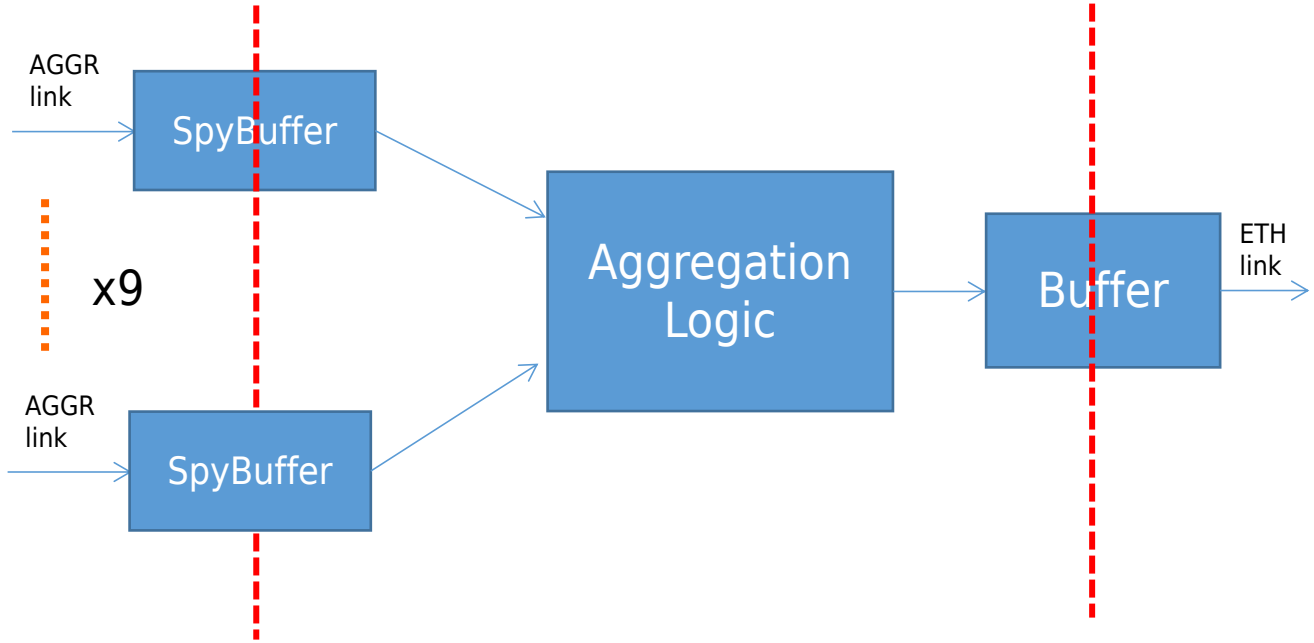
- Preliminary layout



Aggregation logic

- Current status: Identified spy buffer from past ATLAS project
  - Will ask around also if CMS has something similar (more support within the group)
- Testing:
  - Initially one aggregator will be assumed to setup proper handshaking
  - Interface with control/monitoring logic to identify needed information
  - Duplicate for 2x aggregators (design needed for test beam)

- Preliminary layout



Control/Monitoring logic

- Block required for configuring the system and monitor the status
- Current status: Haven’t thought much about implementation yet
  - Setup meeting with Alex T. to discuss data formatting for DAQ I/F
- Testing: TBD

Summary

- Hardware tests:
  - Check signal integrity of all Aggregator2TIP links in as close as possible conditions
    - Identify maximum cable length
    - DC voltage limit
    - Critical components
  - Missing still LArPIX timeline
    - Rate is much smaller than Aurora link, do we want to test the connector?
- Firmware tests:
  - SiTCP evaluation in progress with first loopback tests over TCP
  - Aurora links evaluated once hardware tests define baseline configuration for GTH
  - Aggregation logic requires a bit more thinking for details
  - Con/Mon: Not much developed but about to take up
- Am I missing anything?