Vertical Drift **Top Drift Electronics** Numerology

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> Apologies for having postponed so many times

- defined and what's not
- And start thinking where we want to go...

These slides some facts, numbers and formats of the Top Detector Electronics from the DAQ perspective to start building a common understanding of what's



NOTA BENE

The TDE electronics descends from the NP02 Dual Phase electronics

- strictly speaking it's EXACTLY the same
- In NP02 the AMCs responsible to buffer data and responding to triggers
 - See Dario's presentation: <u>https://indico.fnal.gov/event/50169/contributions/220266/</u> attachments/145752/185674/TDE data transmission.pdf
- > The AMCs will operate in a different mode in DUNE VD (streaming)
 - and interface with DAQ (DUNE, not theirs)
- TDE numbers has to be taken with a grain of salt
 - Data formats, protocols, etc have to be adapted/reoptimised
 - Some modifications have been already made (no compression, 40G MCH, etc...) but the underlying firmware is ~the same
 - No overhauls expected, but we've started the discussion



VERTIGAL DRIFT DETECTOR LAYOUT

- 80 CRP/drift volume
 - Charge Readout Plane
- 1 CRP made of 2 CRUs
 - Charge Readout Unit





1 CRU











TOP DRIFT ELECTRONICS NUMBERS



		ltem	Quantity
	1.5 m x 1.7 m CRUs	320	
	Anode ch	annels per CRP	3200
	Channels per FE ca	rd or AMC card	64
	FE cards or AMC	C cards per CRP	50
		Number of SFT	105
Upper C	FE car	50	
	Installed FE	50	
		μTCA crates	400
	AMC	cards per crate	10
		WR-MCH	400
	40	Gb/s data links	400
1/4 CRP element: 2432 / 4 ch for 2-view	Anode channels	256,000	
3200 / 4 ch for 3-view			

Sampling frequency: ~2 Mhz =125 Mhz/64



NEW CRT LAYOUT TOP DRIFT ELECTRONICS NUMBERS



3072 channels per chimney

CRP layout optimised in summer to better match BDE electronics modularity

- $\sim 4\%$ reduction in # of (used) channels
- 20% reduction in detector electronics
- Sampling frequency unchanged

	Quantity	ltem
	320	$1.5 \text{ m} \times 1.7 \text{ m}$ CRUs in the top drift
3072	3200	Anode channels per CRP
	64	Channels per FE card or AMC card
48	50	FE cards or AMC cards per CRP
	105	Number of SFT
48	50	FE card slots per SFT
48	50	Installed FE cards per SFT
320	400	μTCA crates
12		AMC cards per crate
320	400	WR-MCH
320	400	40 Gb/s data links
245,760	256,000	Anode channels in the top drift

Sampling frequency: ~2 Mhz =125 Mhz/64



TDE CRATE

Picture from TDE CDR in June

Each AMC

Sampling 12b@2 Mhz

- ► 64 channels
- 1,5 Gb/s output stream
- Each Crate
 - 1 x 40G MCH
 - 12 AMC
 - "Pure" data throughout : ~18 Gbps

(packaging, protocol, encoding)

Closer to 24 Gbps

Aggregated by the on-board MCH switch

40 Gbps crate at IP2I Lyon (MCH-40G-XAUI)





DATA SAMPLING AND TRANSMISSION

- Each AMC acquires all 64 channels @ 2MHz in parallel
- Channel data buffered in the on-board RAM;
 - Storage capability of several ms of data
 - Unclear if needed in streaming mode
- > Streamed out to the MCH switch, 1 channel at a time, in round-robin;
 - Each board acts as source of <u>64 "independent" UDP streams</u>
- Number of samples per channel is configurable

 - the best option.
 - Discussed with TDE experts, no objections

Requirements maximises bandwidth efficiency and minimise transmission complexity Setting the @samples such that size(1 pkt) = 1 Jumbo Frame (MTU 9000) looks like

Proto DUNE UDP DATA packet Format

• • •	IP/ UDP Header + Data Header 48 bytes (64 bits aligned)						Source Source Source Source	IP[2] = IP[3]= MAC[4] = MAC[5] =	32+ChassisNum AMC slot + 12 = chassisNum+1 = AMC slot + 12		
	UDP Lenght	UDP lenght	OxD (4 bits)	OxE (4 bits)	OxF (4 bits)	Total Packet Number (6 bits)	Current Packet Number (6 bits)	ADCchannel (6 bits)	Global Packet Counter (MSB)	Global Packet Counter(LSB)	
	ADCs or Encoded Huffman Sequence (10000 samples for protoDUNE) No compression => 2 packets of 8000 bytes (4000 samples) + 1 packet of 4000 bytes (2000 samples)										
	Compression => 1 packets of 8048 bytes max Size of Huffman Sequence is the UDP length – 6 bytes										

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DP DATA FORMAT

Created:	140ct2021										
Updated:											
Version:	1										
	63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 23 1 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 3 2 1										
0	MAC Header										
1	UDP Header MAC Header										
2	UDP Header										
3	UDP Header										
4	UDP Header										
5	48bit DP Data Header UDP Header										
6	reserved	Sample t0+3	reserved	Sample t0+2	reserved	Sample t0+1	reserved	Sample t0+0			
7	reserved	Sample t0+7	reserved	Sample t0+6	reserved	Sample t0+5	reserved	Sample t0+4			
8	reserved	Sample t0+11	reserved	Sample t0+10	reserved	Sample t0+9	reserved	Sample t0+8			
1125	served	Sample t0+11	reserved	Sample t0+10	reserved	Sample t0+9	reserved	Sample t0+8			
1126											

- My attempt to put the numbers on a spreadsheet Chances are it's all wrong :)
- Known issues:
 - Source information are part of the IP/UDP header (problematic on many levels)
 - The DP data header holds information relevant to the old DP daq
 - Nota bene: This is NOT what will be used for the VD ethernet readout, but it's the starting point



INTERVALLO : STANDARD RAW DATA HEADERS

- Sadly we don't one
- It's becoming clear that this has to change, or to run at the risk of overcomplicating data processing and bookkeeping
- Initiated discussion with offline last week
 - The picture below is a proposal for a header format uniquely identifies source and creation time of any data fragment (Far and Near detector)
 - To be discussed with detector experts

DET data formats											
 Agree on a minimal common header with all detectors 											
K/D	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0										
0	Link Slot Crate DetID Version										
1	DTS timestamp[31:0]										
2	DTS timestamp[63:32]										
 This breaks backward compatibility but we are sure that it will be very beneficial for the future 											



A POSSIBLE ETHERNET FORMAT?

If one puts things together... DISCLAIMER: Not discussed with TDE experts yet

Version:	1										
	63 62 61 60 5	59 58 57 56 55 54 53 52 51 50 49 48	47 46 45 44	43 42 41 40 39 38 37 36 35 34 33 32	31 30 29 28	27 26 25 24 23 22	21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6	5 4 3 2 1	
0	MAC Header										
1	UDP Header MAC Header										
2	UDP Header										
3	UDP Header										
4	UDP Header										
4	48bit DP Data Header ???? UDP Header										
5	Reserved? Link Slot Crate Det ID Ver										
7	DTS timestamp										
6				TIA	time						
8	reserved	Sample t0+3	reserved	Sample t0+2	reserved	Samp	le t0+1	reserved	Sample	e t0+0	
9	reserved Sample t0+7 reserved Sample t0+6 reserved Sample t0+5 reserved Sample t0+4								e t0+4		
10	reserved	Sample t0+11	reserved	Sample t0+9 reserved Samp			e t0+8				
1125	reserved	Sample t0+11	reserved	Sample t0+10	reserved	Samp	le t0+9	reserved	Sample	e t0+8	
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Note: in the example, samples size is artificially blown up from 12b to 16b to favour byte alignment

Alas: 12b > 16b blows increases the crate throughput from $\sim 18Gbps$ to $\sim 25Gbps$ • Very close to the 100Gbps limit, some thought required







SOME THOUGHTS ABOUT TRAFFIC

- > AMC streams out data from each channel as an independent UDP stream
 - i.e. 768 per Crate, 3072 for each CRP
- 100 G readout unit
 - Each Ethernet 100G readout unit would receive 3072 independent UDP stream
 - Streams interleaved with each other



Modularity and bandwidth arguments point towards aggregating 4 crates in a

WHAT DOES IT MEAN FOR PACKET ORDERING?

More or less like



- Assuming, MTU=9000B, 2B/sample (conservative), the interval between packets from the same channel is $\Delta t_{chan} = 2.25$ ms
 - Note: transmitting 9000B at 100 Gbps should take much less, $O(10\mu s)$
- Risk of packets arriving out of order seems small
- Any attempt of reordering would have to deal with "large" gaps between packets from the same stream
 - Does this make sense?





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